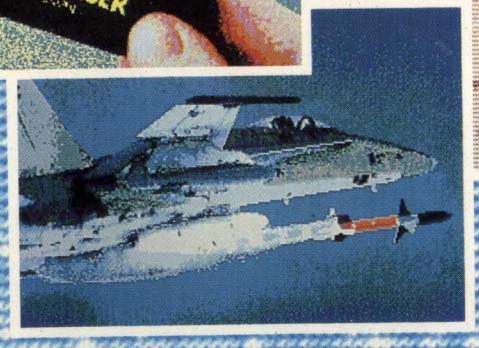
SEPTEMBER 1988

LINEAR
IC Handbook



Plessey Semiconductors

LINEAR
IC Handbook

PLESSEY
Semiconductors

Foreword

Plessey Semiconductors is recognised as a leading supplier of high speed Bipolar Linear integrated circuits. Over 20 years of experience in high speed Bipolar technology has earned Plessey Semiconductors a reputation for quality, reliability and above all outstanding performance.

Backed by an unrivalled Bipolar process Plessey has led the field in Radar and Radio market sectors, producing products like the SL521 logarithmic amplifier which was designed in 1964 and is still being designed into new equipment.

Today, using 3 micron oxide isolated Bipolar processes with on-chip capacitors, logarithmic amplifiers with over 1.3GHz bandwidth are achievable. Our new op-amp the SL2541 (with a small signal bandwidth, of over 800MHz) is outperforming the best Gallium Arsenide.

In radio, high levels of integration coupled with low power has always been our speciality. Offering a range of very low power superhet IF amplifiers to high frequency Direct Conversion receivers, ideal for use in portabe receivers such as paging. For example our SL6655 FM receiver operates from 0.9V and consumes as little as 1mA.

Performance, quality, reliability and service are what our customers have come to expect and we don't expect our customers to accept anything less. Plessey Semiconductors continues to meet those expectations.

Contents

Product index

Operational amplifiers

Type	Supply Voltage	Supply Current	Bandwidth	Maximum Offset Voltage	Open Loop Gain	Page
SL541B	+12V, -6V	16mA	100MHz	5mV	70dB	29
SL562	±1.5V to ±10V	20μA to 5mA	50kHz to 4MHz	5mV	95dB	49
SL2541B	±9V to ±15V	25mA	800MHz	22mV	70dB	103
SL6310C	4.5V to 15V	15mA	1MHz	20mV	50dB	130
TAB1043	±1.5V to ±12V	50μA to 5mA	50kHz to 4MHz	5mV	95dB	202
ZN424P[1]	±2V to±18V	5.5mA at ±12V	20kHz to 1MHz	6mV	86dB	216

1. ZN424P is a gated op amp

Very low noise amplifiers

Type	Function	Bandwidth	Gain	Input Noise Voltage	Page
SL561B	Preamplifier	6.0MHz	60dB	0.8nV/√Hz(Typical)	45
SL561C	Preamplifier	6.0MHz	60dB	0.8nV/√Hz(Typical)	45
ZN459	Preamplifier	15MHz	60dB	1.1nV/√Hz(Guaranteed)	227
ZN460	Preamplifier	6.0MHz	60dB	1.1nV/√Hz(Guaranteed)	236

Matched transistor arrays

Type	LV_{CEO} Min.	LV_{CEO} Typ.	I_{CM}	Typ. Cut-Off Frequency	No. of Transistors	h_{FE} (Min.)	Page
SL360G	7V	14V	50mA	2.2GHz	2	30 at 5mA	13
SL362C	7V	14V	50mA	2.2GHz	2	30 at 1mA	13
SL2363	6V	9V	12mA	5.0GHz	6	20 at 8mA	78
SL2364	6V	9V	12mA	5.0GHz	6	20 at 8mA	78
SL2365	6V	9V	12mA	5.0GHz	8	50 at 8mA	80
SL3127	15V	25V	20mA	1.6GHz	5	40 at 1mA	111
SL3145	15V	25V	20mA	1.6GHz	5	40 at 1mA	115
SL3227	6V	9V	12mA	3.0GHz	5	40 at 1mA	119
SL3245	6V	9V	12mA	3.0GHz	5	40 at 1mA	121

Product index (continued)

Logarithmic/limiting amplifiers

Type	Supply Voltage	Supply Current	Bandwidth	Noise Figure	Gain	Page
SL521A	6V	15mA	100MHz	4dB	12dB (±0.5)	15
SL521B	6V	15mA	100MHz	4dB	12dB (±0.7)	15
SL521C	6V	15mA	100MHz	4dB	12dB (±1.0)	15
SL523B	6V	30mA	100MHz	4dB	24dB (±1.4)	19
SL523C	6V	30mA	100MHz	4dB	24dB (±2.0)	19
SL523HB	6V	30mA	100MHz	4dB	24dB (±0.4) (matched gain sets, MIL 883B)	19
SL531C	9V	17mA	500MHz		10dB (±2)	23
SL532C[1]	9V	10mA	400MHz		10dB (±2)	26
SL1521A	5.2V	15mA	220MHz	3dB	12dB (±0.5)	65
SL1521C	5.2V	15mA	200MHz	3dB	12dB (±1.1)	65
SL1523C	5.2V	30mA	200MHz	3dB	24dB (±3)	68
SL1613C	6V	15mA	80MHz	4.5dB	12dB (±2.0)	73
SL2521B[2]	6V	40mA	1300MHz	9dB	16dB (±1.2)	82
SL2521C[2]	6V	40mA	1000MHz	9dB	16dB (±1.2)	93

1. The SL532C is a hard limiter
2. The SL2521 is an S.D. log amp and a limiting amplifier

Wideband amplifiers

Type	Supply Voltage	Supply Current	Bandwidth	Noise Figure	Gain	Page
SL550G	6V	11mA	125MHz	2dB	42dB	34
SL560C	2-15V	20mA	300MHz	2dB	35dB	40
SL952	5V	70mA	1GHz		35dB	62

Radiocoms

Type	Function	Page
SL610C	85MHz RF Amplifier, 20dB - AGC capability	52
SL611C	50MHz RF Amplifier, 26dB - AGC capability	52
SL612C	15MHz RF Amplifier, 34dB - AGC capability	52
SL621C	AGC Generator (from detected audio)	55
SL623C	AMSSB detector with AGC	58
SL640C	Double balanced modulator (emitter follower O/P)	60
SL641C	Double balanced modulator (open collector O/P)	60
SL1610C	RF Amplifier 120MHz, 20dB	70
SL1611C	RF Amplifier 80MHz, 26dB	70
SL1612C	RF Amplifier 15MHz, 34dB	70
SL1640C	Double balanced modulator (emitter follower O/P)	76
SL1641C	Double balanced modulator (open collector O/P)	76
SL6140	400MHz RF amplifier, 45dB - AGC capability	123
SL6270C	Gain controlled microphone preamplifier/VOGAD	127
SL6310C	500mW switchable audio amplifier	130
SL6440A/C	High level mixer (A grade has military temperature range)	133
SL6601C	FM IF, PLL detector (double conversion) and RF mixer	136
SL6652	Low power IF/AF circuit (with RSSI) for FM cellular radio	151
SL6653	Low power IF/AF circuit for FM receivers	159
SL6654	Low power IF/AF circuit (with RSSI) for FM cellular radio	164
SL6700A	AM IF and detector (double conversion) with noise blanker (military temperature range)	190
SL6700C	AM IF and detector (double conversion) with noise blanker	194
SL6701A	AM IF and detector (double conversion)	198
ZN414Z	AM radio receiver	205
ZN415E	AM radio receiver	205
ZN416E	AM radio receiver	205

Low power radio receivers

Type	Function	Page
SL6638	200MHz direct conversion FSK data receiver	142
SL6655	Ultra low power FM radio receiver	170
SL6670	0.9V DC/DC voltage converter	177
SL6691	IF system for paging receivers	187

Product List - alpha numeric

Technical Data

PLESSEY
Semiconductors

SL360G & SL362C

HIGH PERFORMANCE NPN DUAL TRANSISTOR ARRAYS

The SL360G and SL362C are high performance NPN dual transistor arrays fabricated as monolithic silicon devices. They feature accurate parameter matching and close thermal tracking. They have high transition frequencies (typ. 2.2GHz) and low device capacitance. In addition the SL362C offers good noise performance (1.6dB noise figure at 60MHz).

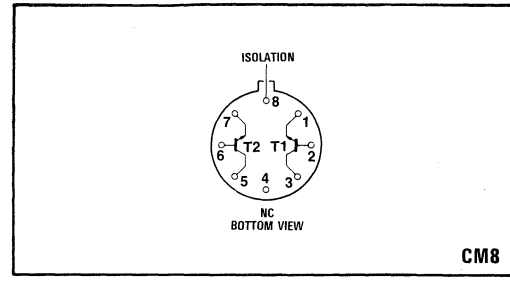


Fig. 1 Pin connections

APPLICATIONS

- Instrumentation
- PCM Repeaters
- Analog Signal Processing
- High Speed Switches — Digital and Analog

FEATURES

- Accurate Parameter Matching.
- High f_T (1.5GHz min., SL360)
- Low Noise (1.6dB at 60MHz SL362)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Type	Value			Units	Conditions
			Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	Both	10	32		V	I_C = 10μA
Collector isolation breakdown	BV_{CIO}	Both	16	60		V	I_C = 10μA
Emitter base leakage	I_{EBO}	SL360/362C			1	μA	V_{EB} = 4V
Emitter base leakage	I_{FBO}	SL360			1	nA	V_{EB} = 2V
Collector emitter breakdown	LV_{CEO}	All	7	14		V	I_C = 5mA
DC current gain	H_{FE}	SL360	30	65			V_{CE} = 2V, I_E = 5mA
		SL362	30	70			V_{CE} = 2V, I_E = 1mA
Transition frequency	f_T	SL360G	1.6	2.2		GHz	V_{CE} = 2.5V, I_E = 25mA, f = 200MHz (See Notes)
		SL362	1.0	1.5		GHz	V_{CE} = 5V, I_F = 5mA, f = 200MHz
Input offset voltage	V_{BE1} - V_{BE2}	SL360		3	10	mV	V_{CE} = 2V, I_E = 1mA
		SL362		5		mV	V_{CE} = 2V, I_E = 1mA
Input offset current	H_{FE1}/H_{FE2}	Both	0.9	1.0	1.1		V_{CE} = 2V, I_E = 5mA
Saturation voltage	$V_{CE(SAT)}$	SL360		0.25	0.6	V	I_E = 10mA, I_B = 1mA
Noise figure	NF	SL362		1.6	2.0	dB	I_E = 1mA, R_S = 200Ω, f = 60MHz
Collector base capacitance	C_{OB}	SL360		0.5		pF	V_{CB} = 0V
		SL362		1.3		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}	SL360		2.3		pF	V_{CI} = 0V
		SL362		3.8		pF	V_{CI} = 0V
Emitter base capacitance	C_{TE}	SL360		0.5		pF	V_{BE} = 0V
		SL362		2.1		pF	V_{BE} = 0V
Forward base emitter voltage	$V_{BE(ON)}$	SL360		0.72		V	I_E = 1mA, V_{CE} = 2V
Collector base leakage	I_{CBO}	SL360			1	nA	V_{CB} = 10V
Collector isolation leakage	I_{CIO}	SL360			1	nA	V_{CI} = 10V

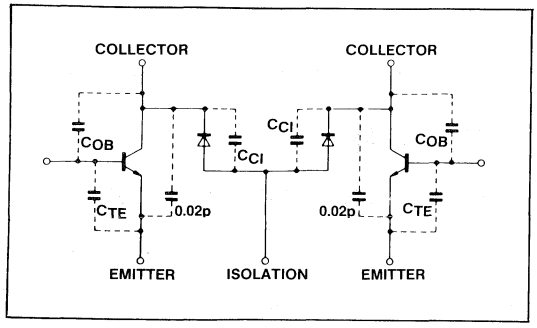


Fig.2 Equivalent circuit for SL360, SL362

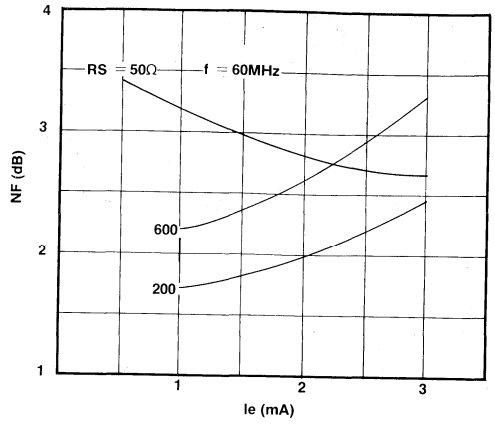


Fig. 3 Typical noise figure emitter current for SL362

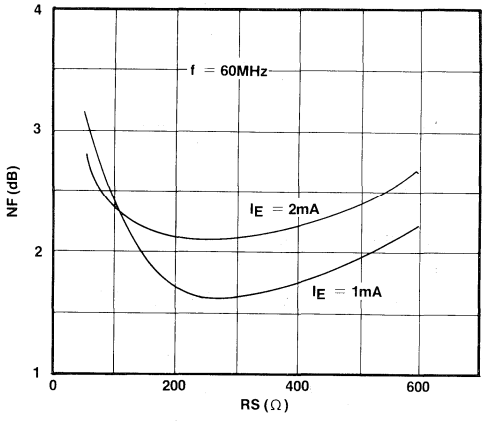


Fig. 4 Typical noise figure v source impedance for SL362

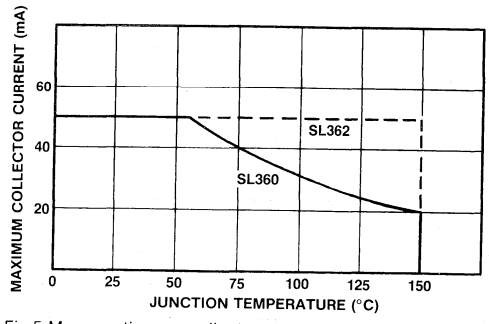


Fig.5 Max. continuous collector current vs junction temperature

ABSOLUTE MAXIMUM RATINGS

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The absolute maximum ratings are limiting values above which life may be shortened or specified parameters may be degraded.

The isolation pin (substrate) must be connected to the most negative point of the circuit to maintain electrical isolation between transistors.

Electrical ratings

V_{CB} = 10V V_{EB} = 4V V_{CE} = 8V
V_{CI} = 16V I_C = 20mA (SL360); 50mA (SL362) (see Figure 5)

Thermal ratings

	CM8
Storage temperature	−55°C to +150°C
Operating junction temperature	150°C
Thermal resistance (see Note 2)	
Chip-to-case	265° C/W
Chip-to-ambient	425° C/W

These figures are worst case, assuming all power is dissipated in one transistor. If the power is equally shared between the two transistors, both thermal resistance figures can be reduced by 50° C/watt.

SL521A, B & C

140MHz WIDEBAND LOG AMPLIFIER

The SL521A, B and C are bipolar monolithic integrated circuit wideband amplifiers, intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 100MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL521 is typically 12dB (4 times). The SL521A, B and C differ mainly in the tolerance of voltage gain and upper cut-off frequency.

The device is also available as the SL521AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Well-Defined Gain
- 4dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 165MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity better than 1dB

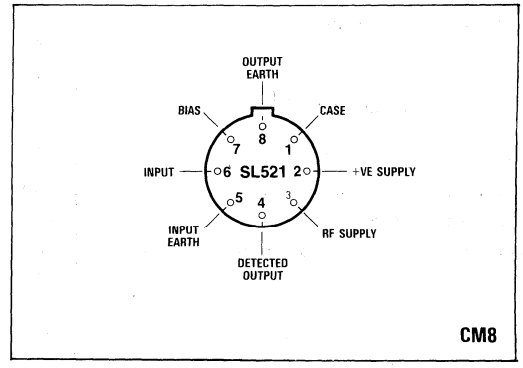


Fig.1 Pin connections - bottom view

ABSOLUTE MAXIMUM RATINGS (Non-simultaneous)

Storage temperature range	-55°C to +175°C
Chip operating temperature	+175°C
Chip-to-ambient thermal resistance	250°C/W
Chip-to-case thermal resistance	80°C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

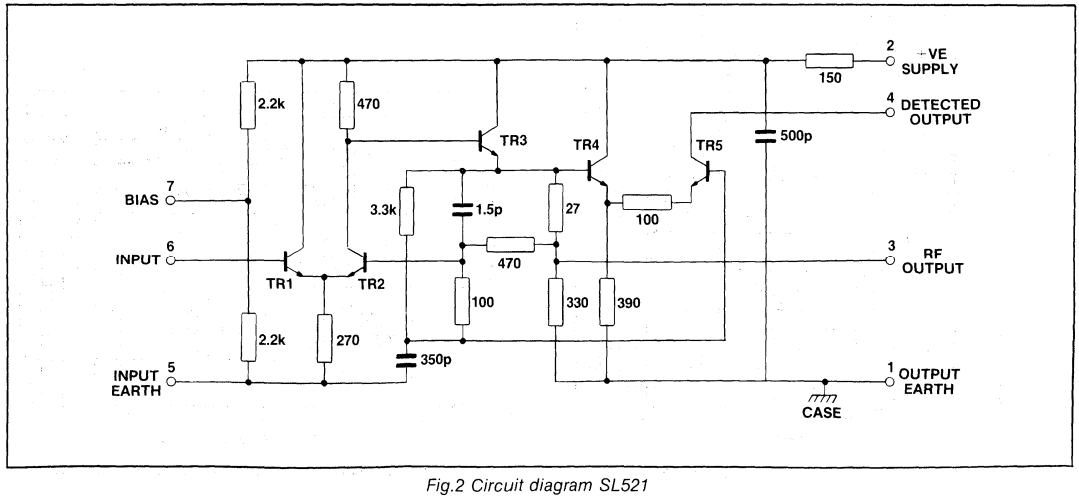


Fig.2 Circuit diagram SL521

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature = +22°C ± 2°C
Supply voltage = +6V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 30MHz	A	11.5		12.5	dB	
	B	11.3		12.7	dB	
	C	11.0		13.0	dB	10 ohms source, 8pF load
Voltage gain, f = 60MHz	A	11.3		12.7	dB	
	B	11.0		13.0	dB	
	C	10.7		13.3	dB	
Upper cut-off frequency (Fig. 3)	A	150	170		MHz	
	B	140	170		MHz	10 ohms source, 8pF load
	C	130	170		MHz	
Lower cut-off frequency (Fig. 3)	A B C		5	7	MHz	10 ohms source, 8pF load
Propagation delay	A B C		2		ns	
Maximum rectified video output current (Fig. 4 and 5)	A	1.00		1.10	mA	
	B	0.95		1.15	mA	f = 60MHz, 0.5V rms input
	C	0.90		1.20	mA	
Variation of gain with supply voltage	A B C		0.7		db/V	
Variation of maximum rectified output current with supply voltage	A B C		25		%/V	
Maximum input signal before overload	ABC	1.8	1.9		V rms	See note below
Noise figure (Fig. 6)			4	5.25	dB	f = 60MHz, Rs = 450 ohms
Supply current	A	12.5	15.0	18.0	mA	
	B	12.5	15.0	18.0	mA	
	C	11.5	15.0	19.0	mA	
Maxiumum RF output voltage			1.2		Vp-p	

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction to TR1 on peaks.

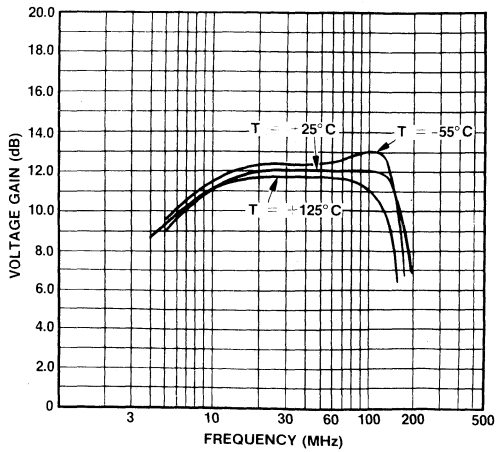


Fig.3 Voltage gain v. frequency (typical)

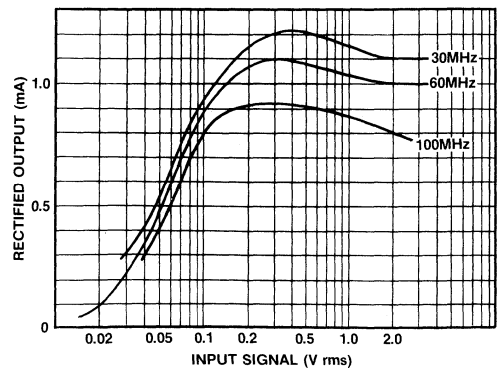


Fig.4 Rectified output current v. input signal (typical)

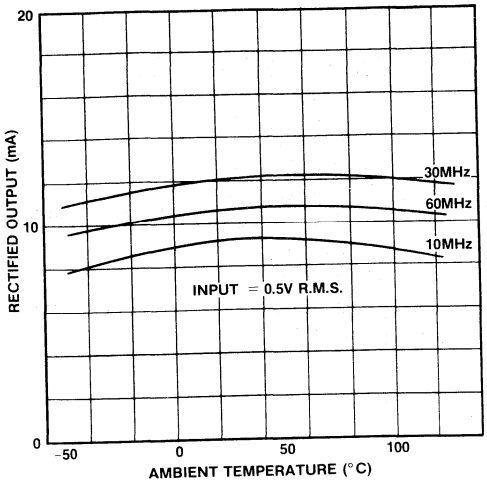


Fig.5 Maximum rectified output current v. temperature (typical)

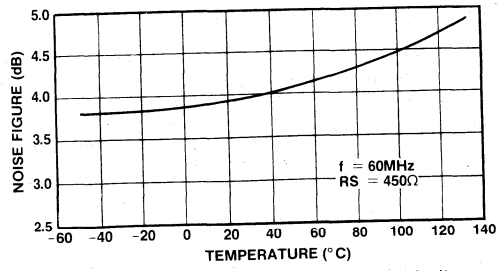


Fig.6 Noise figure v. temperature (typical)

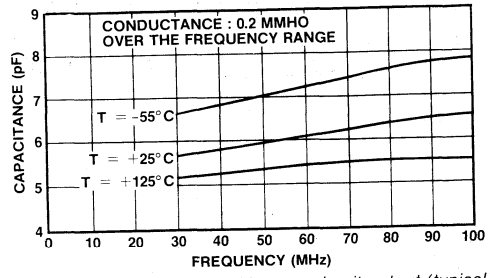


Fig.7 Input admittance with open-circuit output (typical)

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig.8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig.9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required. Alternative arrangements may be derived, based on the parasitic parameters given.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

The amplifiers have been provided with two earth leads to avoid the introduction of common ground lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

The 500pF supply decoupling capacitor has a resistance of, typically, 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (see Absolute Maximum Ratings).

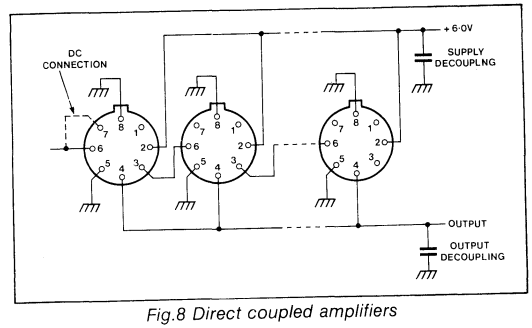


Fig.8 Direct coupled amplifiers

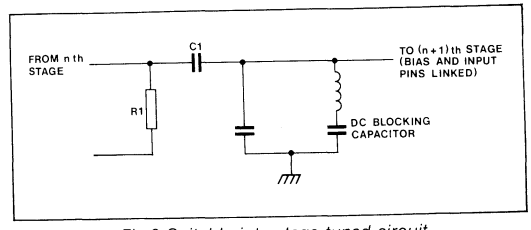


Fig.9 Suitable interstage tuned circuit

Parasitic Feedback Parameters (Approximate)

The quotation of these parameters does not indicate that elaborate decoupling arrangements are required; the amplifier has been designed specifically to avoid this requirement. The parameters have been given so that the necessity or otherwise of further decoupling, may become a matter of calculation rather than guesswork.

$$\frac{\widetilde{I_4}}{V_6} = \frac{\text{RF current component from pin 4}}{\text{Voltage at pin 6}} = 20 \text{ mmhos}$$

(This figure allows for detector being forward biased by noise signals).

$$\frac{V_6}{V_4} = \frac{\text{Effective voltage induced at pin 6}}{\text{Voltage at pin 4}} = 0.003$$

$$\frac{I_2}{V_6} = \frac{\text{Current from pin 2}}{\text{Voltage at pin 6}} = 6 \text{ mmhos (f = 10MHz)}$$

$$\left[\frac{V_6}{V_2}\right]_a = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.03 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 6 joined to pin 7 and
fed from 300Ω source)

$$\left[\frac{V_6}{V_2}\right]_b = \frac{\text{Voltage induced at pin 6}}{\text{Voltage at pin 2}} = 0.01 \text{ (f = 10MHz)}$$

Voltage at pin 2
(pin 7 decoupled)

$\frac{I_2}{V_6}\left[\frac{V_6}{V_2}\right]_a\left[\frac{V_6}{V_2}\right]_b$ decrease with frequency above 10MHz at 6dB/octave

SL523B,C & HB

100MHz DUAL WIDEBAND LOG AMPLIFIER

The SL523B and C are wideband amplifiers for use in successive detection logarithmic IF strips operating at centre frequencies between 10 and 100MHz. They are pin-compatible with the SL521 series of logarithmic amplifiers and comprise two amplifiers, internally connected in cascade. Small signal voltage gain is 24dB and an internal detector with an accurate logarithmic characteristic over a 20dB range produces a maximum output of 2.1mA. A strip of SL523s can be directly coupled and decoupling is provided on each amplifier. RF limiting occurs at an input voltage of 25mV RMS but the device will withstand input voltages up to 1.8V RMS without damage.

The SL523HB is supplied in matched sets of eight devices. The gain at 60MHz of the devices in the set is matched to 0.75dB. In all other respects the device is identical to an SL523B. This selection enables very precise log strips to be produced. Supplied only to Plessey Class B screening including burn-in.

The device is also available as the SL523AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

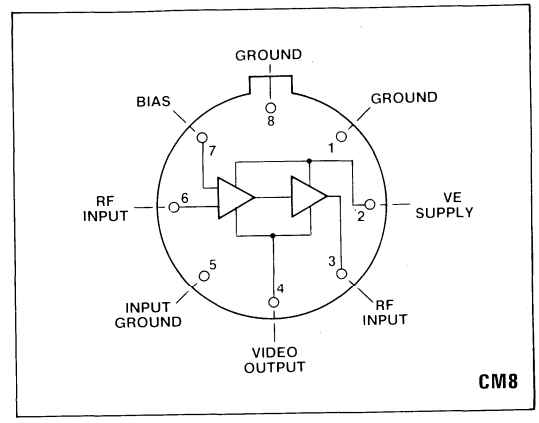


Fig.1 Pin connections (view from beneath)

FEATURES

- Small Size/Weight
- Lower Power Consumption
- Readily Cascadable
- Accurate Logarithmic Detector Characteristic

QUICK REFERENCE DATA

- Small Signal Voltage Gain: 24dB
- Detector Output Current: 2.1mA
- Noise Figure: 4dB
- Frequency Range: 10-100MHz
- Supply Voltage +6V
- Supply Current 30mA

ABSOLUTE MAXIMUM RATINGS

(Non simultaneous)

Storage temperature range	-55°C to +175°C
Operating temperature range	-55°C to +125°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	+9V

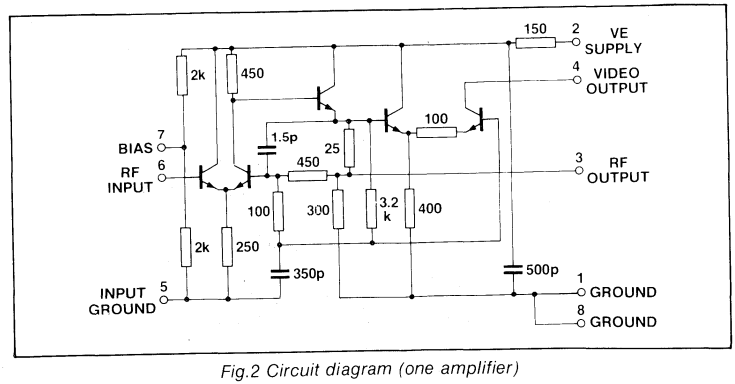


Fig.2 Circuit diagram (one amplifier)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Ambient temperature = 22°C ± 2°C; Source impedance = 10Ω; Supply voltage = +6V; Load impedance = 8pF; Frequency = 60MHz; DC connection between Pins 6 and 7

Characteristic	Type	Value			Units	Conditions
		Min.	Typ.	Max.		
Small signal voltage gain	B,HB	22.6	24	25.4	dB	Frequency = 30MHz
	C	22	24	26	dB	
Small signal voltage gain	B,HB	22	24	26	dB	Frequency = 60MHz
	C	21.4	24	26.6	dB	
Gain variation (set of 8)	HB		0.5	0.75	dB	Frequency = 60MHz
Upper cut-off frequency	B,C & HB	120	150		MHz	
Lower cut-off frequency	B,C & HB		10	15	MHz	
Propagation delay	B,C & HB		4		ns	
Maximum rectified video	B,HB	1.9	2.1	2.3	mA	V_{IN} = 0.5V RMS
output current	C	1.8	2.1	2.4	mA	
Maximum input signal before overload	B,C & HB	1.8	1.9		V RMS	
Noise figure			4	5.25	dB	Source impedance 450Ω
Supply current	B,HB	25	30	36	mA	
	C	23	30	38	mA	
Maximum RF output voltage	B,C & HB		1.2		V p-p	

OPERATING NOTES

The amplifier is designed to be directly coupled (see Fig.5).

The fourth stage in an untuned cascade will give full output on the broad band noise generated by the first stage.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The network chosen must give unity voltage gain at resonance to avoid distorting the log law. The typical value for input impedance is 500Ω in parallel with 5pF and the output impedance is typically 30Ω.

Although a 1nF supply line decoupling capacitor is included in the can an extra capacitor is required when the amplifiers are cascaded. Minimum values for this capacitor are: 2 stages - 3nF, 3 or more stages - 30nF.

In cascades of 3 or more stages care must be taken to avoid oscillations caused either by inductance common to the input and output earths of the strip or by feedback along the common video line. The use of a continuous earth plane will avoid earth inductance problems and a common base amplifier in the video line isolating the first two stages as shown in Fig.6 will eliminate feedback on the video line.

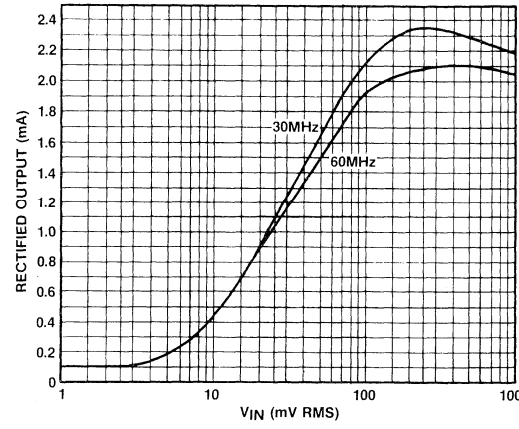


Fig.3 Rectified output current v. input signal (typical)

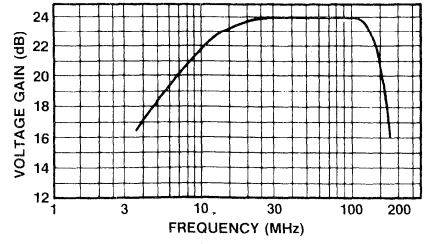


Fig.4 Voltage gain v. frequency (typical)

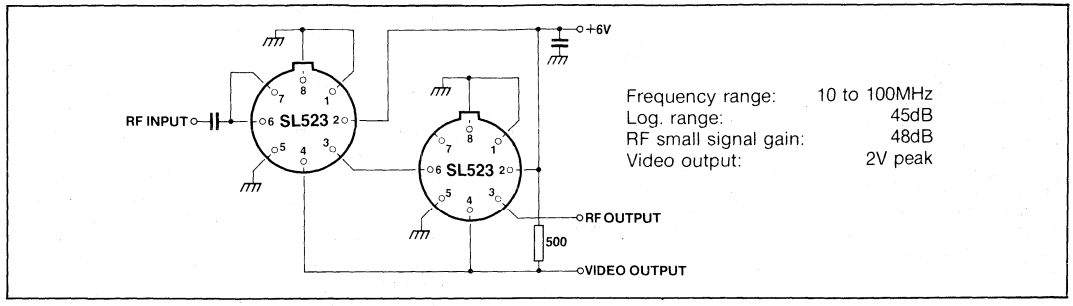


Fig.5 Simple log. IF strip

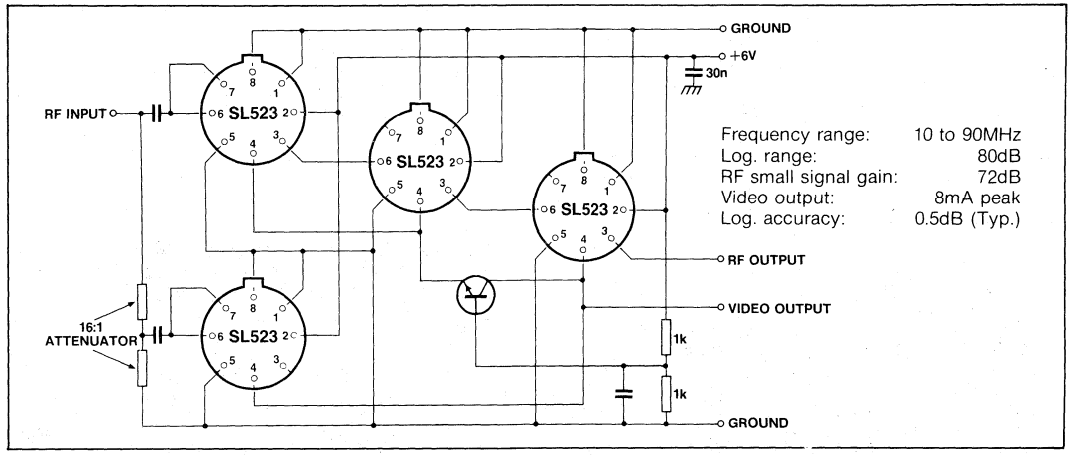


Fig.6 Wide dynamic range log. IF strip

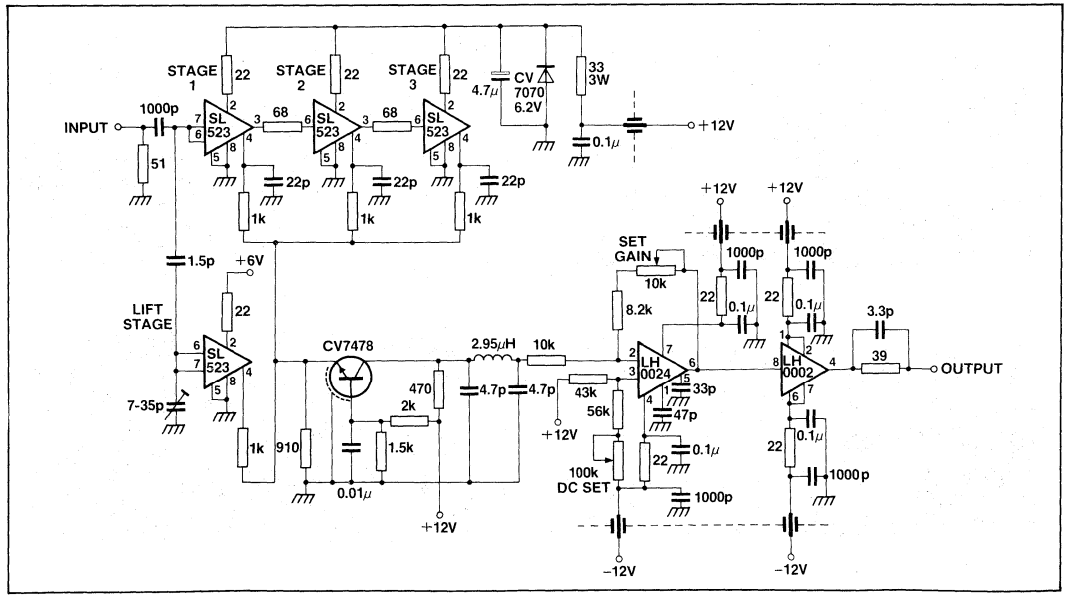


Fig.7 Wideband logarithmic amplifier

TYPICAL PERFORMANCE

Unselected SL523B devices were tested in a wideband logarithmic amplifier, described in RSRE Memo. No. 3027 and shown in Fig.7.

The amplifier consists of six logarithmic stages and two 'lift' stages, giving an overall dynamic range of greater than 80dB. The response and error curves were plotted on an RHG Log Test Set and bandwidth measurements were made with a Telonic Sweeper and Tektronix oscilloscope.

Fig.8 shows the dynamic range error curve and frequency response obtained. The stage gains of the SL523 devices used were as shown in Table 1.

Stages	fo (MHz)	Gain (dB)	Max. Deviation (dB)
1	60	24.123	0.235
2	60	24.089	
3	60	23.888	
Lift	60	24.086	

Table 1 Stage gains of SL523 used in performance tests

The input v. output characteristic (Fig.8a) is calibrated at 10dB/cm in the X axis and 1V/cm in the Y axis. 80dB of dynamic range was attained.

The error characteristic (Fig.8b) is calibrated at 10dB/cm in the X axis and 1dB/cm in the Y axis; this shows the error between the log. input v. output characterisitc and a mean straight line and shows that a dynamic range of 80dB was obtained with an accuracy of ±0.5dB.

As a comparison, the log amplifier of Fig.7 was constructed with randomly selected SL521Bs (two SL521Bs replacing each SL523B). Again, a dynamic response of 80dB was obtained (Fig.9a) with an accuracy of ±0.75dB (Fig.9b).

Bandwidth curves are shown in Figs.8c and 9c, where the amplitude scale is 2dB/cm, with frequency markers at 10MHz intervals from 20 to 100MHz. Using SL523Bs (Fig.8c), the frequency response at 90MHz is 4dB down on maximum and there is a fall-off in response after 50MHz. Fig.9c shows that the frequency response of the amplifier falls off more gradually after 40MHz but again the response at 90MHz is 4dB down on maximum.

These tests show that the SL523 is a very successful dual-stage log amplifier element and, since it is pin-compatible with the SL521, enables retrofit to be carried out in existing log amplifiers. It will be of greatest benefit however, in the design of new log amplifiers, enabling very compact units to be realised with a much shorter summation line.

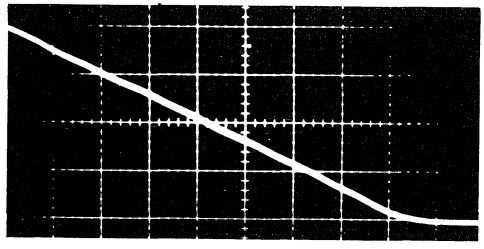


Fig.8a Input/output

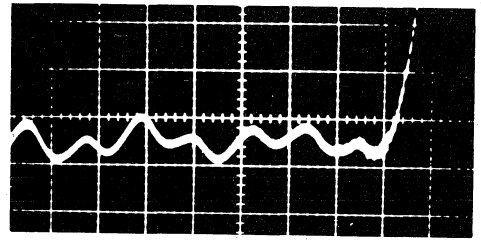


Fig.8b Error curve

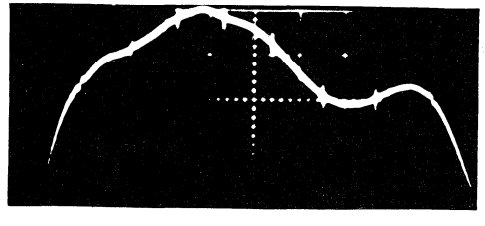


Fig.8c Frequency response, detected output

Fig.8 Characteristics of circuit shown in Fig.7 using SL523Bs

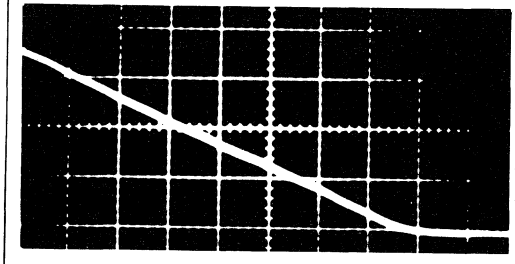


Fig.9a Input/output

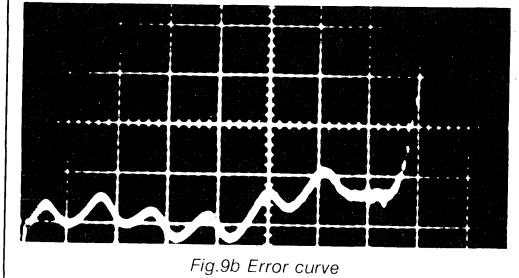


Fig.9b Error curve

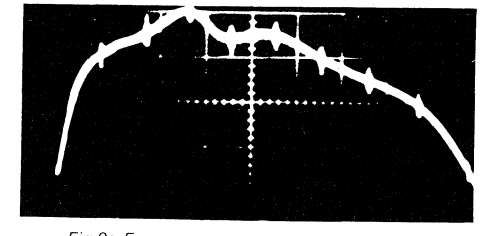


Fig.9c Frequency response, detected output

Fig.9 Characteristics of circuit shown in Fig.7 using SL521Bs

PLESSEY
Semiconductors

SL531C

250MHz TRUE LOG IF AMPLIFIER

The SL531C is a wide band amplifier designed for use in logarithmic IF amplifiers of the true log type. The input and log output of a true log amplifier are at the same frequency i.e. detection does not occur. In successive detection log amplifiers (using SL521, SL1521 types) the log output is detected.

The small signal gain is 10dB and bandwidth is over 500MHz. At high signal levels the gain of a single stage drops to unity. A cascade of such stages give a close approximation to a log characteristic at centre frequencies between 10 and 200MHz.

An important feature of the device is that the phase shift is nearly constant with signal level. Thus any phase information on the input signal is preserved through the strip.

The device is also available as the SL531AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

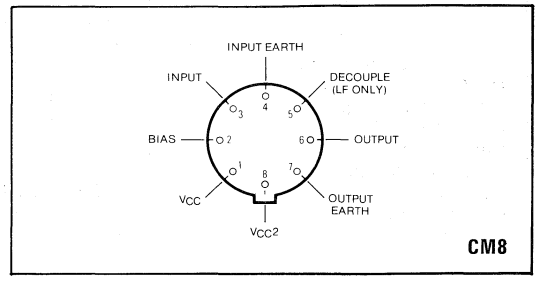


Fig. 1 Pin connections

FEATURES

- Low Phase Shift vs Amplitude
- On-Chip Supply Decoupling
- Low External Components Count

APPLICATIONS

True Log Strips with: —

- Log Range 70 dB
- Centre frequencies 10 — 200 MHz
- Phase Shift ± 0.5 degrees / 10 dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+12 volts
Storage temperature range	-55 °C to +150 °C
Operating temperature range	-55 °C to +125 °C
	See operating notes
Max junction temperature	150 °C
Junction — ambient thermal resistance	220 °C/Watt
Junction — case thermal resistance	80 °C/Watt

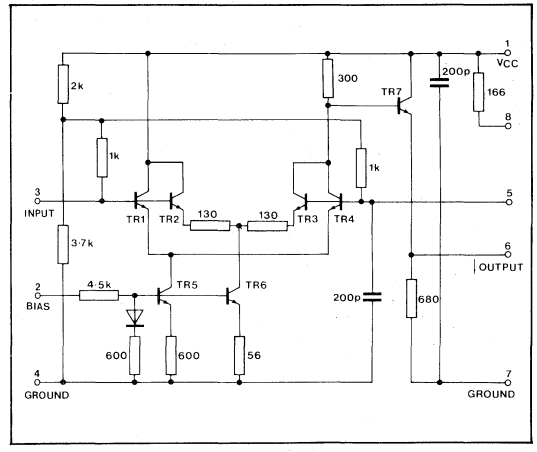


Fig. 2 Circuit diagram

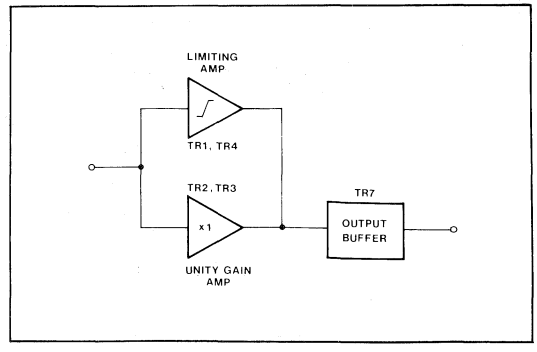


Fig. 3 Block diagram

CIRCUIT DESCRIPTION

The SL531 transfer characteristic has two regions. For small input signals it has a nominal gain of 10 dB, at large signals the gain falls to unity (see Fig 7). This is achieved by operating a limiting amplifier and a unity gain amplifier in parallel (see Fig 3). Tr1 and Tr4 comprise the long tailed pair limiting amplifier, the tail current being supplied by Tr5, see Fig 2. Tr2 and Tr3 form the unity gain amplifier the gain of which is defined by the emitter resistors. The outputs of both stages are summed in the 300 ohm resistor and Tr7 acts as an emitter follower output buffer. Important features are the amplitude and phase linearity of the unity gain stage which is achieved by the use of 5GHz transistors with carefully optimised geometries.

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Test circuit Fig (4)
Frequency 60 MHz
Supply voltage 9 volts
Ambient temperature 22± 2°C

Characteristic	Value			Units	Conditions
	Min	Typ	Max		
Small signal voltage gain	8	10	12	dB	Vin = −30 dBm
High level slope gain	−1	0	+1	dB	
Upper cut off frequency	250	500		MHz	
Lower cut off frequency		3	10	MHz	−3dB w.r.t. ± 60 MHz
Supply current		17	25	mA	
Phase change with input amplitude		1.1	3	degrees	-Vin = 30 dBm to + 10 dBm
Input impedance	2.5pF parallel with 1kΩ				f = 10 - 200MHz
Output impedance	15Ω series with 25nH				

OPERATING NOTES

1. Supply Voltage Options

An on chip resistor is provided which can be used to drop the supply voltage instead of the external 180 ohms shown in the test circuit. The extra dissipation in this resistor reduces the maximum ambient operating temperature to 100°C. It is also possible to use a 6 volt supply connected directly to pins 1 and 2. Problems with feedback on the supply line etc may occur in this connection and RF chokes may be required in the supply line between stages.

2. Layout Precautions

The internal decoupling capacitors help prevent high frequency instability, however normal high frequency layout precautions are still necessary. Coupling capacitors should be physically small and be connected with short leads. It is most important that the ground connections are made with short leads to a continuous ground plane.

3. Low Frequency Response

The LF response is determined by the on chip capacitors. It can be extended by extra external decoupling on pins 5 and 1.

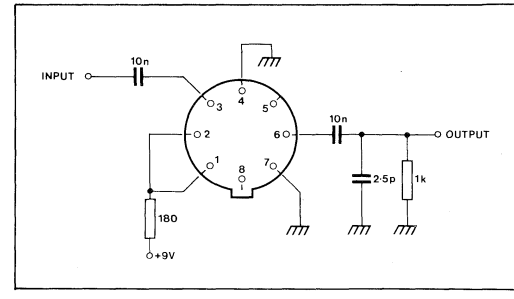


Fig. 4 Test circuit

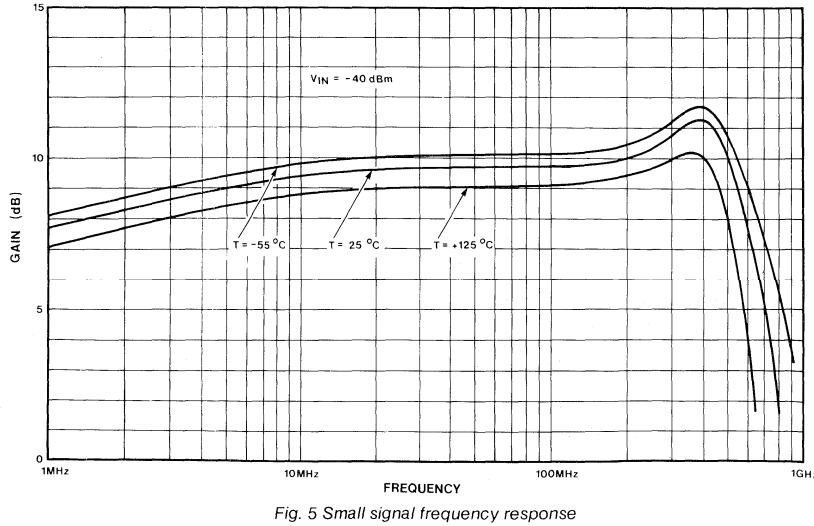


Fig. 5 Small signal frequency response

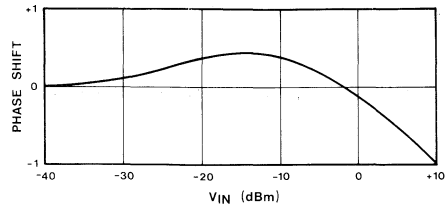


Fig. 6 Phase v. input

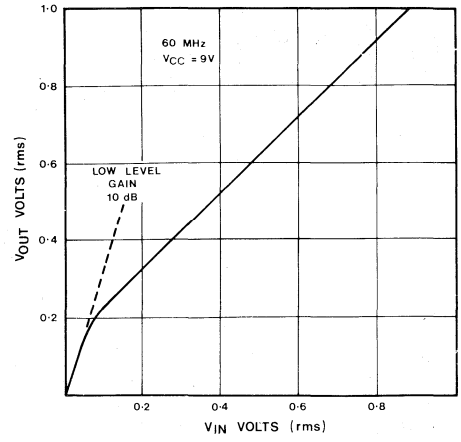


Fig. 7 Transfer characteristics linear plot

TYPICAL APPLICATION — 6 STAGE LOG STIP

Input log range 0dBm to −70dBm
Low level gain 60dB (−70dBm in)
Output dynamic range 20dB
Phase shift (over log range) ±3°
Frequency range 10 — 200MHz

The circuit shown in Fig 9 is designed to illustrate the use of the SL531 in a complete strip. The supply voltage is fed to each stage via an external 180Ω resistor to allow operation to 125°C ambient. If the ambient can be limited to + 100°C then the internal resistor can be used to reduce the external component count. Interstage coupling is very simple with just a capacitor to isolate bias levels being necessary. No connection is necessary to pin 5 unless operation below 10MHz is required. It is important to provide extra decoupling on pin 1 of the first stage to prevent positive feedback occuring down the supply line. An SL560 is used as a unity gain buffer, the output of the log strip being attenuated before the SL560 to give a nominal 0dBm output into 50Ω.

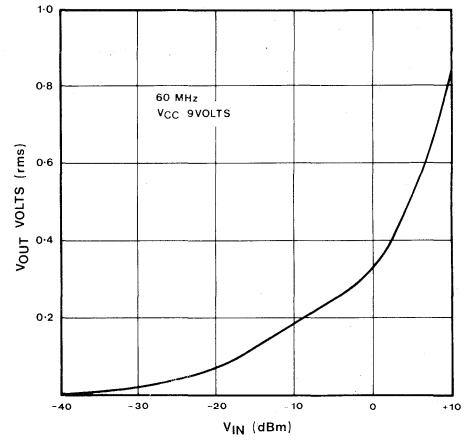


Fig. 8 Transfer characteristics logarithmic input scale

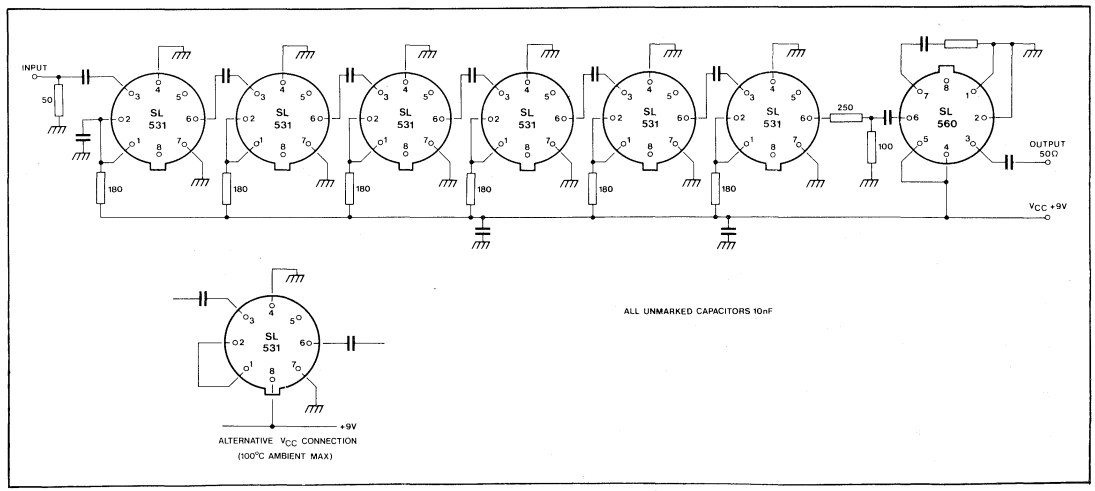


Fig. 9 Circuit diagram 6 stage strip

SL532C

LOW PHASE SHIFT LIMITER

The SL532C is a monolithic integrated circuit designed for use in wideband limiting IF strips. It offers a bandwidth of over 400MHz and very low phase shift with amplitude. The small signal gain is 12dB and the limited output is 1V peak to peak. The use of a 5GHz IC process has produced a circuit which gives less than 1° phase shift when overdriven by 12dB. The amplifier has internal decoupling capacitors to ease the construction of cascaded strips and the number of external components required has been minimised.

The device is also available as the SL532AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

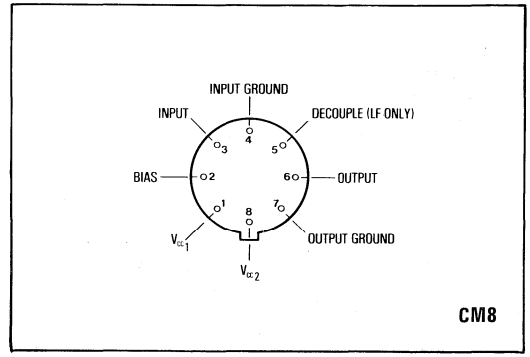


Fig.1 Pin connections

FEATURES

- Low Phase Shift v. Amplitude
- Wide Bandwidth
- Low External Component Count

APPLICATIONS

- Phase Recovery Strips in Radar and ECM Systems (e.g. Doppler)
- Limiting Amps for SAW Pulse Compression Systems
- Phase Monopulse Radars
- Phased Array Radars
- Low Noise Oscillators

ABSOLUTE MAXIMUM RATINGS

Supply voltage	+15V
Storage temperature range	-55°C to +150°C
Operating temperature range	-55°C to +125°C

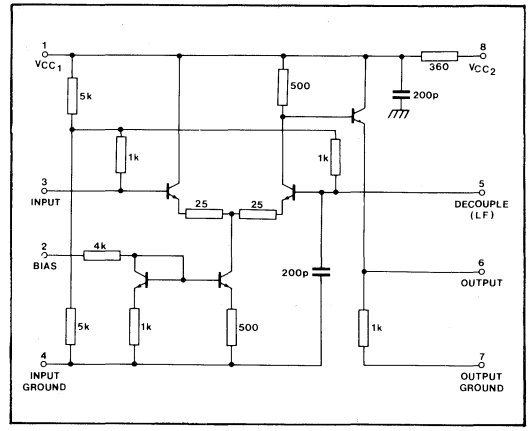


Fig.2 Circuit diagram

CIRCUIT DESCRIPTION

The SL532 uses a long-tailed pair limiting amplifier which combines low phase shift with a symmetrical limiting characteristic. This is followed by a simple emitter follower output stage. Each stage of a strip is capable of driving to full output a succeeding SL532 but a buffer amplifier is needed to drive lower impedance loads. No external decoupling capacitors are normally required but for use below 10MHz extra decoupling can be added on pins 1 and 5. Bias for the long-tailed pair is provided by connecting the bias (pin 2) to the decoupled supply (pin 1).

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature (ambient) 25 °C ± 2 °C
Frequency 60MHz : R_L = 1kΩ/<5pF : V_{IN} = -30dBm
V_{CC} = +9.0V : R_S = 50Ω

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	12.8	14	dB	
Small signal voltage gain		12.5		dB	f = 150MHz
-1dB compression point		-10		dBm	
Limited output voltage	1.0	1.15	1.4	V p-p	V_{IN} = +10dBm
Limited output voltage		1.10		V p-p	f = 150MHz
Upper cut-off frequency	250			MHz	-3dB w.r.t. 60MHz
Lower cut-off frequency			10	MHz	May be extended by decoupling pin 5
Supply current	6	8.5	11	mA	No signal
Phase variation with signal level		±1	±3	Degrees	-30dBm to +10dBm
		±1.5		Degrees	-30dBm to 0dBm. f = 150MHz
Absolute phase shift input to output		-21		Degrees	f = 60MHz
		-34		Degrees	f = 100MHz
		-43		Degrees	f = 150MHz
		-69		Degrees	f = 200MHz
Input impedance		1kΩ/2.5pF			
Output impedance		30Ω			
Noise figure		7		dB	400Ω source impedance. f = 60MHz
Gain variation with temperature		±2		dB	-40 °C to 85 °C
Phase variation with temperature		±0.5		Degrees	-40 °C to +85 °C at any level between -30dBm to +10dBm
Limited output voltage variation with temperature		±0.05		V p-p	V_{IN} = +10dBm -40 °C to +85 °C

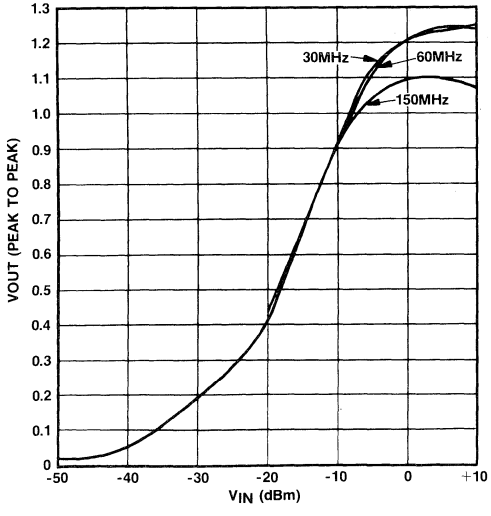


Fig.3 Transfer characteristic of a single stage

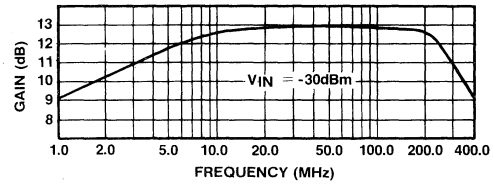


Fig.4 Gain/frequency curve of a typical device

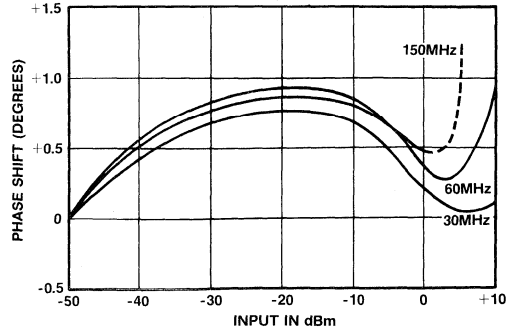
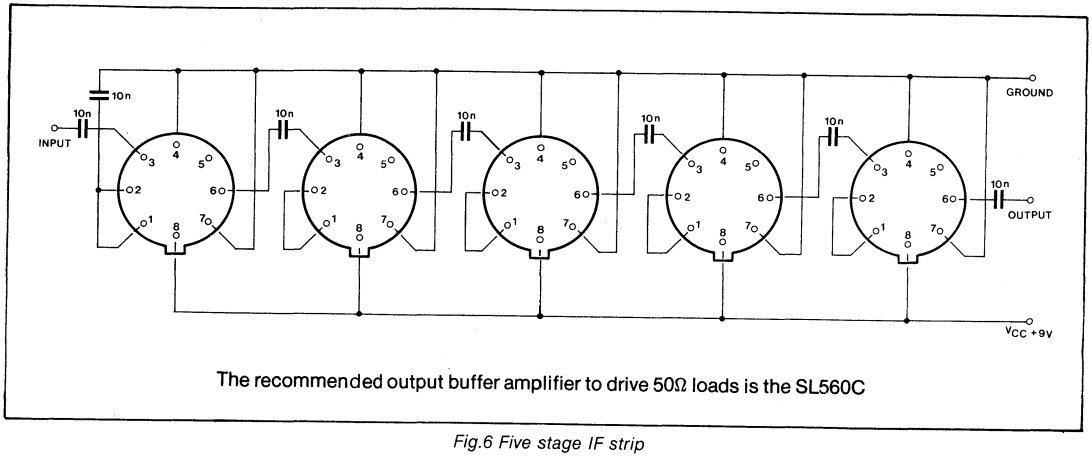


Fig.5 Phase change with input level

TYPICAL APPLICATION

Five stage strip

Input signal for full limiting	300μV rms -57dBm
Limited output	1V p-p
Phase shift (V_{IN} -57 → +10dBm)	±3° typ.



The recommended output buffer amplifier to drive 50Ω loads is the SL560C

Fig.6 Five stage IF strip

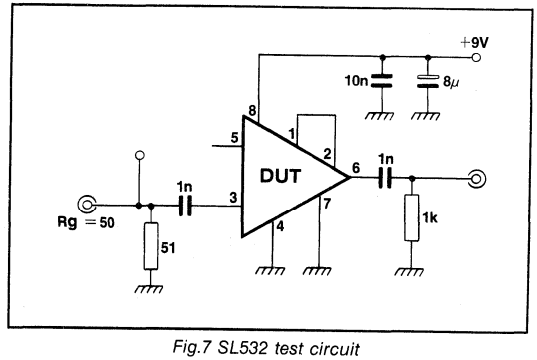


Fig.7 SL532 test circuit

PLESSEY
Semiconductors

SL541B

HIGH SLEW RATE OPERATIONAL AMPLIFIER

The SL541 is a monolithic amplifier designed for optimum pulse response and applications requiring high slew rate with fast settling time to high accuracy. The high open loop gain is stable with temperature, allowing the desired closed loop gain to be achieved using standard operational amplifier techniques. The device has been designed for optimum response at a gain of 20dB when no compensation is required. The SL541B has a guaranteed input offset voltage of ±5mV maximum and replaces the SL541C.

The SL541B is tested in two circuit applications (A and B).

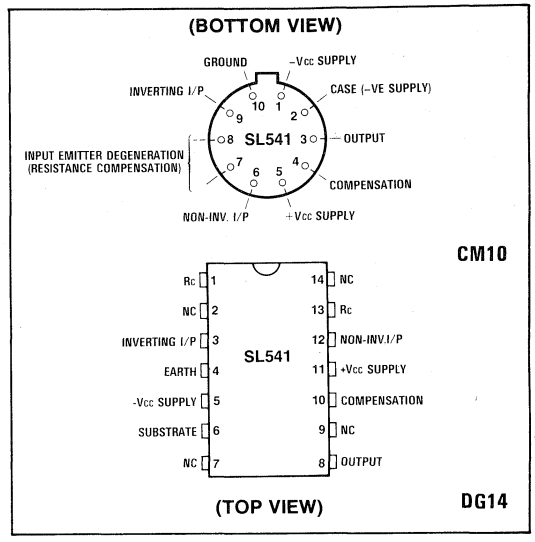


Fig. 1 Pin connections

FEATURES

- High Slew Rate: 175V/μs
- Fast Settling Time: 1% in 50ns
- Open Loop Gain: 70dB (SL541B)
- Wide Bandwidth: DC to 100MHz at 10dB Gain
- Very Low Thermal Drift: 0.02dB/°C Temperature Coefficient of Gain
- Guaranteed 5mV input offset maximum
- Full Military Temperature Range (DIL Only)

Package: 10 Lead TO-5
14 Lead DIL Ceramic

APPLICATIONS

- Wideband IF Amplification
- Wideband Video Amplification
- Fast Settling Pulse Amplifiers
- High Speed Integrators
- D/A and A/D Conversion
- Fast Multiplier Preamps

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V+ to V−)	24V
Input voltage (Inv. I/P to non inv. I/P)	±9V
Storage temperature	−55°C to +175°C
Chip operating temperature	+175°C
Operating temperature:	TO-5: −55°C to +85°C
	DIL: −55°C to +125°C

Thermal resistances

Chip-to-ambient:	TO-5	220°C/W
	DIL	125°C/W
Chip-to-case:	TO-5	60°C/W
	DIL	40°C/W

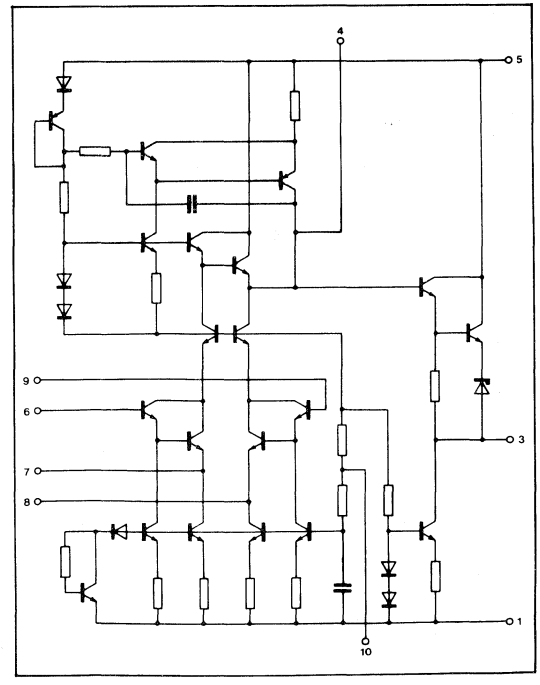


Fig. 2 SL541 circuit diagram (TO-5 pin nos.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C
R_C = 0Ω
Test circuits: see Fig.8

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current	A,B		16	21	mA	
Input bias current	A,B		7	25	μA	
Input offset voltage	A,B			5	mV	
Dynamic open loop gain	A	45	54		dB	600Ω load
	B	60	71		dB	
Open loop temperature coefficient	A,B		-0.02		dB/° C	
Closed loop bandwidth (-3dB)	A,B		100		MHz	X10 gain
Slew rate (4V peak)	A,B	100	175		V/μs	X10 gain
Settling time to 1 %	A,B		50	100	ns	
Maximum output voltage						
(+ve)	A	5.5	5.7		V	
(-ve)	A		-1.9	-1.5	V	
(+ve)	B	2.5	3.0		V	
(-ve)	B		-3.0	-2.5	V	
Maximum output current	A,B	4	6.5		mA	
Maximum input voltage						
(+ve)	A			5	V	
(-ve)	A	-1			V	Non-inverting
(+ve)	B			3	V	modes
(-ve)	B	-3			V	
Supply line rejection						
(+ve)	A,B	54	66		dB	
(-ve)	A,B	46	54		dB	
Input offset current	A,B			9.85	μA	
Common mode rejection	A,B	60.7			dB	
Input offset voltage drift	A		25		μV/° C	

ELECTRICAL CHARACTERISTICS (Typical)

Test conditions (unless otherwise stated):

T_{amb} = -55° C to +85° C (TO5)
T_{amb} = -55° C to +125° C (DIL only)
R_C = 0Ω, Test circuit B

Characteristic		Value			Units	Conditions
		Min.	Typ.	Max.		
Static nominal supply current			16	25	mA	
Input bias current				35	μA	
Input offset voltage	(+ve)			8	mV	
	(-ve)	-8			mV	
Maximum output current		3.5	6.5		mA	
Maximum input voltage	(+ve)			3	V	Non-inverting modes
	(-ve)	-3			V	
Supply line rejection	(+ve)	50			dB	
	(-ve)	42			dB	
Maximum output voltage	(+ve)	2.3			V	
	(-ve)			-2.5	V	
Common mode rejection		55			dB	
Input offset current				16	μA	
Output voltage drift			15		μV/° C	
Input bias current drift			60		nA/° C	
Output current drift			40		nA/° C	

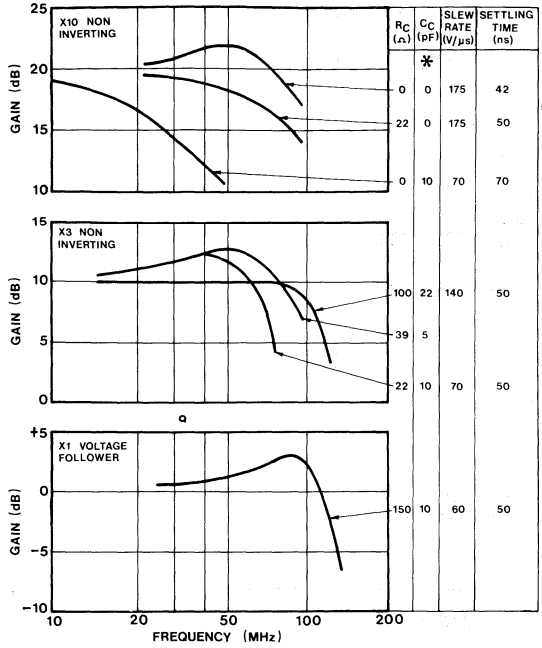


*Fig. 3 Performance graphs – gain v. frequency (load = 2kΩ/10pF) * See operating note 2*

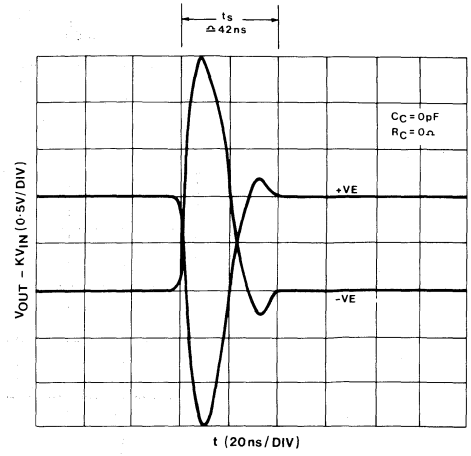


Fig.5 Settling time - X10 non-inverting mode

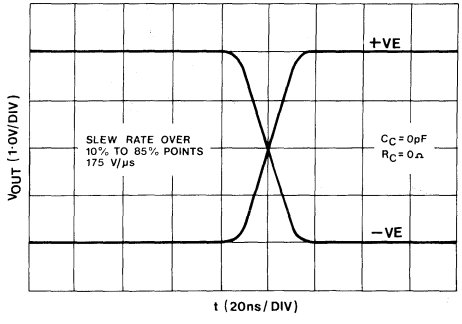


Fig.4 Slew rate - X10 non-inverting mode Input square wave 0.4V p/p

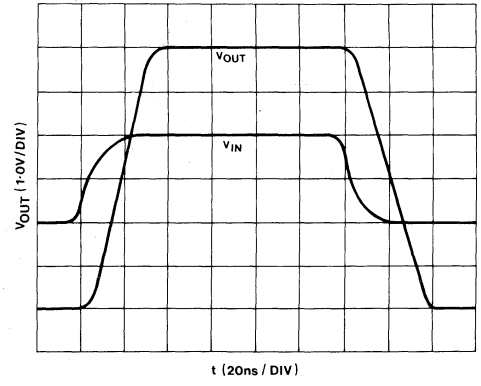


Fig.6 Output clipping levels - X10 non-inverting mode Input moderately overdriven, so that output goes into clipping both sides

OPERATING NOTES

The SL541 may be used as a normal, but non saturating operational amplifier, in any of the usual configurations (amplifiers, integrators etc.), provided that the following points are observed:

1. Positive supply line decoupling back to the output load earth should always be provided close to the device terminals.
2. Compensation capacitors should be connected between pins 4 and 5. These may have any value greater than that necessary for stability without causing side offsets.
3. The circuit is generally intended to be fed from a fairly low impedance (<1kΩ), as seen from pins 6 and 9 – 100Ω or less results in optimum speed.
4. The circuit is designed to withstand a certain degree of capacitive loading (up to 20pF) with virtually no effect. However, very high capacitive loads will cause loss of speed due to the extra compensation required and asymmetric output slew rates.
5. Pin 10 does not need to be connected to zero volts except where the clipping levels need to be defined accurately w.r.t. zero. If disconnected, an extra ±0.5 volt uncertainty in the clipping levels results, but the separation remains. However, the supply line rejection is improved if pin 10 can be left open-circuit (circuit B only).

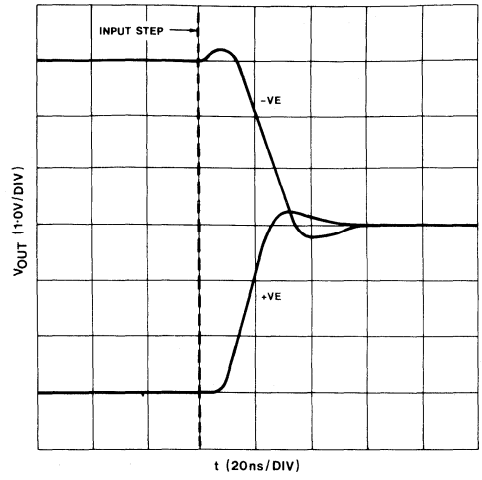


Fig.7 Output clippings levels - X10 non-inverting mode. Output goes from clipping to zero volts. V_{in} = 3V peak step, offset +ve or -ve.

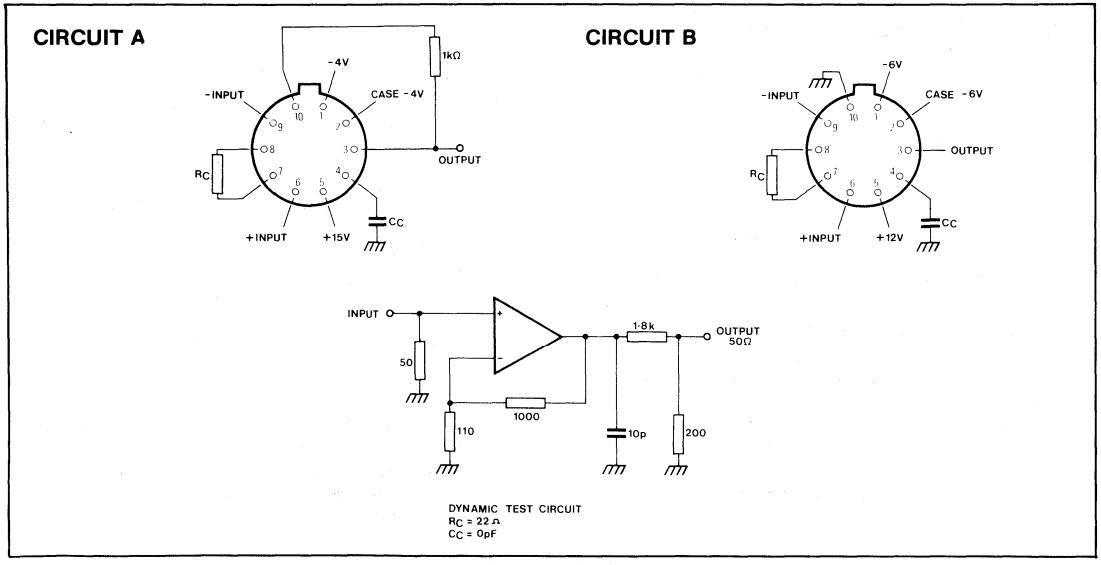


Fig. 8 Test circuits

TEST CONDITIONS AND DEFINITIONS

Both slew rate and settling time are measures of an amplifier's speed of response to an input. Slew rate is an inherent characteristic of the amplifier and is generally less subject to misinterpretation than is settling time, which is often more dependent upon the test circuit than the amplifier's ability to perform.

Slew rate defines the maximum rate of change of output voltage for a large step input change and is related to the full power frequency response (fp) by the relationship.

$$S = 2\pi f_p E_o$$

where E_o is the peak output voltage

Settling time is defined as the time elapsed from the application of a fast input step to the time when the amplifier output has entered and remained within a specified error band that is symmetrical about the final value. Settling time, therefore, is comprised of an initial propagation delay, an additional time for the amplifier to slew to the vincinity of some value of output voltage, plus a period to recover from overload and settle within the given error band.

The SL541 is tested for slew rate in a X10 gain configuration.

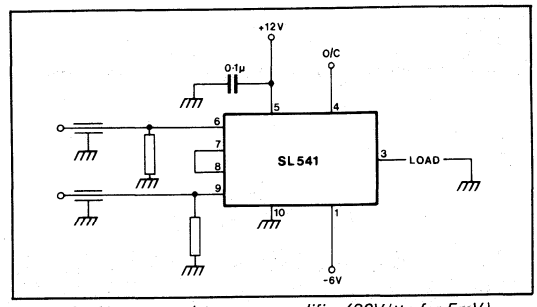


Fig. 9 Non-saturating sense amplifier (30V/µs for 5mV)
Note: the output may be caught at a pre-determined level. (TO-5 pin nos.)

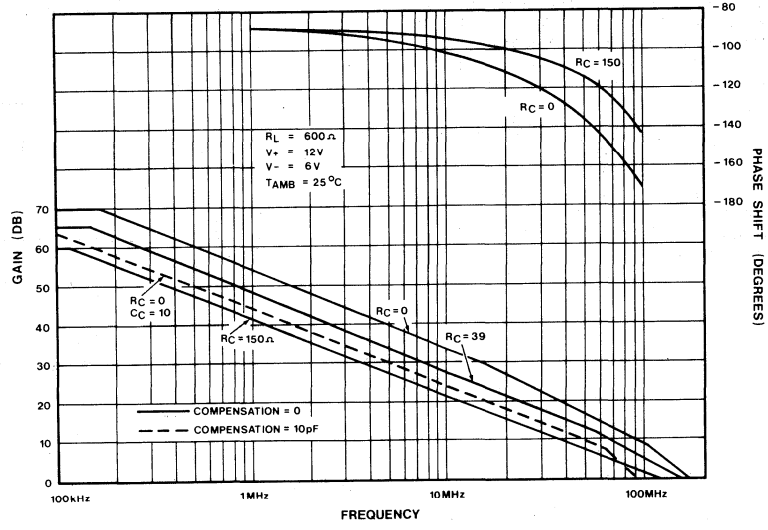


Fig.10 SL541B open loop gain and phase shift v. frequency

SL550 G

LOW NOISE WIDEBAND AMPLIFIER WITH EXTERNAL GAIN CONTROL

The SL550 is a silicon integrated circuit designed for use as a general-purpose wideband linear amplifier with remote gain control. At a frequency of 60MHz, the SL550G noise figure is 1.8dB (typ.) from a 200 ohm source, giving good noise performance directly from a microwave mixer. The SL550 has an external gain control facility which can be used to obtain a swept gain function and makes the amplifier ideal for use either in a linear IF strip or as a low noise preamplifier in a logarithmic strip.

External gain control is performed in the feedback loop of the main amplifier which is buffered on the input and output, hence the noise figure and output voltage swing are only slightly degraded as the gain is reduced. The external gain control characteristic is specified with an accuracy of ±1dB, enabling a well-defined gain versus time law to be obtained.

The input transistor can be connected in common emitter or common base and the quiescent current of the output emitter follower can be increased to enable low impedance load to be driven.

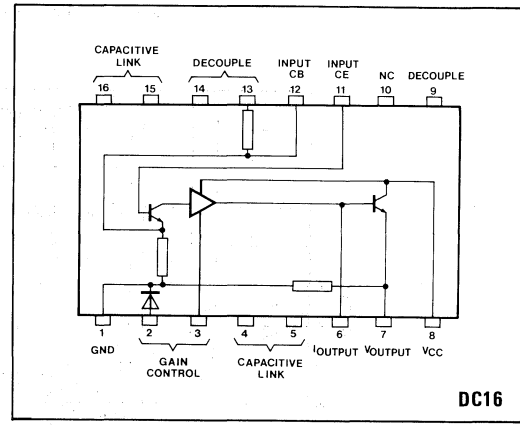


Fig. 1 Pin connections (top view)

FEATURES

- 200 MHz Bandwidth
- Low Noise Figure
- Well-Defined Gain Control Characteristic
- 25dB Gain Control Range
- 40dB Gain
- Output Voltage 0.8Vp-p (Typ.)

APPLICATIONS

- Low Noise Preamplifiers
- Swept Gain Radar IFs

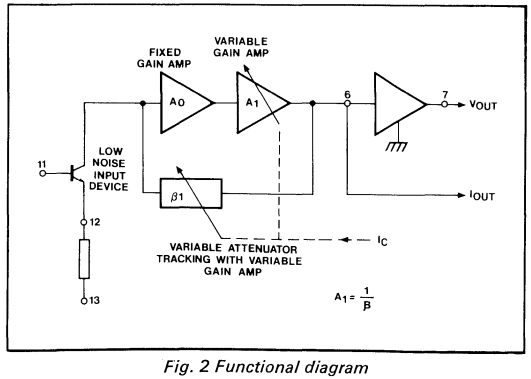


Fig. 2 Functional diagram

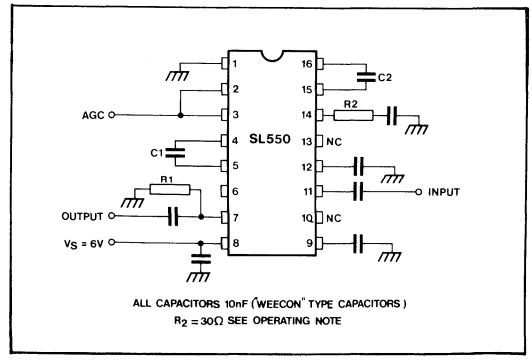


Fig. 3 Test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
f = 30MHz, V_S = +6V, R_L = 200Ω, I_C = 0, R_1 = 750Ω, T_{amb} = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	39	42	44	dB	
Gain control characteristic		See Note 1			
Gain reduction at mid-point		10		dB	I_C = 0.24mA
Max. gain reduction	20	25		dB	I_C = 2.0mA
Noise figure		2.0	2.7	dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Output voltage		0.15		Vrms	R_1 = ∞
		0.3		Vrms	R_1 = 750Ω
Supply current		11	13	mA	R_1 = ∞
		15		mA	R_1 = 750Ω
Gain variation with supply voltage		0.2		dB/V	V_S = 6V to 9V
Upper cut-off frequency (-3dB w.r.t. 30MHz)		125		MHz	
Gain variation with temperature (see Note 2)		±3		dB	T_{amb} = -55°C to +125°C

NOTES
1. The external gain control characteristic is specified in terms of the gain reduction obtained when the control current (I_C) is increased from zero to the specified current.
2. This can be reduced by using an alternative input configuration (see operating note: 'Wide Temperature Range').

OPERATING NOTES

Input Impedance

The input capacitance, which is typically 12pF at 60MHz, is independent of frequency. The input resistance, which is approximately 1.5k at 10MHz, decreases with frequency and is typically 500 ohms at 60MHz.

Control Input

Gain control is normally achieved by a current into pin 2. Between pin 2 and ground is a forward biased diode and so the voltage on pin 2 will vary between 600 mV at I_C = 1μA to 800 mV at I_C = 2 mA. The amplifier gain is varied by applying a voltage in this range to pin 3. To avoid problems associated with the sensitivity of the control voltage and with operation over a wide temperature range the diode should be used to convert a control current to a voltage which is applied to pin 3 by linking pins 2 and 3.

Minimum Supply Current

If the full output swing is not required, or if high impedance loads are being driven, the current consumption can be reduced by omitting R_1 (Fig. 3). The function of R_1 is to increase the quiescent current of the output emitter follower.

High Output Impedance

A high impedance current output can be obtained by taking the output from pin 6 (leaving pin 7 open-circuit). Maximum output current is 2 mA peak and the output impedance is 350Ω.

Wide Temperature Range

The gain variation with temperature can be reduced at the expense of noise figure by including an internal 30Ω resistor in the emitter of the input transistor. This is achieved by decoupling pin 13 and leaving pin 12 open-circuit. Gain variation is reduced from ±3dB to ±1dB over the temperature range —55°C to +125°C (Figs. 6 and 7).

Low Input Impedance

A low input impedance (≃25Ω) can be obtained by connecting the input transistor in common base. This is achieved by decoupling pin 11 and applying the input to pin 12 (pin 13 open-circuit).

High Frequency Stability

Care must be taken to keep all capacitor leads short and a ground plane should be used to prevent any earth inductance common between the input and output circuits. The 30Ω resistor (pin 14) shown in the test circuit eliminates high frequency instabilities due to the stray capacitances and inductances which are unavoidable in a plug-in test system. If the amplifier is soldered directly into a printed circuit board then the 30Ω resistor can be reduced or omitted completely.

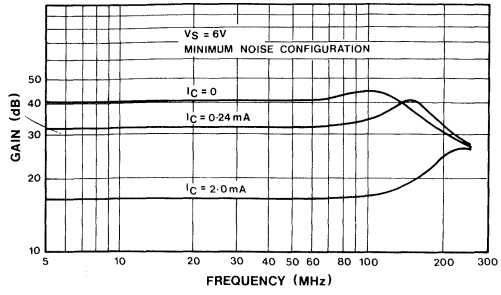


Fig. 4 Frequency response

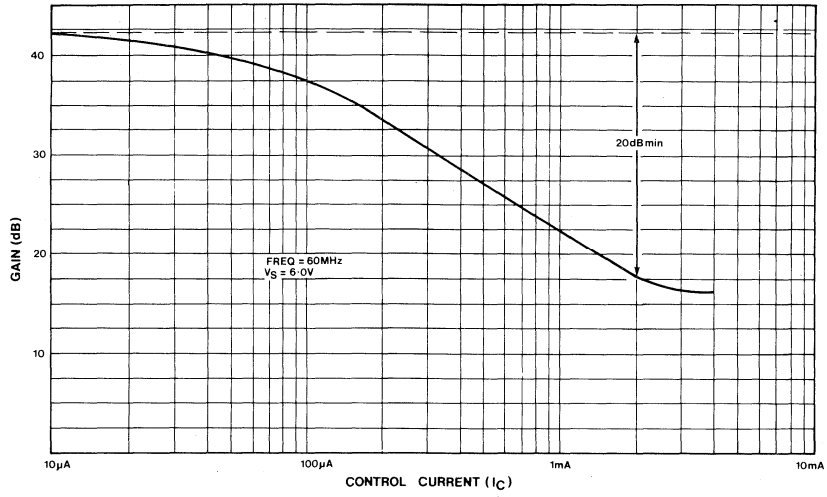


Fig. 5 Gain control characteristic

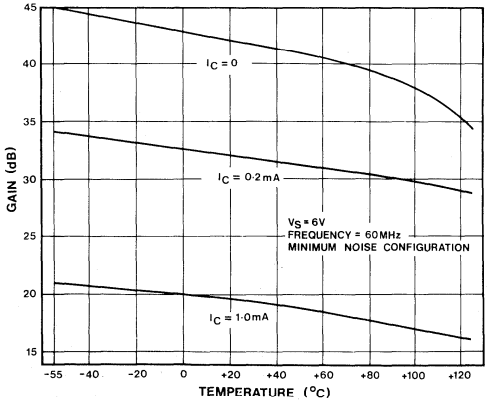


Fig. 6 Voltage gain v. temperature (pin 12 decoupled, standard circuit configuration)

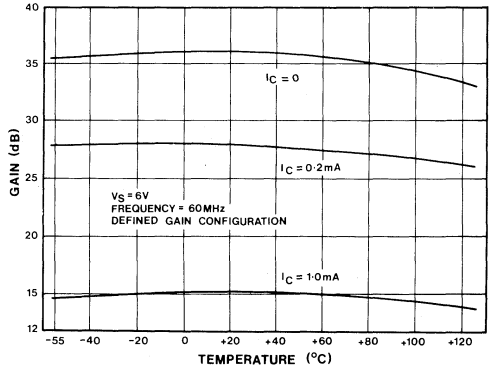


Fig. 7 Voltage gain v. temperature (pin 13 decoupled for improved gain variation with temperature – see operating notes)

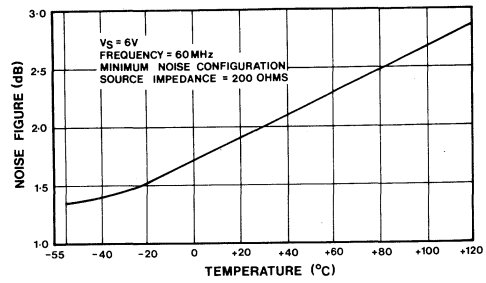


Fig. 8 Typical noise figure

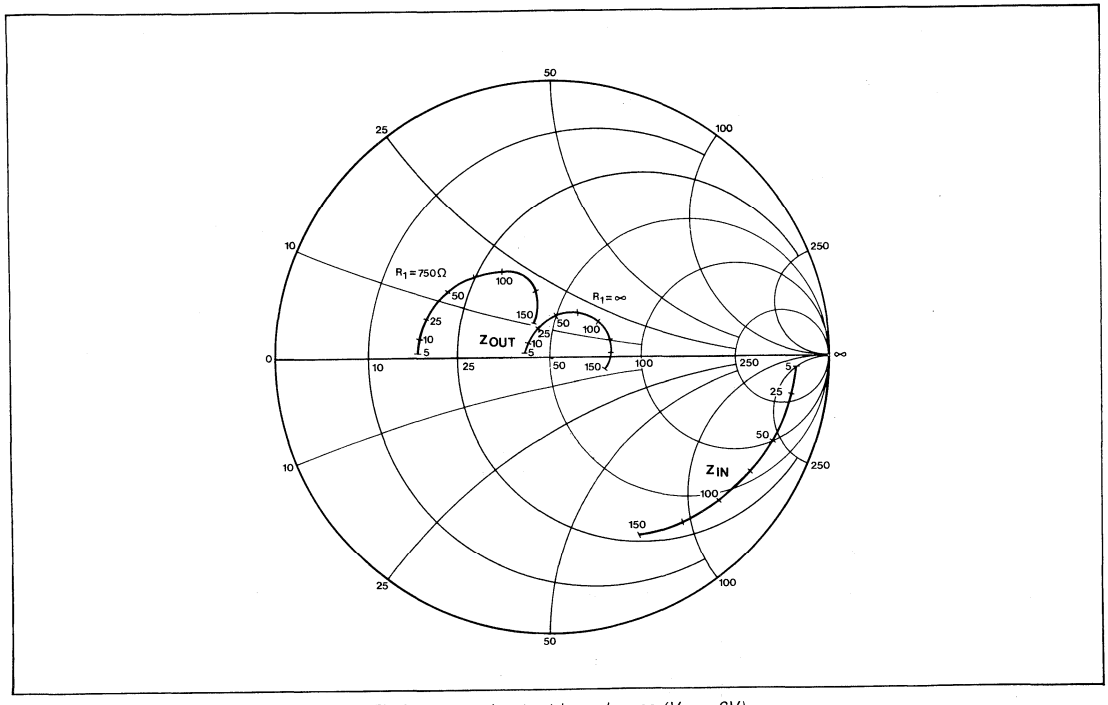


Fig.9 Input and output impedances (Vs = 6V)

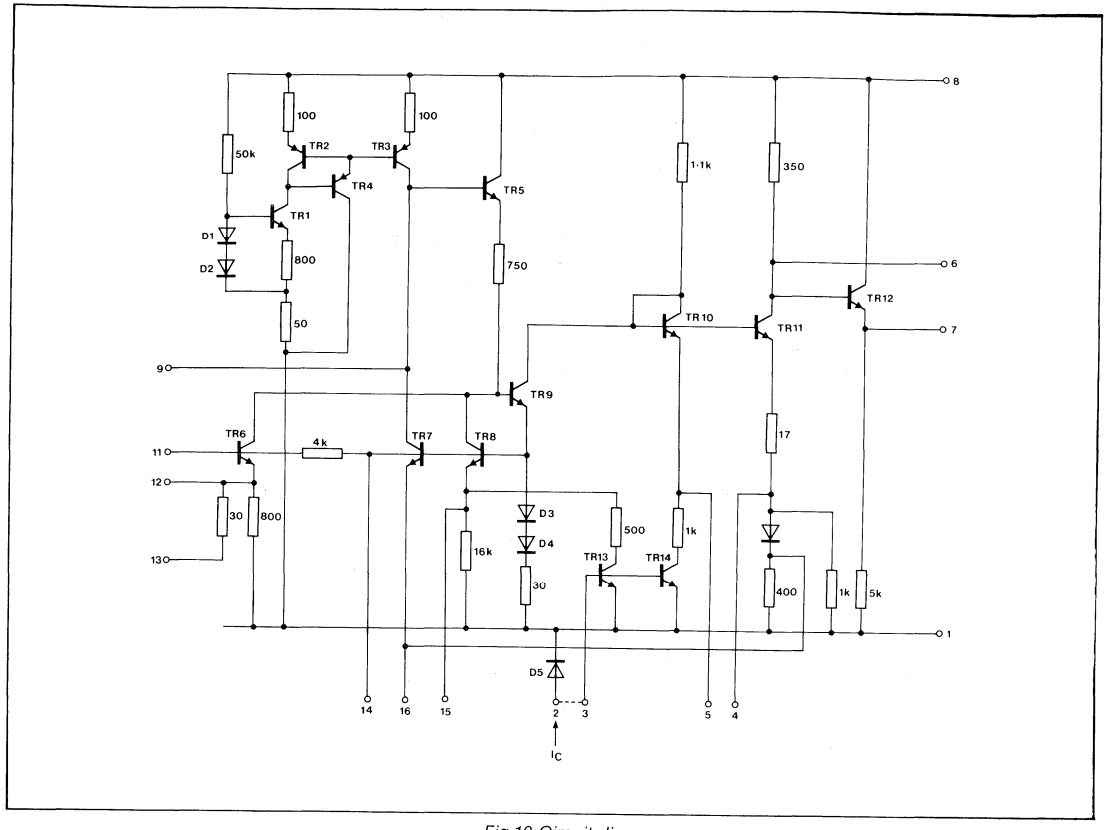


Fig.10 Circuit diagram

APPLICATION NOTES

A wideband high gain configuration using two SL550s connected in series is shown in Fig. 11. The first stage is connected in common emitter configuration, whilst the second stage is a common base circuit. Stable gains of up to 65 dB can be achieved by the proper choice of R1 and R2. The bandwidth is 5 to 130 MHz, with a noise figure only marginally greater than the 2.0 dB specified for a single stage circuit.

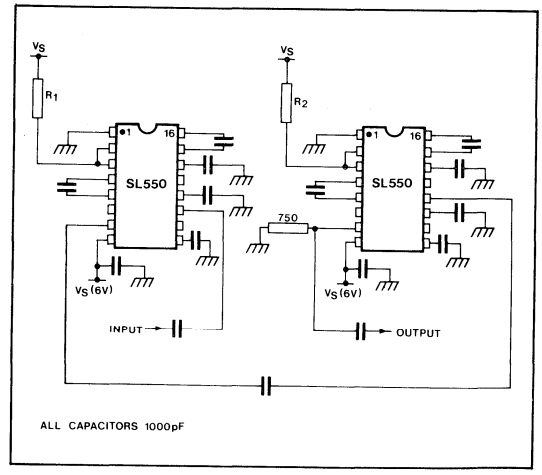


Fig. 11 A two-stage wide-band amplifier

A voltage gain control which is linear with control voltage can be obtained using the circuit shown in Fig. 12. The input is a voltage ramp which is negative going with respect to ground. The output drives the control current pins 2 and 3 directly (see Fig. 13). If two SL550s in the strip are controlled as shown in Fig. 14, with a linear ramp input to the linearising circuit, a fourth power law (power gain v. time) will be obtained over a 50 dB dynamic range.

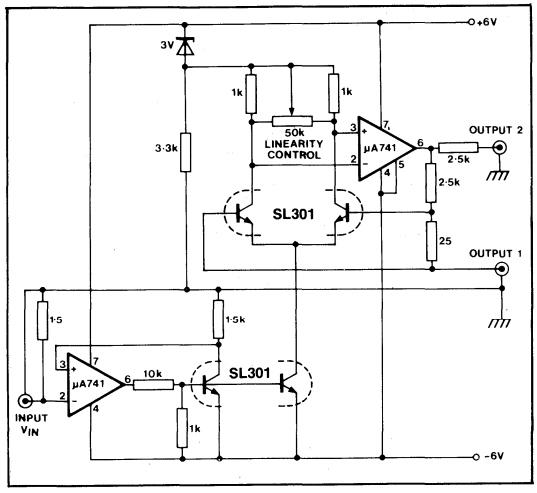


Fig. 12 Gain control linearising circuit

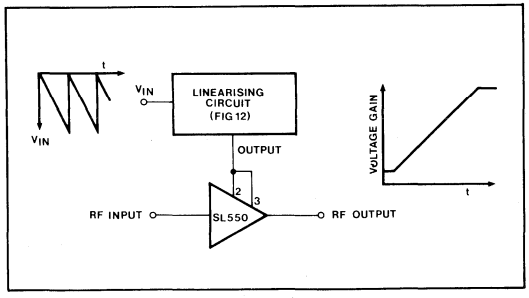


Fig. 13 Linear swept gain circuit

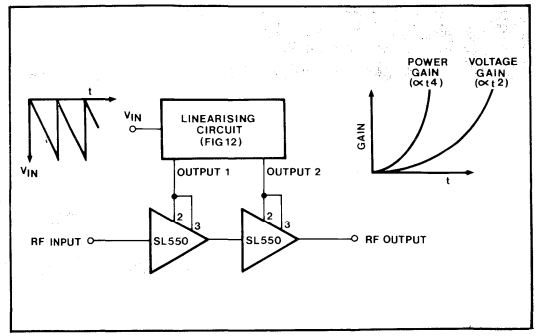
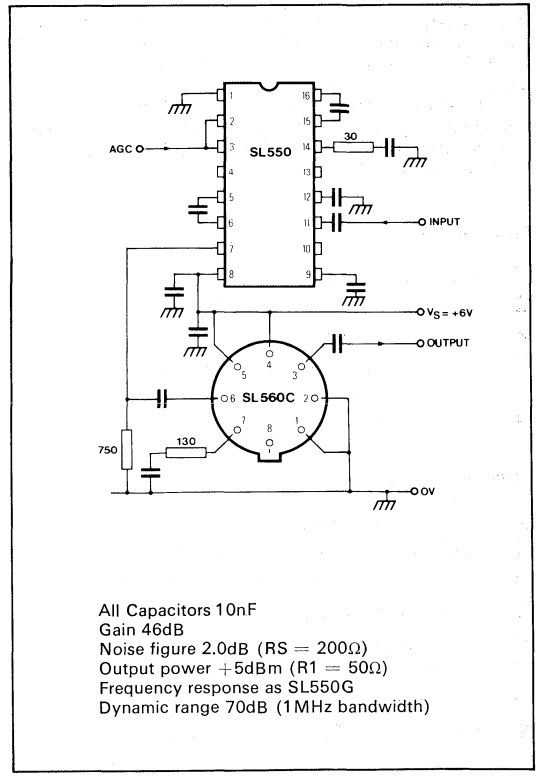


Fig. 14 Square law swept gain circuit



All Capacitors 10nF
Gain 46dB
Noise figure 2.0dB (RS = 200Ω)
Output power +5dBm (R1 = 50Ω)
Frequency response as SL550G
Dynamic range 70dB (1MHz bandwidth)

Fig. 15 Applications example of wide dynamic range: 50Ω load amplifier with AGC using SL500 series integrated circuit.

ABSOLUTE MAXIMUM RATINGS

Storage temperature	—55°C to +150°C
Ambient operating temp.	—40°C to +125°C
Max. continuous supply Voltage wrt pin 1	+9V
Max. continuous AGC current	
pin 2	10mA
pin 3	1mA

SL560C

300MHz LOW NOISE AMPLIFIER

This monolithic integrated circuit contains three very high performance transistors and associated biasing components in an eight-lead TO-5 package forming a 300MHz low noise amplifier. The configuration employed permits maximum flexibility with minimum use of external components. The SL560C is a general purpose low noise, high frequency gain block.

The device is also available as the SL560AC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

FEATURES

- Gain up to 40dB
- Noise Figure less than 2dB (Rs 200 ohm)
- Bandwidth 300MHz
- Supply Voltage 2-15V (Depending on Configuration)
- Low Power Consumption

APPLICATIONS

- Radar IF Preamplifiers
- Infra-Red Systems Head Amplifiers
- Amplifiers in Noise Measurement Systems
- Low Power Wideband Amplifiers
- Instrumentation Preamplifiers
- 50 ohm Line Drivers
- Wideband Power Amplifiers
- Wide Dynamic Range IF Amplifiers
- Aerial Preamplifiers for VHF TV and FM Radio

ABSOLUTE MAXIMUM RATINGS

Supply voltage (Pin 4)	+15V
Storage temperature	-55°C to 150°C (CM) -55°C to 125°C (DP)
Junction temperature	150°C (CM) 125°C (DP)
Thermal resistance	
Junction-case	60°C/W (CM)
Junction ambient	220°C/W (CM) 230°C/W (DP)
Maximum power dissipation	See Fig.15
Operating temperature range	-55°C to +125°C (CM) at 100mW -55°C to +100°C (DP) at 100mW

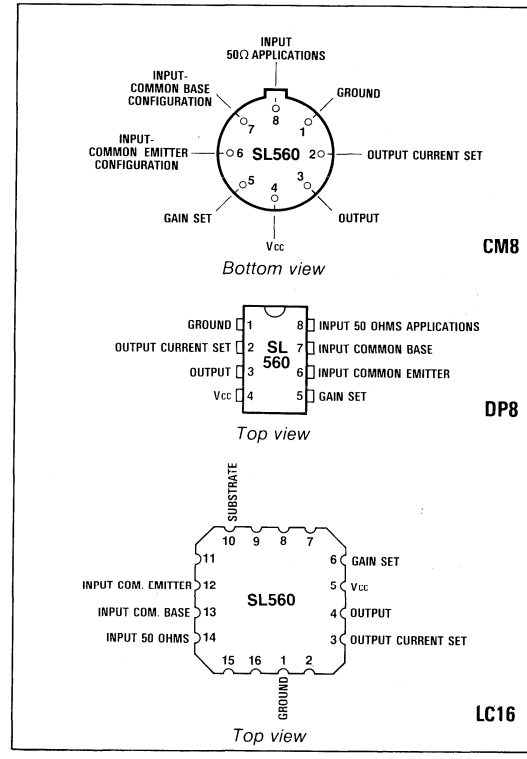


Fig.1 Pin connections

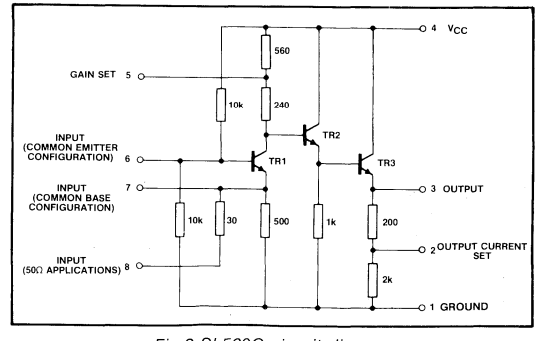


Fig.2 SL560C circuit diagram

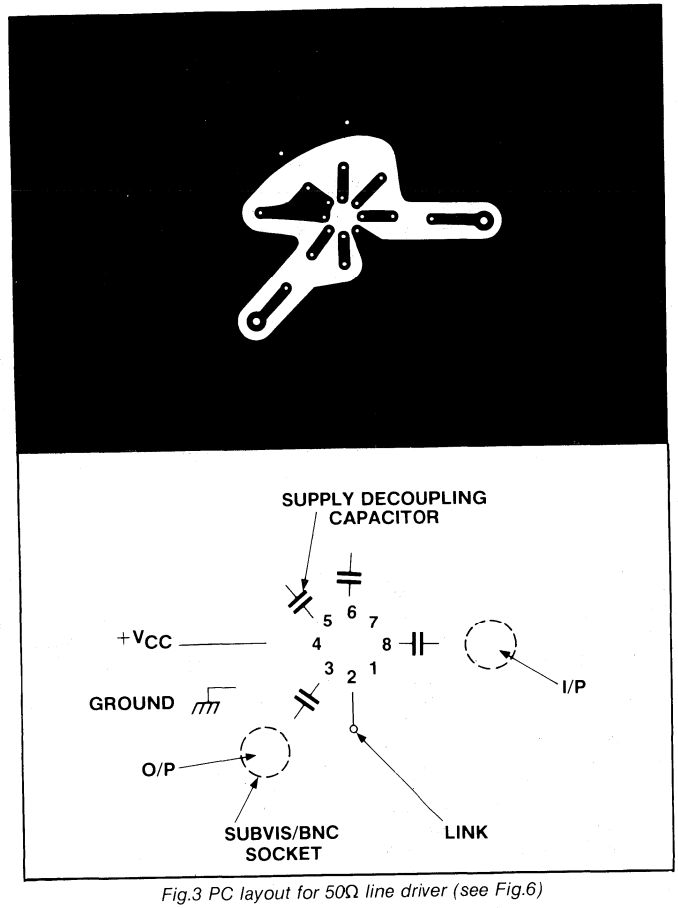


Fig.3 PC layout for 50Ω line driver (see Fig.6)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Frequency = 30MHz; V_{CC} = 6V; R_S = R_L = 50Ω; T_{amb} = 25°C; Test Circuit: Fig.6

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Small signal voltage gain	11	14	17	dB	
Gain flatness		±1.5		dB	10MHz - 220MHz
Upper cut-off frequency		250		MHz	
Output swing	+5	+7		dBm	V_{CC} 6V } See Fig.5
		+11		dBm	V_{CC} = 9V }
Noise figure (common emitter)		1.8		dB	R_S = 200Ω
		3.5		dB	R_S = 50Ω
Supply current		20	30	mA	

CIRCUIT DESCRIPTION

Three high performance transistors of identical geometry are employed. Advanced design and processing techniques enable these devices to combine a low base resistance ($R_{bb'}$) of 17Ω (for low noise operation) with a small physical size - giving a transition frequency, f_T, in excess of 1GHz.

The input transistor (TR1) is normally operated in common base, giving a well defined low input impedance. The full voltage gain is produced by this transistor and the output voltage produced at its collector is buffered by the two emitter followers (TR2 and TR3). To obtain maximum bandwidth the capacitance at the collector of TR1 must be minimised. Hence, to avoid bonding pad and can capacitances, this point is not brought out of the package. The collector load resistance of TR1 is split, the tapping being accessible via pin 5. If required, an external roll-off capacitor can be fixed to this point.

The large number of circuit nodes accessible from the outside of the package affords great flexibility, enabling the operating currents and circuit configuration to be optimised for any application. In particular, the input transistor (TR1) can be operated in common emitter mode by decoupling pin 7 and using 6 as the input. In this configuration, a 2dB noise figure (R_S = 200Ω) can be achieved. This configuration can give a gain of 35dB with a bandwidth of 75MHz (see Figs. 8 and 9) or, using feedback 14dB with a bandwidth of 300MHz (see Figs. 10 and 11).

Because the transistors used in the SL560C exhibit a high value of f_T, care must be taken to avoid high frequency instability. Capacitors of small physical size should be used, the leads of which must be as short as possible to avoid oscillation brought about by stray inductance. The use of a ground plane is recommended.

Further applications information is available in the 'Broadband Amplifier Applications' booklet.

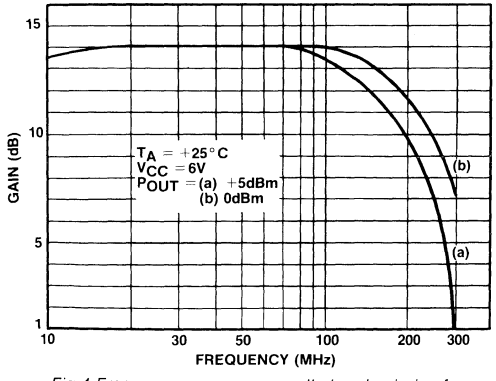


Fig.4 Frequency response, small signal gain is of a typical device

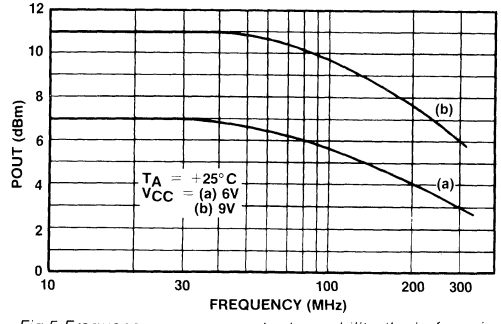


Fig.5 Frequency response, output capability (loci of maximum output power with frequency, for 1dB gain compression (typical)

TYPICAL APPLICATIONS

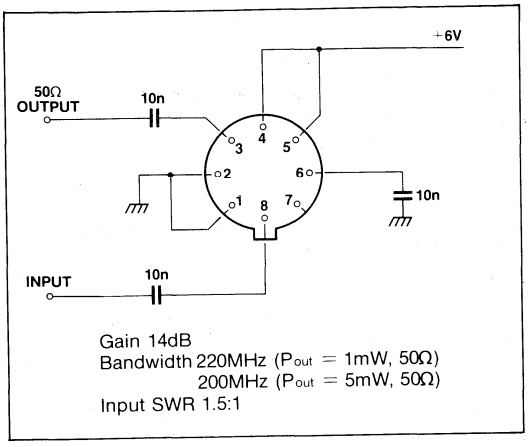


Fig.6 50Ω line driver. The response of this configuration is shown in Fig.4.

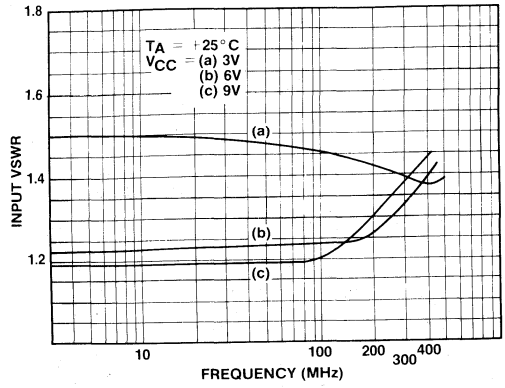


Fig.7 Input standing wave ratio plot of circuit shown in Fig.6 (typical)

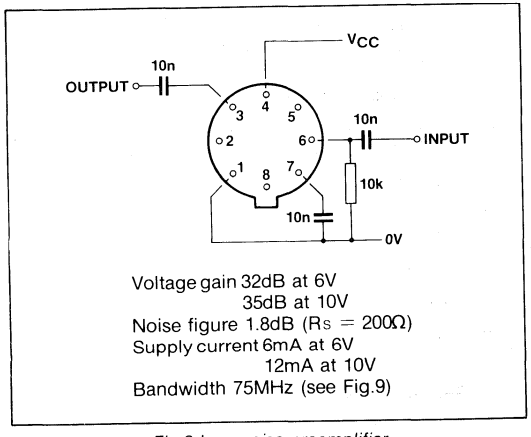


Fig.8 Low noise preamplifier

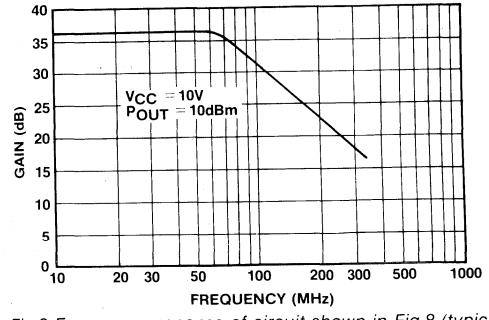


Fig.9 Frequency response of circuit shown in Fig.8 (typical)

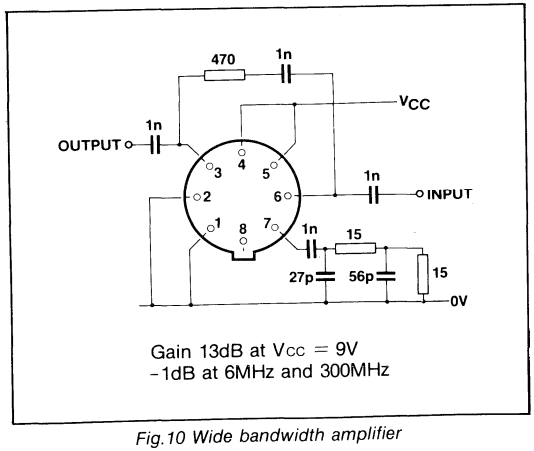


Fig.10 Wide bandwidth amplifier

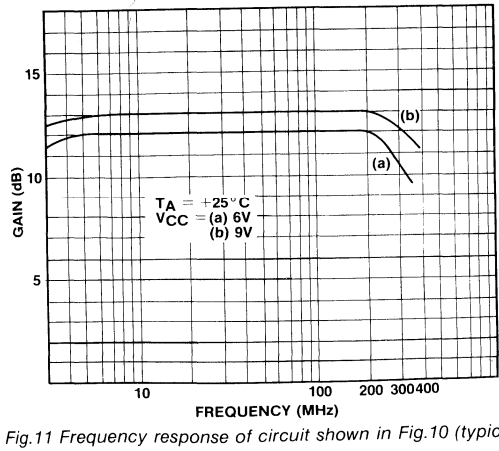


Fig.11 Frequency response of circuit shown in Fig.10 (typical)

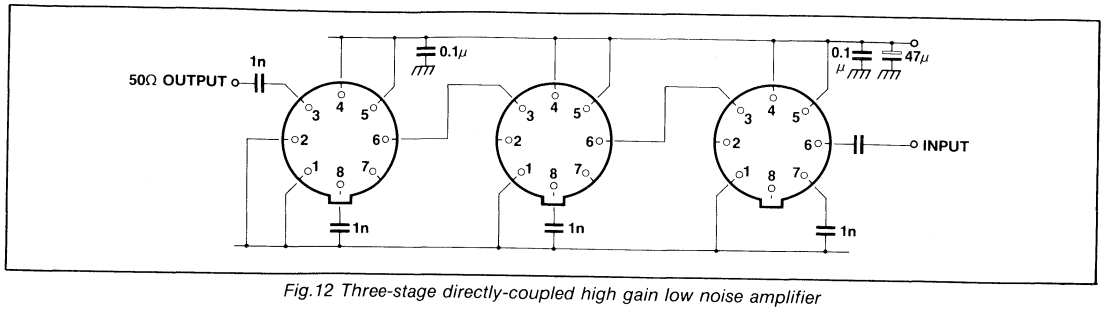


Fig.12 Three-stage directly-coupled high gain low noise amplifier

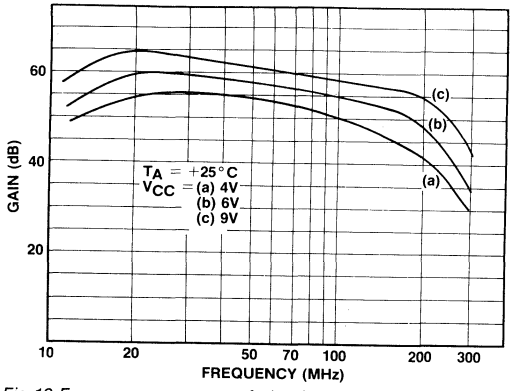


Fig.13 Frequency response of circuit shown in Fig.12 (typical)

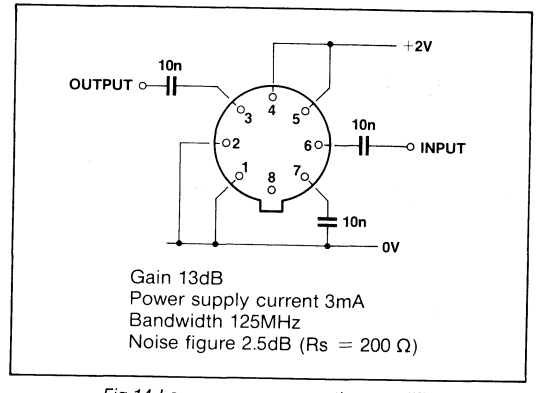


Fig.14 Low power consumption amplifier

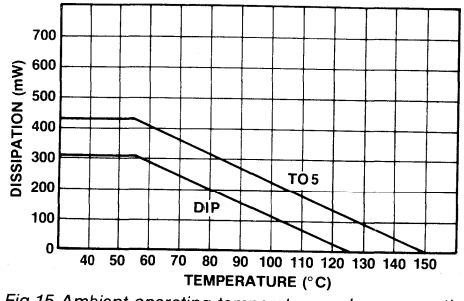


Fig.15 Ambient operating temperature v. degrees centigrade (typical)

SL561B, SL561C

ULTRA LOW NOISE PREAMPLIFIERS

This integrated circuit is a high gain, low noise preamplifier designed for use in audio and video systems at frequencies up to 6MHz. Operation at low frequencies is eased by the small size of the external components and the low 1/f noise. Noise performance is optimised for source impedances between 200Ω and 1kΩ making the device suitable for use with a number of transducers including photo-conductive IR detectors, magnetic tape heads and dynamic microphones.

The SL561B is only available in the TO-5 package.

The SL561C is only available in the Plastic package.

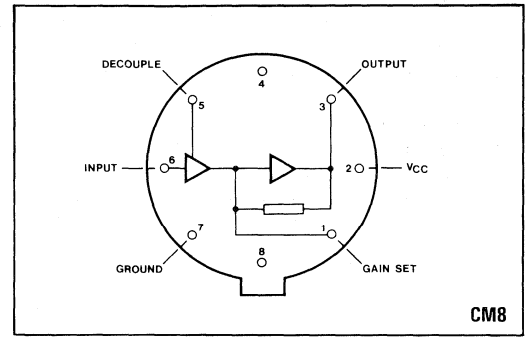


Fig.1 Pin connections (viewed from above) SL561B

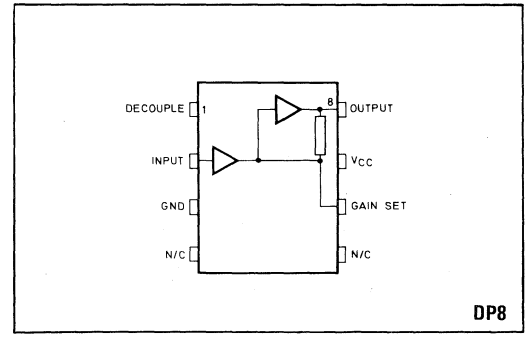


Fig.2 Pin connections (viewed from above) SL561C

FEATURES

■ High Gain	60dB
■ Low noise	0.8nV/√Hz (Rs = 50Ω)
■ Bandwidth	6MHz
■ Low Power Consumption	10mW (V_{CC} = 5V)

APPLICATIONS

- Audio Preamplifiers (low noise from low impedance source)
- Video Preamplifier
- Preamplifier for use in Low Cost Infra-Red Systems

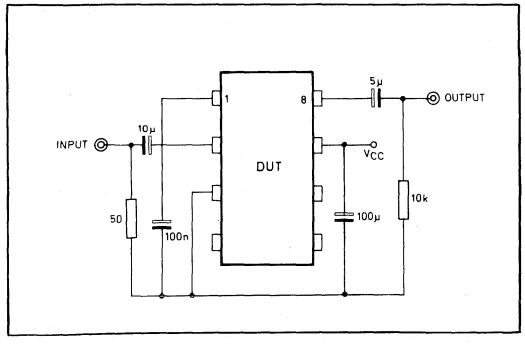


Fig.3 Test circuit

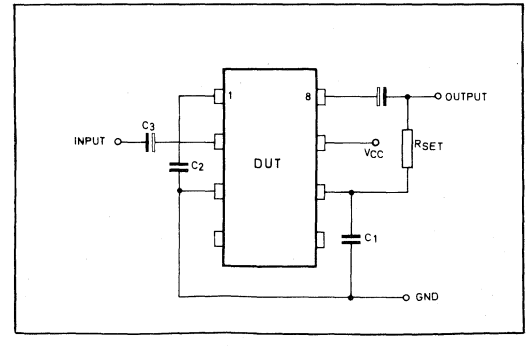


Fig.4 Typical application

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} 5V
Source impedance 50Ω
Load impedance 10kΩ
T_{amb} 25°C

SL561B

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 1 O/C
Equivalent input noise voltage		0.8	1.2	nV/√Hz	100Hz to 6MHz
Output voltage	2	3		V p-p	See note
Supply current		2.0	3.0	mA	
Output resistance		50		Ω	
Input resistance		3		kΩ	
Input capacitance		15		pF	
Upper cut-off frequency	5	6.5		MHz	V_{out} = 10mV p-p
		6.2		MHz	V_{out} = 1.5V p-p

SL561C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	57	60	63	dB	Pin 6 O/C
Equivalent input noise voltage		0.8		nV/√Hz	100Hz to 6MHz
Input resistance		3		kΩ	
Input capacitance		15		pF	
Output impedance		50		Ω	
Output voltage	2	3		V p-p	See note
Supply current		2	3	mA	
Bandwidth		6		MHz	

OPERATING NOTES (Pin numbers refer to DIL package)

Upper cut-off Frequency

The bandwidth of the amplifier can be reduced from 6MHz to any desired value by a capacitor from pin 6 to ground. This is shown in Fig.5. No degradation in noise or output swing occurs when this capacitor is used. The high frequency roll off is approximately 6dB/octave.

Low frequency response

The capacitors C_2 and C_3 (Fig.4) determine the lower cut-off frequency. C_2 decouples an internal feedback loop and if its value is close to that of C_3 an increase in gain at low frequencies can occur. For a flat response either make C_2 less than 0.05 C_3 or make C_2 greater than 5 C_3.

Gain set facility

Provision is made to adjust the gain by means of a resistor between pin 6 and the output. Gains as low as 10dB can be selected. This resistor increases the feedback around the output stage and stability problems can result if the bandwidth of the amplifier is not reduced as indicated in Note 1. Fig.6 shows recommended values of C_1 for each gain range. Since the input stage is a common emitter stage without emitter degeneration (for best noise) at values of gain less than 40dB this input stage, rather than the output stage, determines the maximum output voltage swing. For a distortion of less than 10% the input voltage should be restricted to less than 5mV (see Fig.9).

Driving low impedance loads

The quiescent current of the output emitter follower is 0.5mA. If larger voltage swings are required into low impedance loads this current can be increased by a resistor from pin 8 to ground. To avoid exceeding the ratings of the output transistor the resistor should not be less than 200Ω.

Noise performance

The equivalent input voltage for the amplifier is shown in Fig.7 From this the input noise voltage and current generators can be derived. They are:

$e_n = 0.8nV/\sqrt{Hz}$
$i_n = 2.0pA/\sqrt{Hz}$

Flicker or 1/f noise is not normally a problem, the knee frequency being typically below 100Hz.

ABSOLUTE MAXIMUM RATINGS

Supply voltage	10V
Storage temperature range	-55°C to +125°C
Operating temperature range DIL	-55°C to +100°C
Operating temperature range TO5	-55°C to +125°C

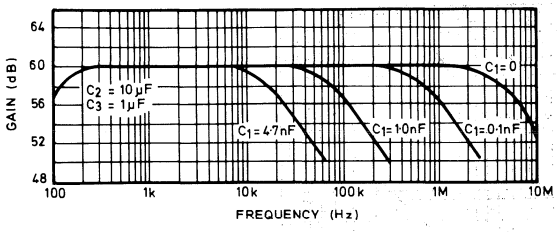


Fig.5 Gain v. frequency

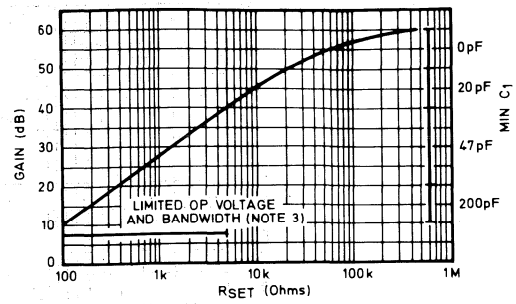


Fig.6 Gain v. R_{set}

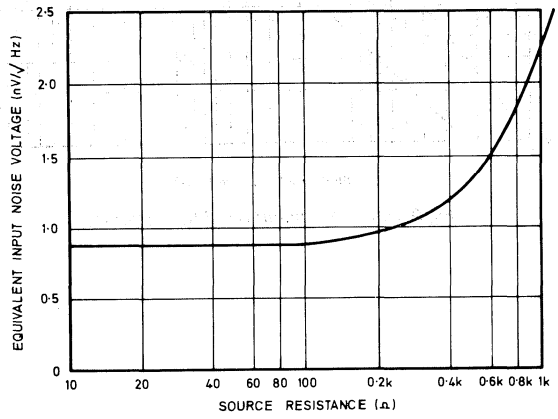


Fig.7 Noise v. source impedance

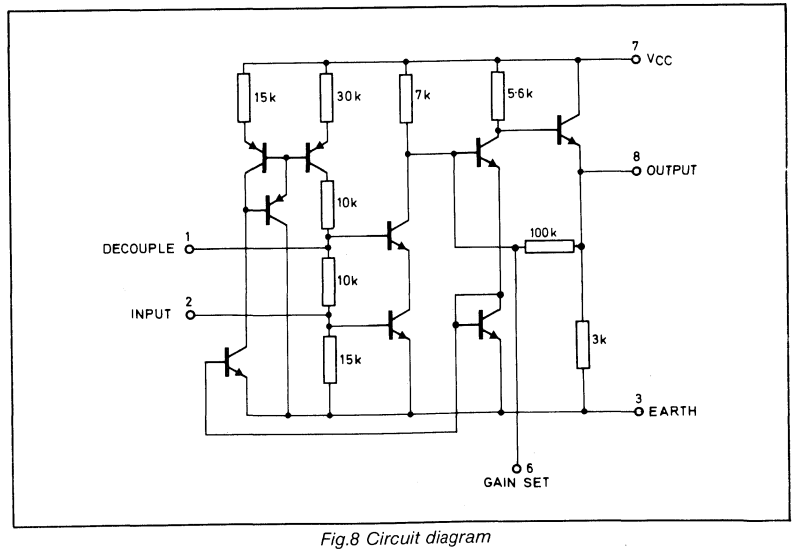


Fig.8 Circuit diagram

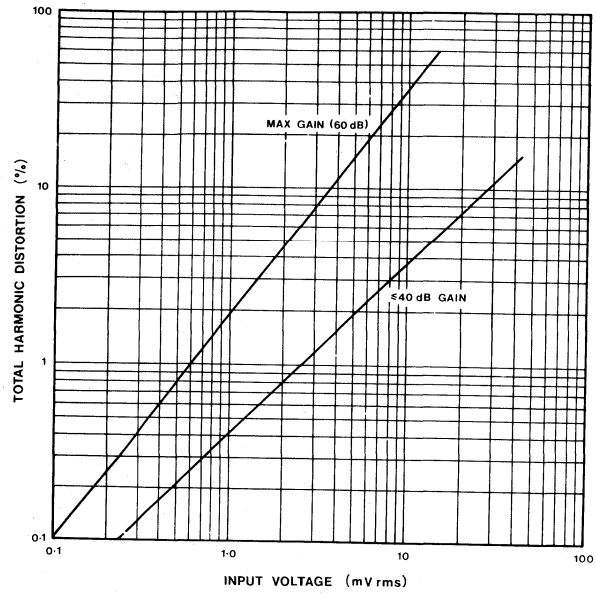


Fig.9 Harmonic distortion SL561 at 20kHz

PLESSEY
Semiconductors

SL562

LOW NOISE PROGRAMMABLE OPERATIONAL AMPLIFIER

The SL562 is an advanced bipolar integrated circuit containing a single programmable operational amplifier. The amplifier can be programmed by current into a bias pin which determines the main characteristics of the amplifier's, supply current, frequency response and slew rate. With a suitable choice of bias current the SL562 can be used where low power and low noise characteristics are a necessity.

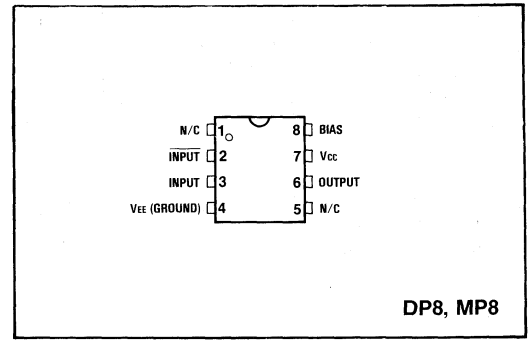


Fig.1 Pin connections - top view

FEATURES

- Low Noise Guaranteed (25nV/√Hz at 1kHz)
- Low Supply Current (40uA)
- Bias Conditions Adjustable to Optimise Performance
- Built In Short Circuit Protection
- Available In Small Outline

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers
- Frequency Synthesisers
- Hand Held Radio Applications

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±10V
- Supply Current ±40μA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

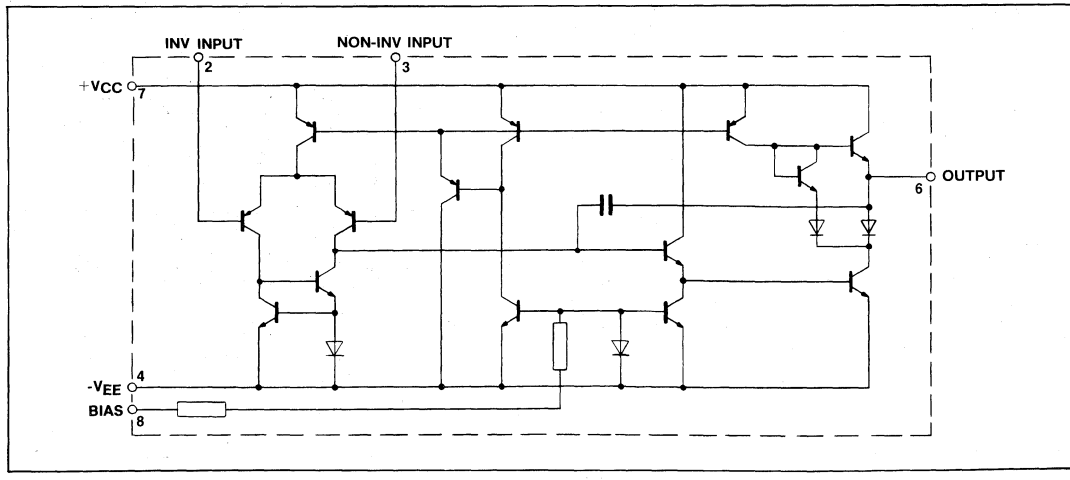


Fig.2 Circuit diagram.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25° C
Operating mode A : Supply volts ±10V Bias set current 75μA
Operating mode B : Supply volts ±3.5V Bias set current 15μA
Operating mode C : Supply volts ±1.5V Bias set current 1μA

Characteristic	Operating mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S = 10kΩ
Input offset current		20	190			150			49	nA	
Input bias current		250	800			350			95	nA	
Input resistance	0.1	0.6		0.2	0.5		0.3	2		MΩ	
Supply current	1000	1600	2200	50	200	1000	20	40	60	μA	
Large signal voltage gain	74	95		74	90		74	90		dB	R_L = 4kΩ(A) R_L = 100kΩ(B) R_L = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	R_S = 10kΩ
Common mode rejection ratio	70	110		70	85		70	82		dB	
Output voltage swing	8			1.5			0.7	0.8		±V	R_L = 4kΩ(A) R_L = 10kΩ(B) R_L = 4kΩ(C)
Supply voltage rejection ratio	74			85			85			dB	R_S = 10kΩ
Short circuit current	12		40				1	2.2		mA	T_{amb} = 0° C to +70° C
Gain bandwidth product		3.5			1			50		kHz MHz	Gain = 20dB
Slew rate		1.5			0.5			0.02		V/μs	Gain = 20dB
Input noise voltage		10	25		25	40		50	85	nV√Hz	f_O = 1kHz
Input noise current		1.6			1.6			1.0		pA√Hz	f = 1kHz

OPERATING NOTES

Bias set current

The amplifier is programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each supply)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02V/μs
	(I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{V_S - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

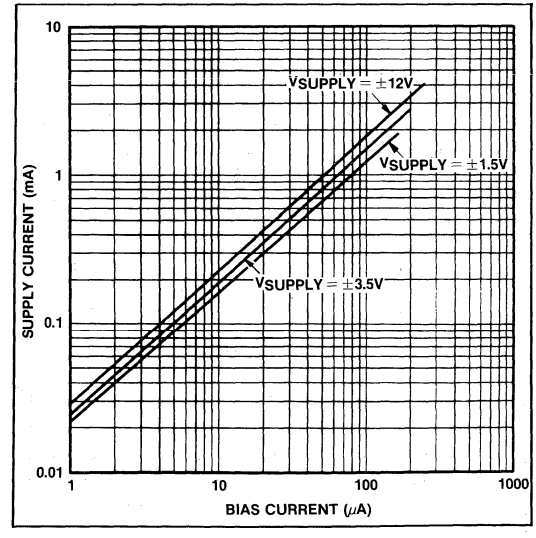


Fig.3 Supply current v. bias set current.

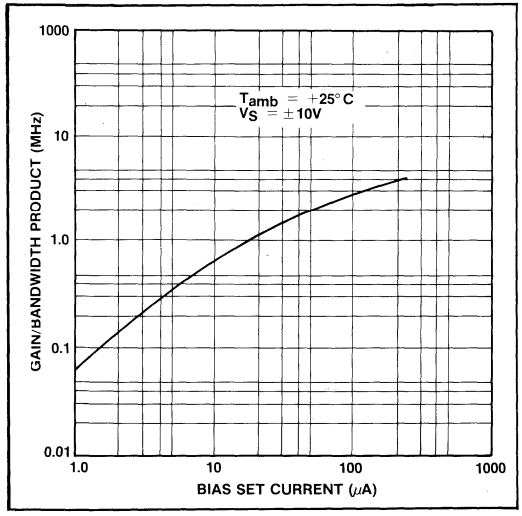


Fig.4 Gain bandwidth product v. ISET

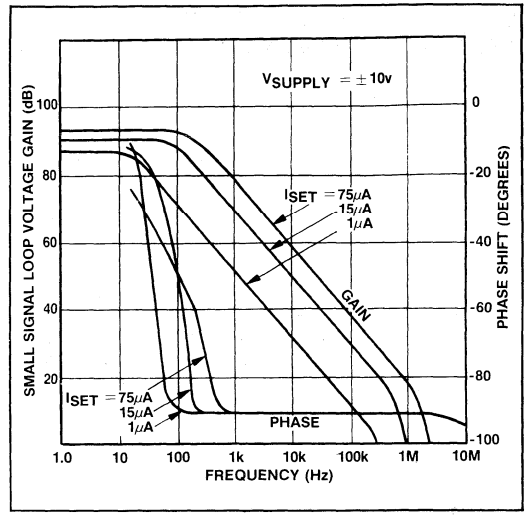


Fig. 5 Typical frequency response

APPLICATION EXAMPLE

The SL562 is especially suitable for use in loop filters for frequency synthesisers, the low noise and low power characteristics of the SL562 making it ideally suited for use with the Plessey low power frequency synthesiser circuits (NJ8820, SP87XX). All three integrated circuits are available in surface mounting packages, thus making a compact hybrid.

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

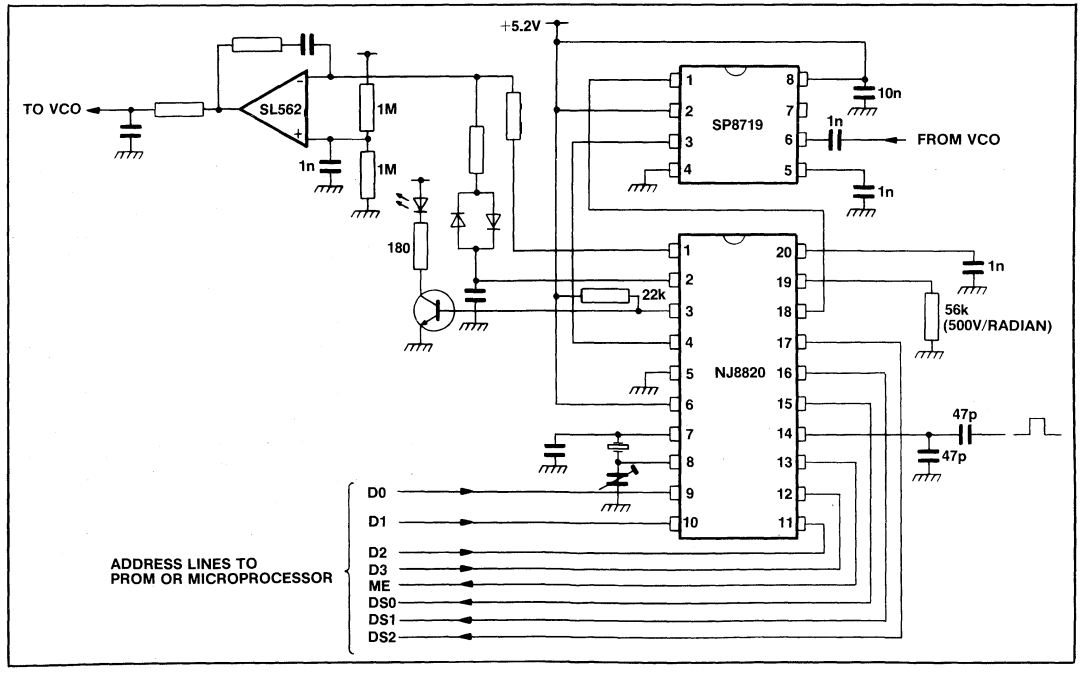


Fig.6 Application example.

SL610C, SL611C & SL612C

RF/IF AMPLIFIERS

The SL1610C, SL1611C and SL1612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15MHz to 120MHz according to type.

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

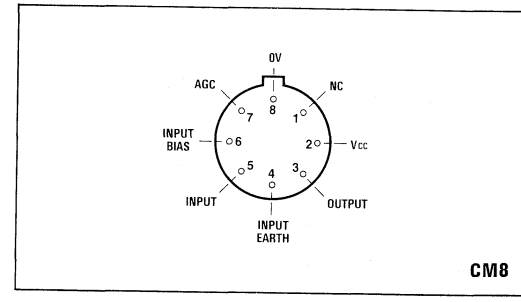


Fig. 1 Pin connections (bottom view)

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

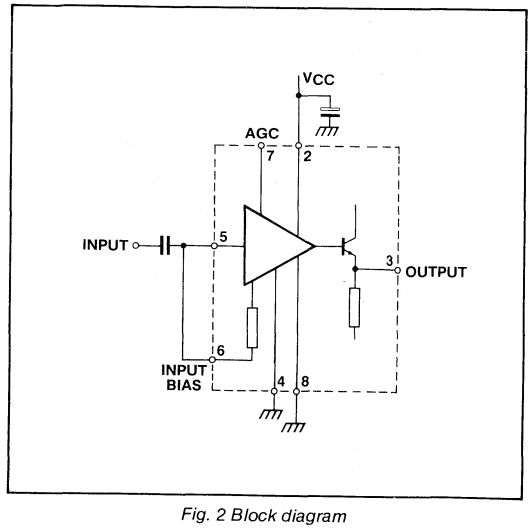


Fig. 2 Block diagram

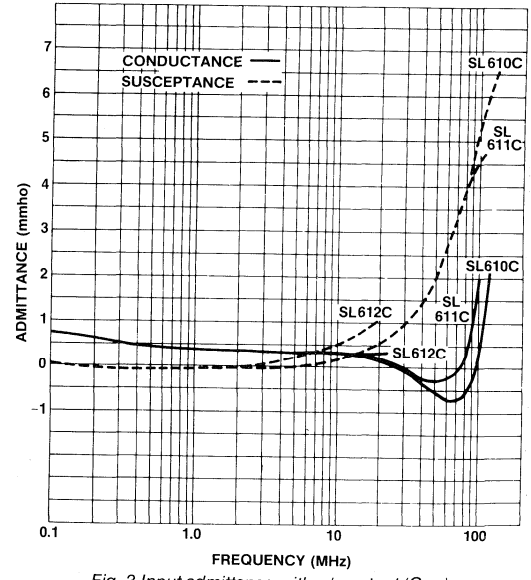


Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL610C 30MHz
SL611C 30MHz
SL612C 1.75MHz

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL610C		15	20	mA	
	SL611C		15	20	mA	No signal, pin 3 open circuit
	SL612C		3.3	5	mA	
Voltage gain	SL610C	18	20	22	dB	R_S = 50Ω
	SL611C	24	26	28	dB	RL = 22°C
	SL612C	32	34	36	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL610C	85	120		MHz	
	SL611C	50	80		MHz	
	SL612C	10	15		MHz	
Max.output signal (max.AGC)			1.0		V rms	RL = 150Ω (SL610C/611C)
						RL = 1.2kΩ (SL612C)
Max.input signal (max.AGC)			250		mV rms	
AGC range	SL610C	40	50		dB	
	SL611C	40	50		dB	Pin 7 0V to 5.1V
	SL612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL610C, SL611C and SL612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL610C, SL611C only) and is shown in Fig. 3. If the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

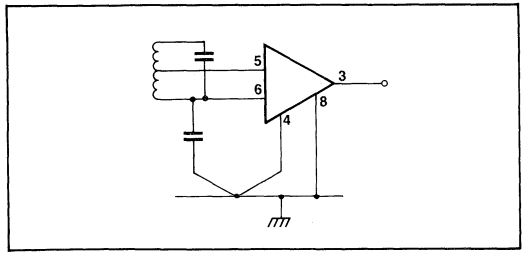


Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

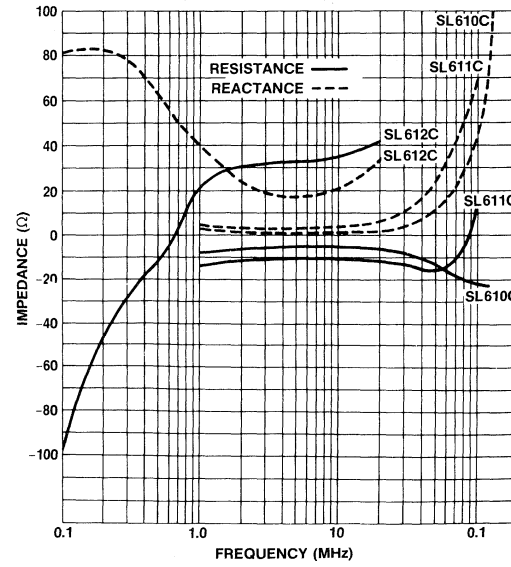


Fig. 5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

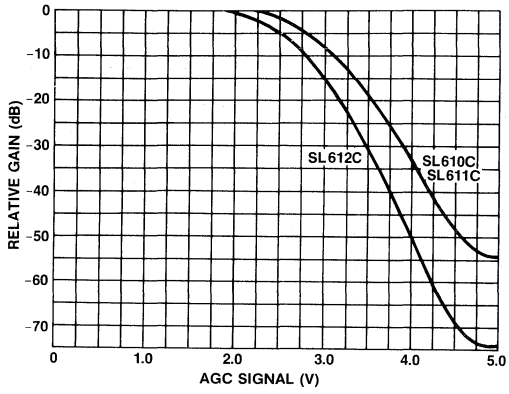


Fig. 6 AGC characteristics (typical)

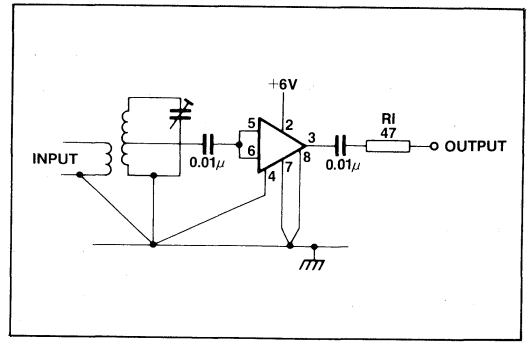


Fig. 7 RF preamplifier

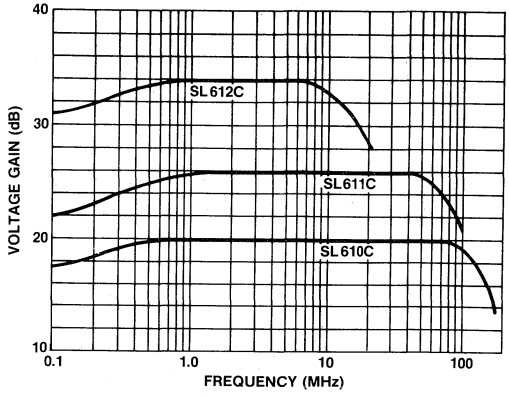


Fig. 8 Typical voltage gain (R_S=50 Ω)

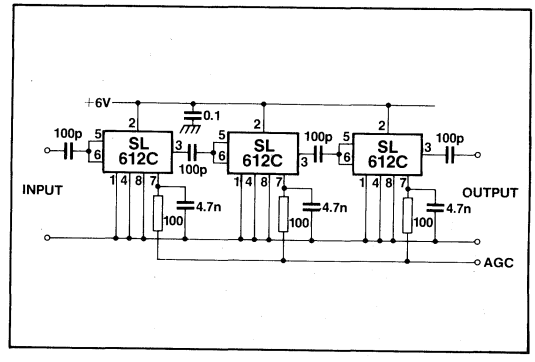


Fig. 9 IF amplifier using SL612

SL621C

AGC GENERATOR

The SL621C is an AGC generator designed specifically for use in SSB receivers in conjunction with the SL610C, SL611C and SL612C RF and IF amplifiers. In common with other advanced systems it generates a suitable AGC voltage directly from the detected audio waveform, provides a 'hold' period to maintain the AGC level during pauses in speech, and is immune to noise interference. In addition it will smoothly follow the fading signals characteristic of HF communication.

When used in a receiver comprising one SL610C and one SL612C amplifier and a suitable detector, the SL621C will maintain the output within a 4dB range for a 110dB range of receiver input signal.

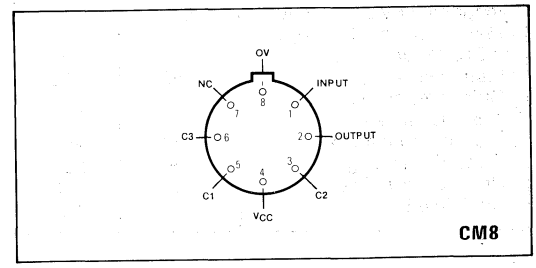


Fig. 1 Pin connections (bottom view)

FEATURES

- All Time Constants Set Externally
- Easy Interfacing
- Compatible with SL610/611/612

APPLICATIONS

- SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply voltage: 6V
- Supply current: 3mA

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

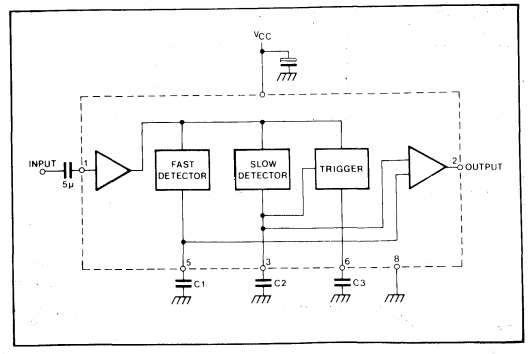


Fig. 2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V
Ambient temperature: −30°C to +85°C
Test frequency: 1kHz
Test circuit as Fig. 2

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.1	4.3	mA	No signal
Cut-off frequency (−3dB)		6		kHz	
Input for 2.2V DC output	3	7	11	mVrms	
Input for 4.6V DC output	9	11	16	mVrms	
Maximum output voltage	5.1			V	
AC ripple on output		12	20	mV pk-pk	1kHz, output open circuit
Input resistance	350	500	700	Ω	
Output resistance		70	230	Ω	
'Fast' rise time t_1		20	55	ms	0 to 50% full output
'Fast' decay time t_2	150	200	330	ms	100% to 36% full output
'Slow' rise time t_3	150	200	300	ms	Time to output transistion point
Hold collapse time t_4	65	100	150	ms	90% to 10% full output
Hold time t_5	0.75	1.0	1.25	s	

APPLICATION NOTES

The SL621C consists of an input AF amplifier coupled to a DC output amplifier by means of two detectors having short and long rise and fall times respectively. The time constants of these detectors are set externally by capacitors on pins 5 (C_1) and 3 (C_2).

The detected audio signal at the input will rapidly establish an AGC level via the 'fast' detector time in t_1 (see Fig. 3). Meanwhile the long time constant detector output will rise and after t_3 will control the output because this detector is more sensitive.

Input signals greater than approximately 4mV rms will actuate a trigger circuit whose output pulses provide a discharge current for C_2.

By this means the voltage on C_2 can decay at a maximum rate, which corresponds to a rise in receiver gain of 20dB/s. Therefore the AGC system will smoothly follow signals which are fading at this rate or slower. However should the receiver input signals fade faster than this, or disappear completely as during pauses in speech, then the input to the AGC generator will drop below the 4mV rms threshold and the trigger will cease to operate. As C_2 then has no discharge path, it will hold its charge (and hence the output AGC level) at the last attained value. The output of the short time constant detector will drop to zero in time t_2 after the disappearance of the signal.

The trigger pulses also charge C_3. When the trigger pulses cease, C_3 discharges and after t_5 C_2 is discharged rapidly (in time t_4) and so full receiver gain is restored. The hold time, t_5 is approximately one second with C_3 = 100μF.

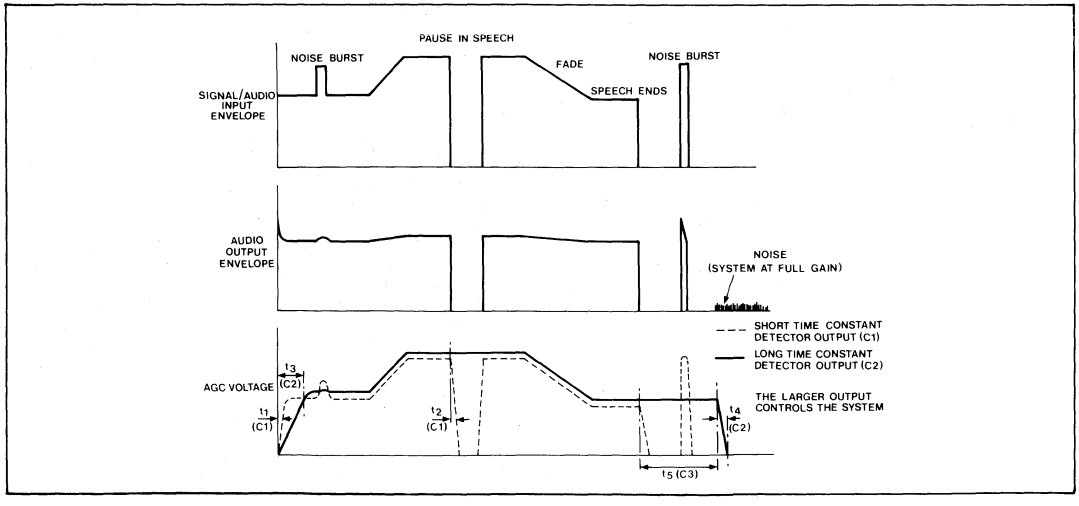


Fig. 3 Dynamic response of a system controlled by SL621C AGC generator

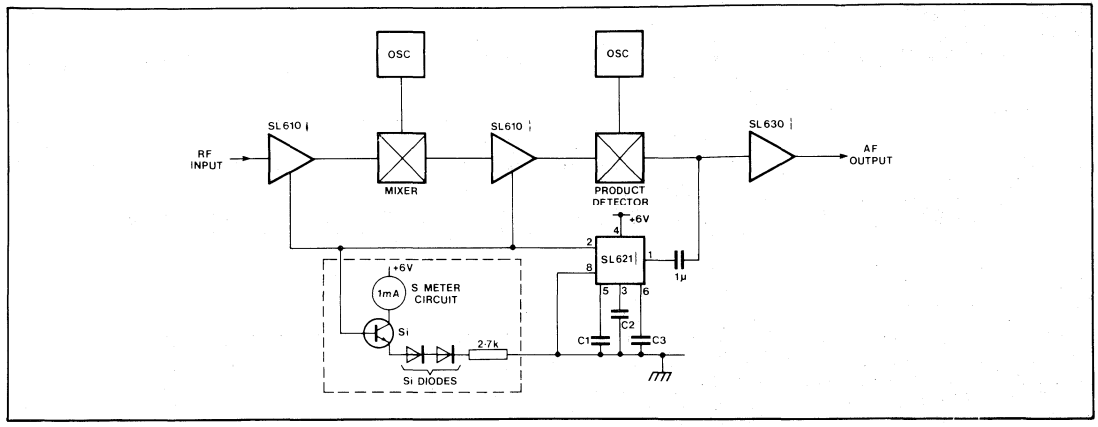


Fig. 4 SL621C used to control SSB receiver

If signals reappear during t_5, then C_3 will recharge and normal operation will continue. The C_3 recharge time is made long enough to prevent prolongation of the hold time by noise pulses.

Fig. 3 shows how a noise burst superimposed on speech will initiate rapid AGC action via the short time constant detector while the long time constant detector effectively remembers the pre-noise AGC level.

The various time constants quoted are for $C_1 = 50\mu F$ and $C_2 = C_3 = 100\mu F$. These time constants may be altered by varying the appropriate capacitors. C_1 controls t_1, t_2; C_2 controls t_3, t_4; C_3 controls t_5.

The supply must either have a source resistance of less than 2Ω at LF or be decoupled by at least $500\mu F$ so that it is not affected by the current surge resulting from a sudden input on pin 1.

In a receiver for both AM and SSB using an SL623C detector/carrier AGC generator, the AGC outputs of the SL621C and SL623C may be connected together provided that no audio reaches the SL621C input while the SL623C is controlling the system.

AGC lines may require some RF decoupling but the total capacitance on the output should not exceed 15000pF or the impulse suppression will suffer.

Under some conditions,overload of the AGC output may occur in a receiver. Possible solutions are shown in Figs.6 and 7.

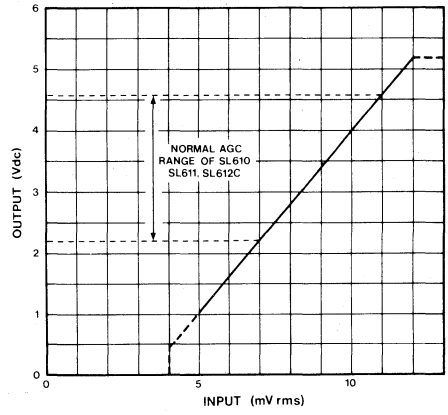


Fig. 5 Transfer characteristic of SL621C (typical)

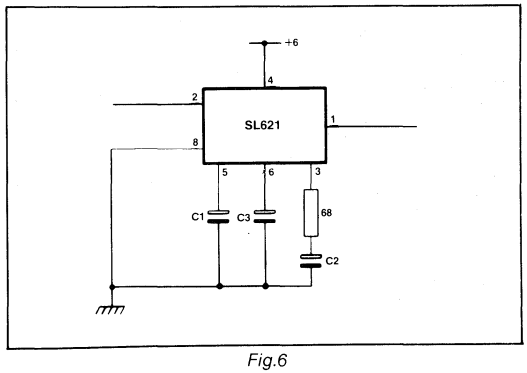


Fig.6

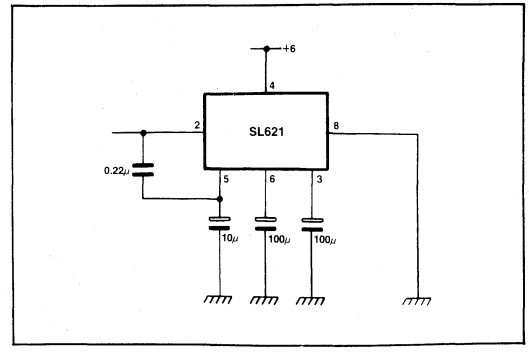


Fig.7

PLESSEY
Semiconductors

SL623C

AM DETECTOR, AGC AMPLIFIER & SSB DEMODULATOR

The SL623C is a silicon integrated circuit combining the functions of low level, low distortion AM detector and AGC generator with SSB demodulator. It is designed specially for use in SSB/AM receivers in conjunction with SL610C, SL611C and SL612C RF and IF amplifiers. It is complementary to the SL621C SSB AGC generator.

The AGC voltage is generated directly from the detected carrier signal and is independent of the depth of modulation used. Its response is fast enough to follow the most rapidly fading signals. When used in a receiver comprising one SL610C and one SL612C amplifier, the SL623C will maintain the output within a 5dB range for a 90dB range of receiver input signal.

The AM detector, which will work with a carrier level down to 100mV, contributes negligible distortion up to 90% modulation. The SSB demodulator is of single balanced form. The SL623C is designed to operate at intermediate frequencies up to 30MHz. In addition it functions at frequencies up to 120MHz with some degradation in detection efficiencies.

FEATURES

- Negligible Distortion
- Easy Interfacing
- Fast Response Time

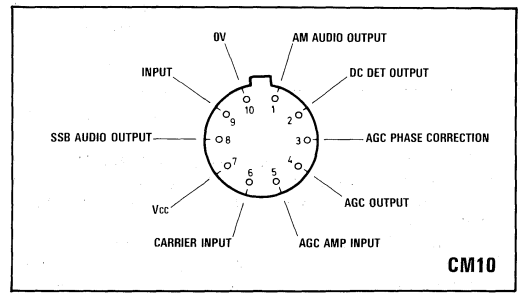


Fig. 1 Pin connections (bottom view)

APPLICATIONS

- AM SSB Receivers
- Test Equipment

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Maximum Frequency: 30MHz

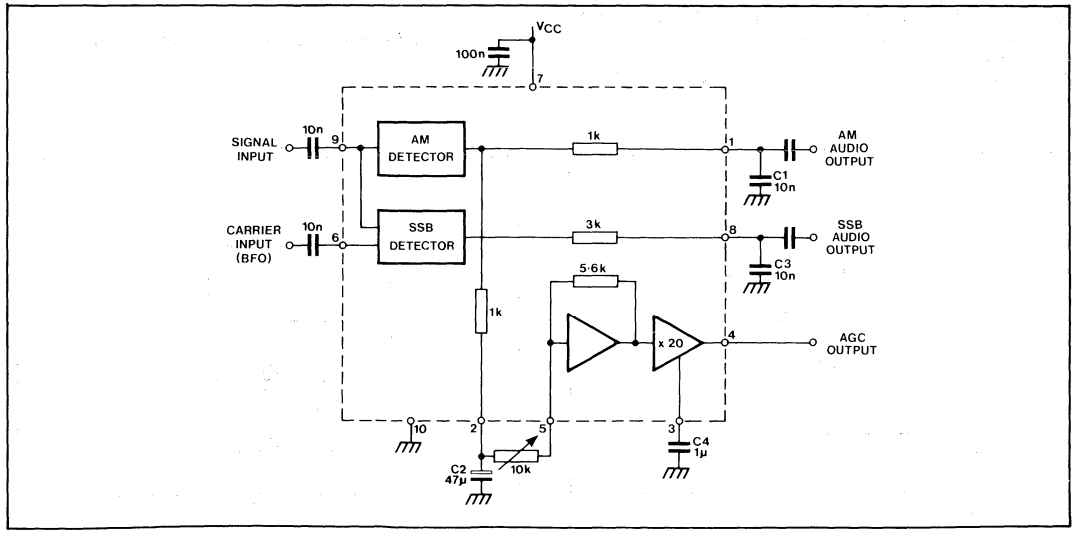


Fig. 2 block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC} = 6V |
Ambient temperature = −30°C to +85°C
Test circuit as Fig. 2

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		9	11	mA	No signal, Pin 4 open
Input impedance		800		Ω	Pins 6, 9
SSB audio output	22	30	47	mV rms	Signal input 20mV rms @ 1.748 MHz. Ref. signal input 100mV @ 1.750 MHz
AM audio output	43	55	67	mV rms	Signal input 125mV rms @ 1.75MHz modulated to 80% at 1kHz
AGC range (Note 1)			6	dB	Initial signal input 125mV rms at 1.75MHz modulated to 80% at 1kHz. Output set to 2.0V with 10kΩ potentiometer between Pins 2 & 5.

NOTES
1. The AGC range is the change in input level to increase AGC output voltage from 2.0V to 4.6V

APPLICATION NOTES

AGC Generator

Pin 3, the AGC amplifier phase correction point should be decoupled to ground by a 1 microfarad capacitor (C4), keeping leads as short as possible. The value of C4 is quite critical, and should not be altered: if it is increased the increased phase shift in the AGC loop may cause the receiver to become unstable at LF and if it is reduced the modulation level of the incoming signal will be reduced by fast-acting AGC.

The AGC output (Pin 4) will drive at least two SL610/11/12 amplifiers. The SL623AGC output is an emitter follower similar to that of the SL621C. Hence the outputs of the two devices may be connected in parallel when constructing AM/SSB systems.

Less signal is needed to drive the SSB demodulator than the AM detector. In a combined AM/SSB system, therefore, the signal will automatically produce an SSB AGC voltage via the SL621C as long as a carrier (BFO) is present at the input to the SSB demodulator of the SL623C. The AGC generator of the SL623 will not contribute in such a configuration.

For AM operation the BFO must be disconnected from the carrier input of the SSB demodulator. In the absence of an input signal, the SL621C will then return to its quiescent state. To switch over a receiver using the SL623C from SSB to AM operation it is therefore necessary to turn off the BFO and transfer the audio pick-off from the SSB to the AM detector.

Neglecting to disconnect the SSB carrier input during AM operation can result in heterodyning due to pick-up of carrier on the input signal. In some sets different filters are used for AM and SSB; these will also need to be switched.

The 10 kilohm gain-setting preset potentiometer is adjusted so that a DC output of 2 volts is achieved for an input of 125mV rms. There will then be full AGC output from the SL623C for a 4dB increase in input. A fixed resistor of 1.5 kilohms can often be used instead of the potentiometer.

SSB Demodulator

The carrier input is applied to Pin 6, via a low-leakage capacitor. It should have an amplitude of about 100mV rms and low second harmonic content to avoid disturbing the DC level at the detector output.

Pin 8 is the SSB output and should be decoupled at RF by a 0.01 microfarad capacitor. The output impedance of the detector is 3 kilohm and the terminal is at a potential of about +2V which may be used to bias an emitter follower if a lower output impedance is required. The input to the audio stage of a receiver using an SL623C should be switched between the AM and the SSB outputs — no attempt should be made to mix them. Since the SL621C is normally used in circumstances where low-level audio is obtained from the detector, the relatively high SSB audio output of the SL623C must be attenuated before being applied to the SL621C. This is most easily done by connecting the SL623C to the SL621C via a 2 kilohm resistor in series with a 0.5 microfarad capacitor.

Input Conditions

The input impedance is about 800 ohms in parallel with 5pF. Connection must be made to the input via a capacitor to preserve the DC bias. An input of about 125mV rms is required for satisfactory carrier AGC performance and 20mV rms for SSB detection. Normally, the AGC will cope with this variation but in an extreme case a receiver using an SL623C and having the same gain to the detector in both AM and SSB modes will be some 10dB less sensitive to AM.

PLESSEY
Semiconductors

SL640C & SL641C

DOUBLE BALANCED MODULATORS

The SL640C and SL641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL641 has a single output designed as a current drive to a tuned circuit.

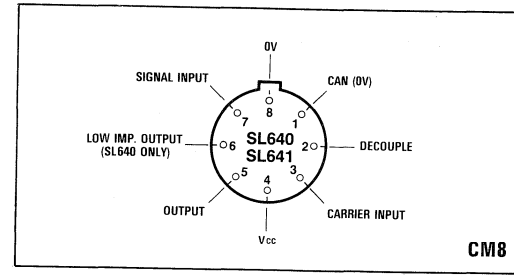


Fig. 1 Pin connections (bottom view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

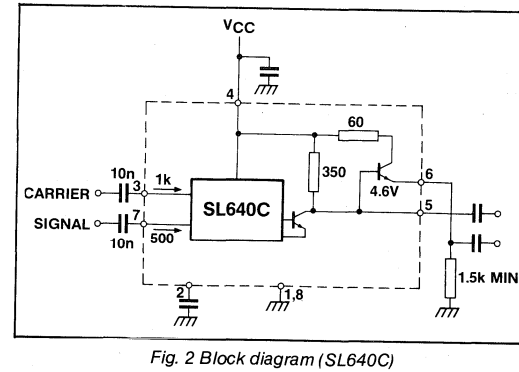


Fig. 2 Block diagram (SL640C)

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

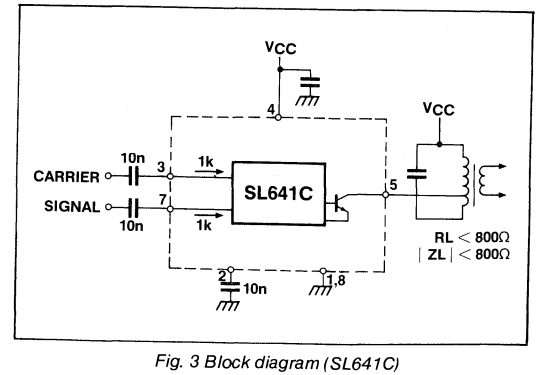


Fig. 3 Block diagram (SL641C)

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL640C		12	17	mA	
	SL641C		10	13	mA	
Conversion gain	SL640C	−3	0	+3	dB	
Conversion transconductance	SL641C	1.75	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL640C		500		Ω	
	SL641C		1		kΩ	
Maximum input voltage	SL640C		210		mV rms	
	SL641C		250		mV rms	
Signal leak	SL640C		−30	−18	dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL640C		−30	−20	dB	
Signal leak	SL641C		−18	−12	dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL641C		−25	−12	dB	
Intermodulation products	SL640C		−45	−35	dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL641C		−45	−30	dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 3.75MHz

APPLICATION NOTES

The SL640C and SL641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

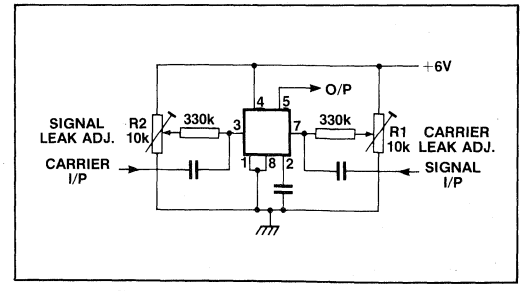


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

SL952

UHF LIMITING AMPLIFIER

The SL952 is a single chip limiting amplifier for use up to 1GHz. It features differential inputs and outputs and is suitable for use as a prescaler driver, limiting amplifier etc.

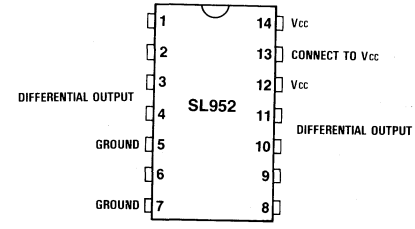
The device operates from a single 5V supply with a minimal number of external components and is encapsulated in either a 14 lead DIL package or a 16 lead chip carrier.

FEATURES

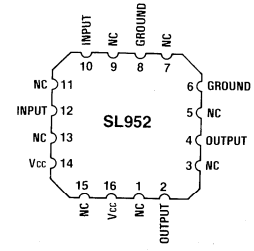
- Low Cost
- High Gain
- Minimal External Component Count
- Good Limiting Characteristics
- 1GHz Response
- 5V Supply

ABSOLUTE MAXIMUM RATINGS

Vcc	+10V
Ambient temperature	0°C to +65°C
Storage temperature	-55°C to +125°C



NOTE: Ground all other unused pins. **DP14**



LC16

Fig.1 Pin connections - top view

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Vcc = +5V, Tamb = +25°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4.75	5.00	5.50	V	
Supply current		70	90	mA	
DC output level		3.2		V	
Output offset		100	600	mV	
Maximum differential output swing	600			mV p-p	950MHz
Differential voltage gain	30	35		dB	100MHz
Differential voltage gain	30	35		dB	500MHz
Differential voltage gain	15	26		dB	950MHz
Gain variation with supply		1		dB	Between 4.75V and 5.25V
Reverse isolation		30		dB	500MHz
1dB gain compression point		37		dBm	Input 10-900MHz
Input impedance		310Ω// 1.8pF			500MHz

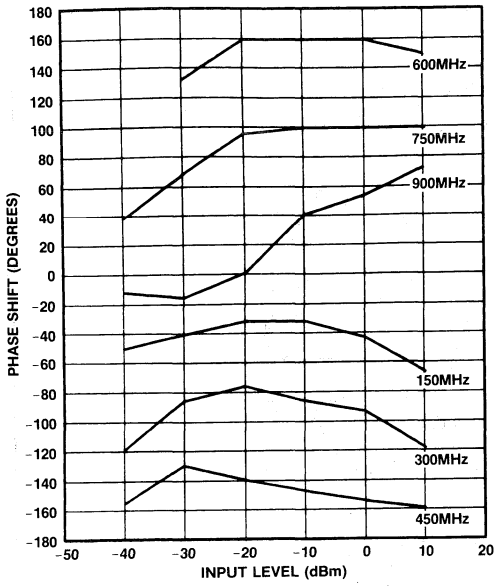


Fig.2 Phase shift/amplitude at various frequencies (input and output terminated at 50Ω

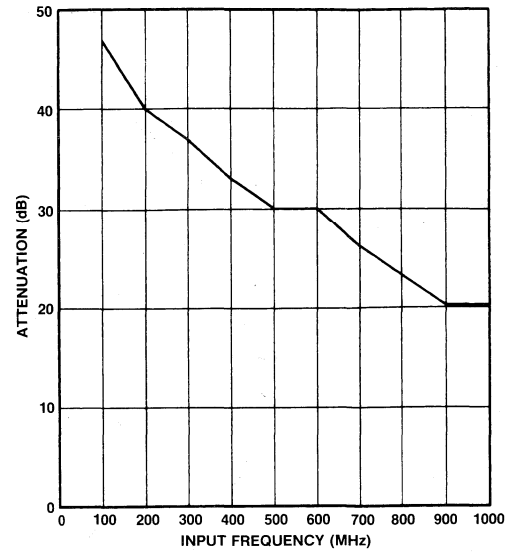


Fig.3 Input/output characteristic, 10-900MHz

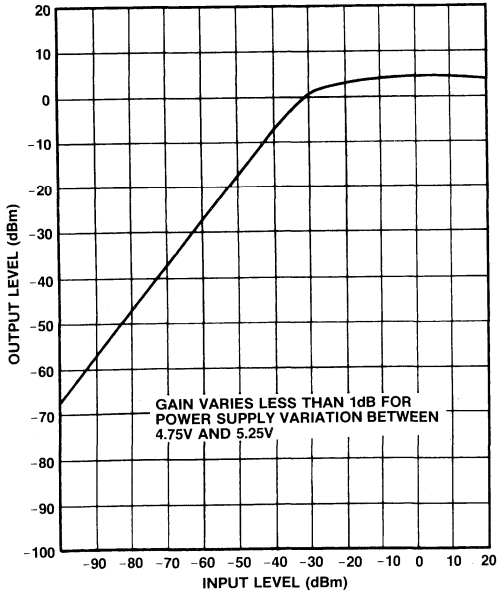


Fig.4 Reverse isolation v. input frequency

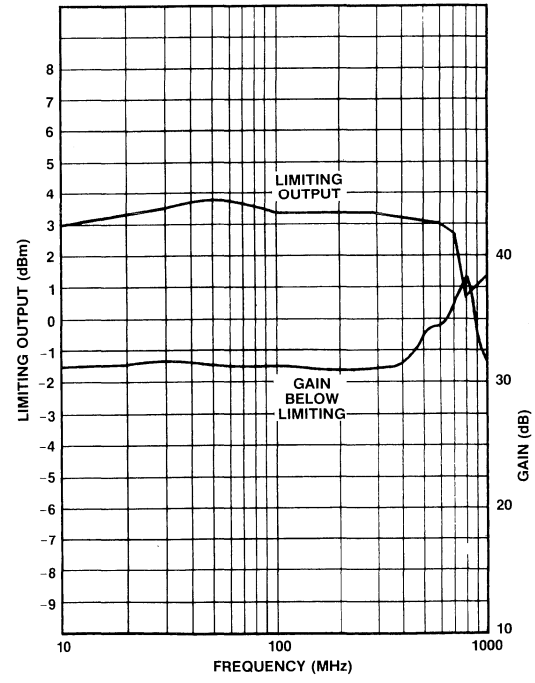


Fig.5 Limiting output v. frequency input -15dBm and gain below limiting v. frequency input -50dBm

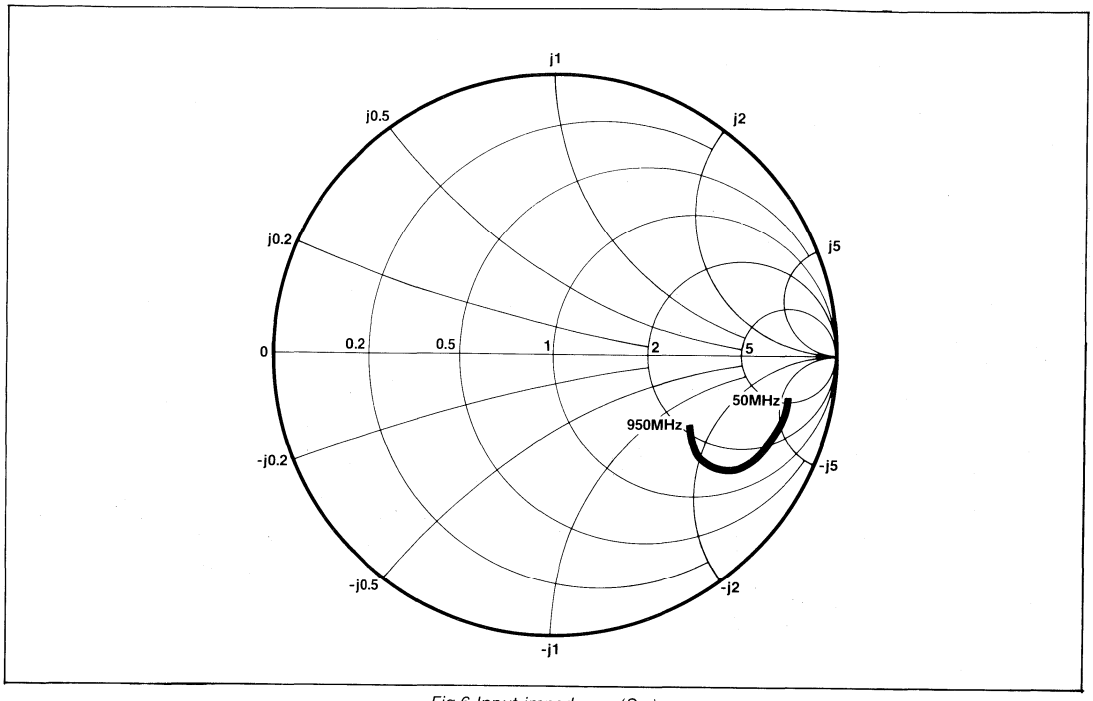


Fig.6 Input impedance (S_{11})

PLESSEY
Semiconductors

SL1521A & C

300MHz WIDEBAND LOG AMPLIFIER

The SL1521A and C are wideband amplifiers intended for use in successive detection logarithmic IF strips operating at centre frequencies of up to 200MHz. It is a plug in replacement for the SL521 series of RF amplifiers. The mid-band voltage gain of the SL1521 is typically 12dB. The SL1521A and C differ mainly in the tolerance of voltage gain.

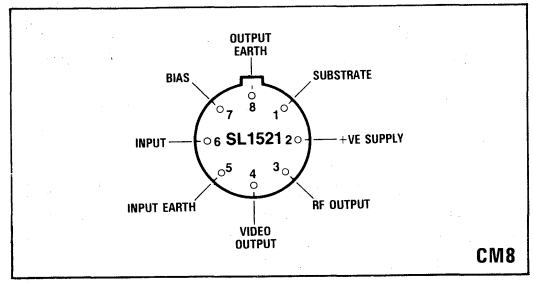


Fig.1 Pin connections

APPLICATIONS

- Radar IF Strips
- Wideband Amplification

ABSOLUTE MAXIMUM RATINGS

Storage temperature	−55°C to +150°C
Operating temperature	−55°C to +125°C
Maximum chip operating temperature	150°C
Chip to ambient thermal resistance	250°C/W

Test circuits: see Fig.8

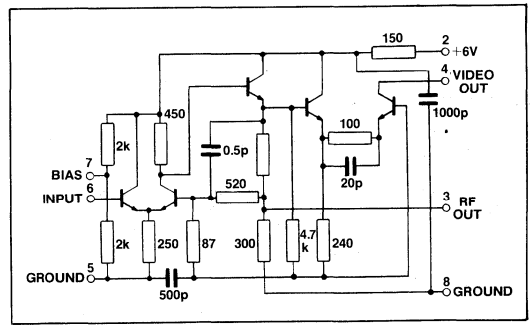


Fig.2 Circuit diagram

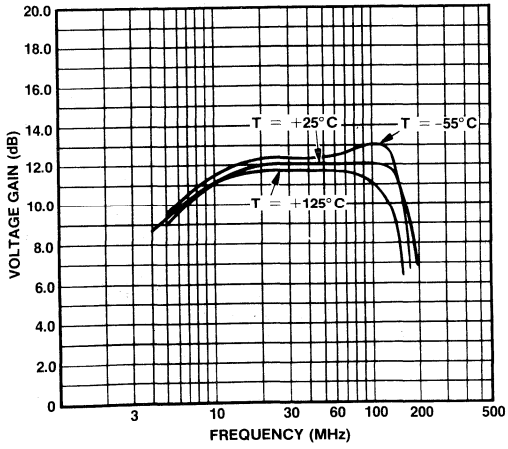


Fig.3 Voltage gain v. frequency

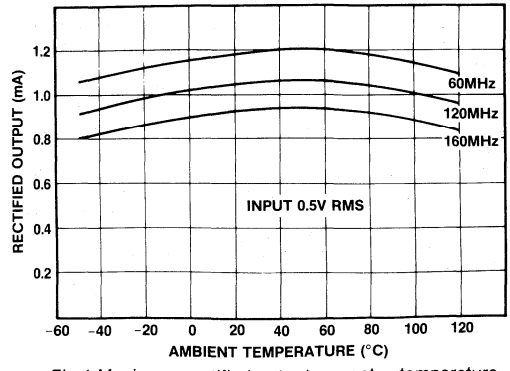


Fig.4 Maximum rectified output current v. temperature

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Temperature = +22°C ± 2°C
Supply voltage = +5.2V
DC connection between input and bias pins.

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Voltage gain, f = 120MHz	SL1521A	11.5		12.5	dB	3mV rms input, 50 ohms source, 8pF load + 500Ω
	SL1521C	10.8		13.1	dB	
Voltage gain, f = 160MHz	SL1521A	11.2		12.8	dB	
	SL1521C	10.6		13.4	dB	
Upper cut-off frequency	SL1521A	250	285		MHz	50 ohms source
	SL1521C		285		MHz	
Lower cut-off frequency	All types		6	10	MHz	50 ohms source
Propagation delay	All types		0.6		ns	
Maximum rectified video output current	SL1521A	0.95		1.05	mA	f = 120MHz, 0.5V rms input, 8pF load, 500 ohms in parallel
	SL1521C	0.90		1.20	mA	
Variation of gain with supply voltage	All types		1.0		dB/V	
Variation of maximum rectified output current with supply voltage	All types		30		%/V	
Maximum input signal before overload	All types		1.5		V rms	See note below
Noise figure			3	4.5	dB	f = 120MHz, source
Supply current	All types	10.0	15.0	20.0	mA	resistance optimised
Maximum RF output voltage	All types	1.0			V p-p	f = 120MHz

Operating Notes

The amplifiers are intended for use directly coupled, as shown in Fig.7.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 8. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nF	10nF	3nF	1nF

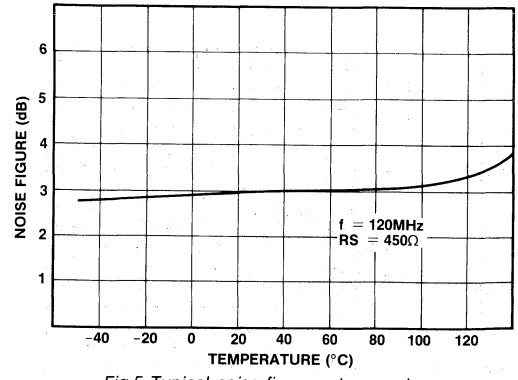


Fig.5 Typical noise figure v. temperature

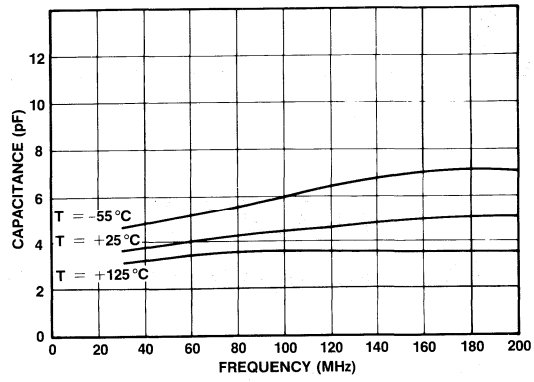


Fig.6 Input admittance with open-circuit output

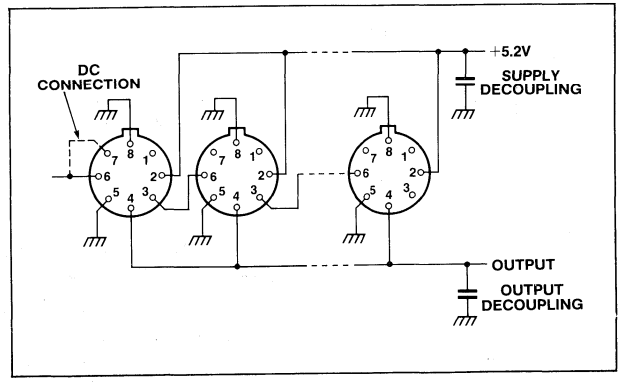


Fig.7 Direct coupled amplifier

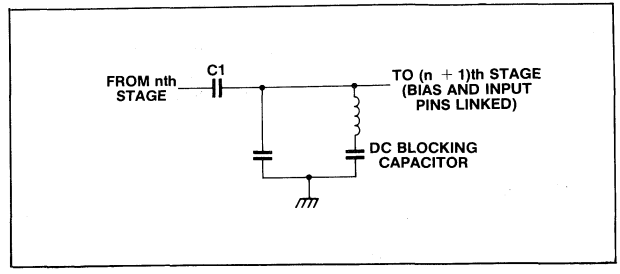


Fig.8 Suitable interstage tuned circuit

SL1523C

300MHz DUAL WIDEBAND LOG AMPLIFIER

The SL1523C consists of two SL1521's in series, and is intended to reduce the package count and improve the packing density in logarithmic strips at frequencies up to 200 MHz.

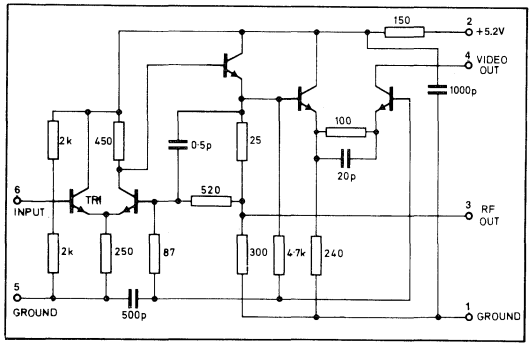


Fig. 2 SL1523 circuit diagram (each amp)

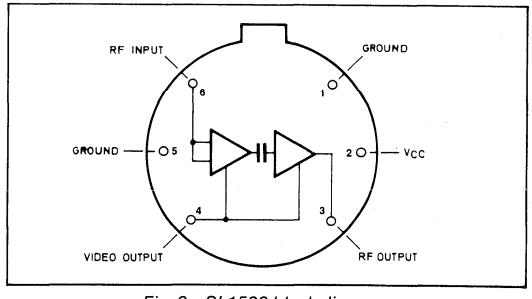


Fig. 3 SL1523 block diagram

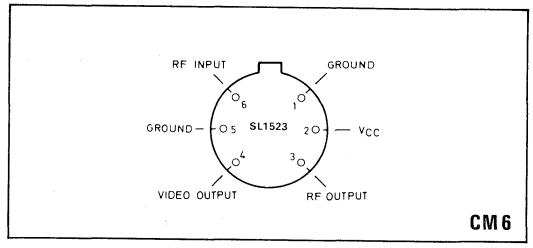


Fig. 1 Pin connections (bottom view)

Absolute Maximum Ratings (Non-Simultaneous)

The absolute maximum ratings are limiting values above which operating life may be shortened or satisfactory performance may be impaired.

Storage temperature range	—55°C to +175°C
Operating temperature	—55°C to +125°C
Chip operating temperature:	150°C
Chip-to-ambient thermal resistance	300°C/W
Chip-to-case thermal resistance	95° C/W
Maximum instantaneous voltage at video output	+12V
Supply voltage	+ 9V

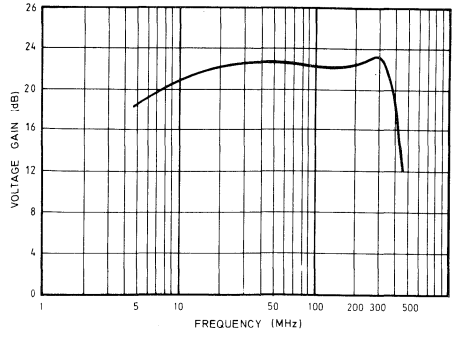


Fig. 4 Voltage gain v. frequency

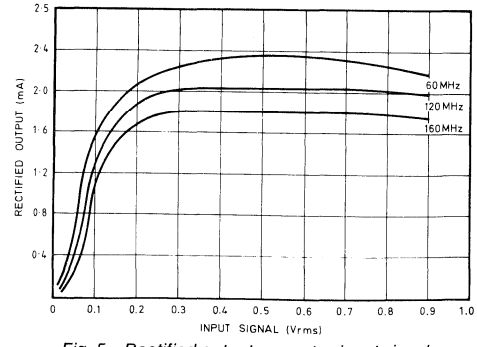


Fig. 5 Rectified output current v. input signal

ELECTRICAL CHARACTERISTICS

Test Conditions (unless otherwise stated):
Temperature = 22°C ± 2°C
Supply voltage = + 5.2V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	21		27	dB	f = 120MHz, 3mV rms input, 50Ω source 4pF load + 50Ω
Voltage gain	20		27	dB	f = 160MHz, 3mV rms input, 50Ω source 4pF load + 500Ω
Upper cut-off frequency	175	200		MHz	50Ω source
Lower cut-off frequency		8	20	MHz	50Ω source
Propagation delay		1.2		ns	
Maximum rectified video output current	1.6		2.0	mA	f = 120MHz, 0.5V rms input, 4pF load
Variation of gain with supply voltage		2.0		dB/V	
Variation of maximum rectified output current with supply voltage		30		%/V	
Maximum input signal before overload		1.5		V rms	See note below
Noise figure		3		dB	f = 120MHz, source resistance optimised
Supply current	20	30	40	mA	
Maximum RF output voltage	1.0			V p-p	f = 120MHz

Note: Overload occurs when the input signal reaches a level sufficient to forward bias the base-collector junction of TR1 on peaks.

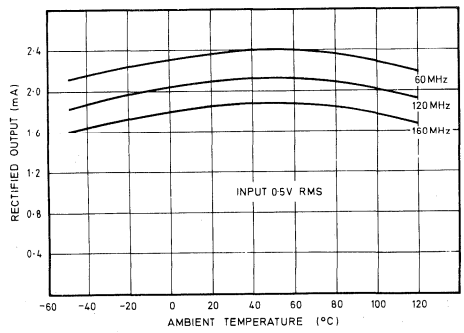


Fig.6 Maximum rectified output current v. temperature

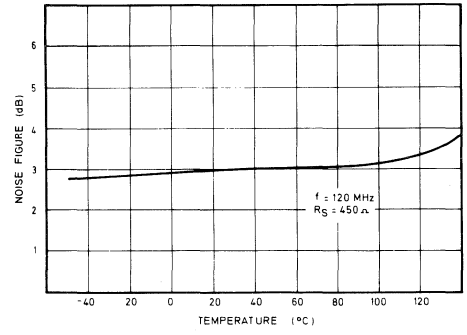


Fig.8 Input admittance with open circuit output

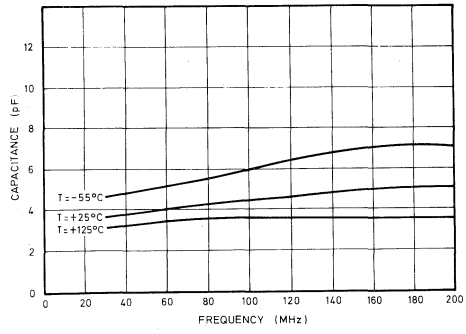


Fig.7 Typical noise figure v. temperature

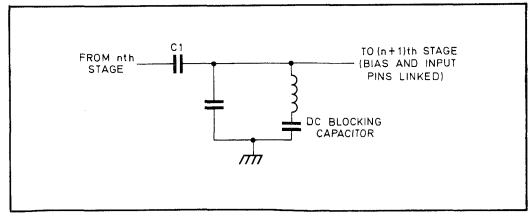


Fig.9 Suitable interstage tuned circuit

PLESSEY
Semiconductors

SL1611 IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL1610C, SL1611C, SL1612C

RF/IF AMPLIFIERS

The SL1610C, SL1611C and SL1612C are RF voltage amplifiers with AGC facilities. The voltage gains are 10, 20 and 50 times respectively and the upper frequency response varies from 15 MHz to 120 MHz according to type.

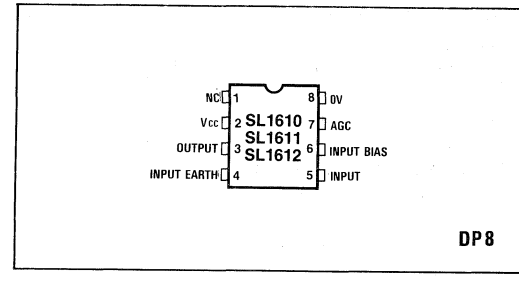


Fig. 1 Pin connections (top view)

FEATURES

- Wide AGC Range: 50dB
- Easy Interfacing
- Integral Power Supply RF Decoupling

APPLICATIONS

- RF Amplifiers
- IF Amplifiers

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Voltage Gain: 20dB to 34dB

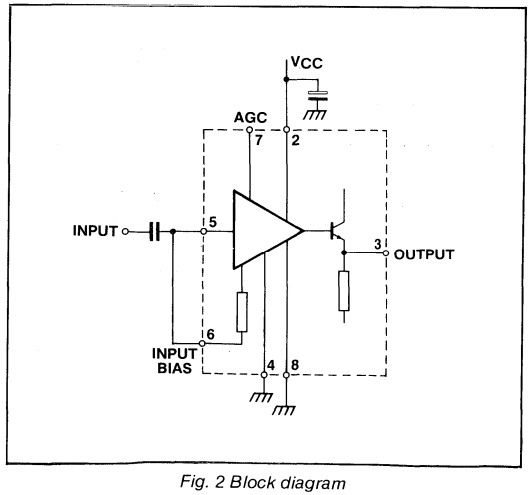


Fig. 2 Block diagram

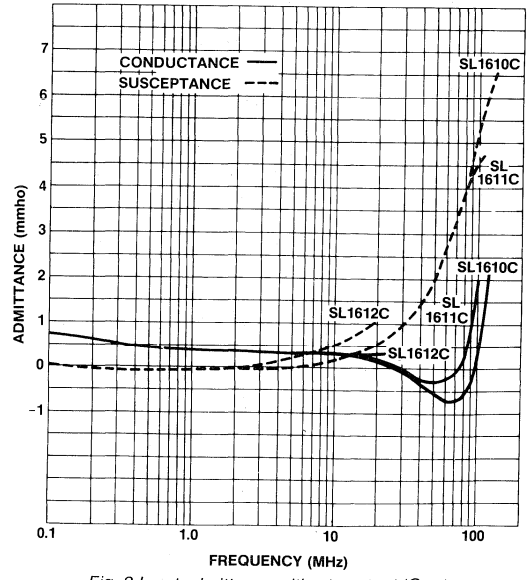


Fig. 3 Input admittance with o/c output (G_{11})

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C
Test frequency: SL1610C 30MHz
SL1611C 30MHz
SL1612C 1.75MHz

Characteristics	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1610C		15	24	mA	
	SL1611C		15	24	mA	No signal, pin 3 open circuit
	SL1612C		3.3	6	mA	
Voltage gain	SL1610C	17	20	24	dB	R_S = 50Ω
	SL1611C	23	26	30	dB	RL = 500Ω
	SL1612C	31	34	38	dB	T_{amb} = 22°C
Cut-off frequency (-3dB)	SL1610C		120		MHz	
	SL1611C		80		MHz	
	SL1612C		15		MHz	
Max.output signal (max.AGC)			1.0		V rms	RL = 150Ω (SL1610C/1611C)
						RL = 1.2kΩ (SL1612C)
Max.input signal (max.AGC)			250		mV rms	
AGC range	SL1610C	40	50		dB	
	SL1611C	40	50		dB	Pin 7 0V to 5.1V
	SL1612C	60	70		dB	
AGC current			0.15	0.6	mA	Current into pin 7 at 5.1V

APPLICATION NOTES

Input circuit

The SL1610C, SL1611C and SL1612C are normally used with pins 5 and 6 connected together and with the input connected via a capacitor as shown in Fig. 2.

The input impedance is negative between 30MHz and 100MHz (SL1610C, SL1611C only) and is shown in Fig. 3. the source is inductive it should be shunted by a 1kΩ resistor to prevent oscillation.

An alternative input circuit with improved noise figure is shown in Fig. 4.

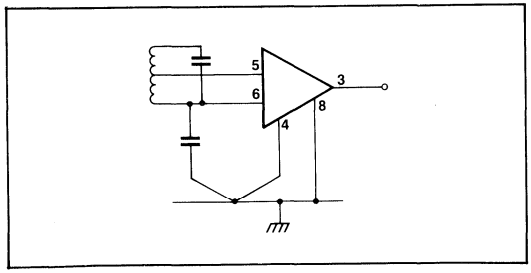


Fig. 4 Alternative input circuit

Output circuit

The output stage is an emitter follower and has a negative output impedance at certain frequencies as shown in Fig. 5.

To prevent oscillation when the load is capacitive a 47Ω resistor should be connected in series with the output.

AGC

When pin 7 is open circuit or connected to a voltage less than 2V the voltage gain is normal. As the AGC voltage is increased there is a reduction in gain as shown in Fig.6. This reduction varies with temperature.

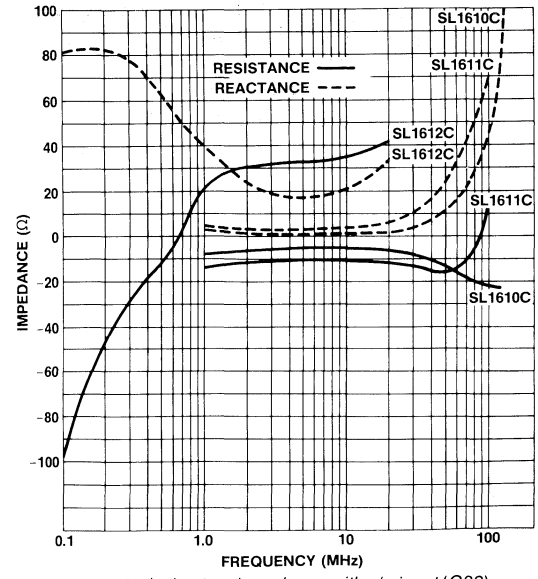


Fig. 5 Typical output impedance with s/c input (G22)

Typical applications

The circuit of Fig. 7 is a general purpose RF preamplifier. The voltage gain (from pin 5 to pin 3) is shown in Fig. 8. Fig. 9 is the IF section of a simple SSB transceiver. At 9MHz it has a gain of 100dB.

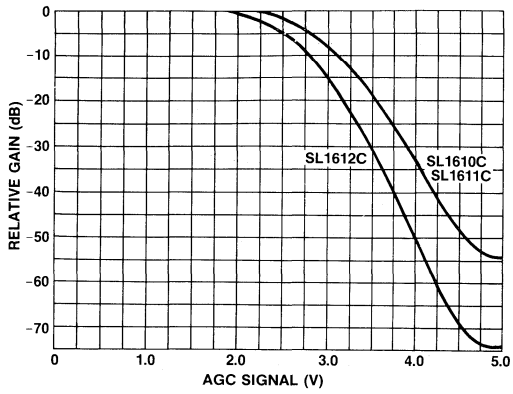


Fig. 6 AGC characteristics (typical)

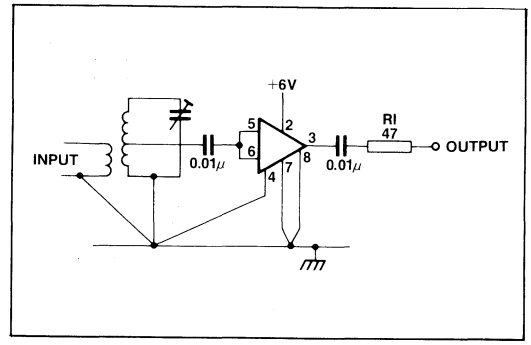


Fig. 7 RF preamplifier

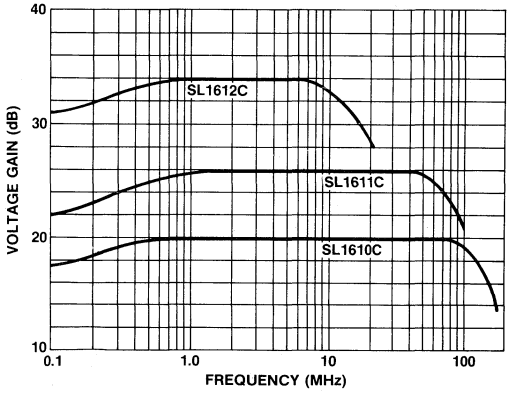


Fig. 8 Typical voltage gain (R_S=50Ω)

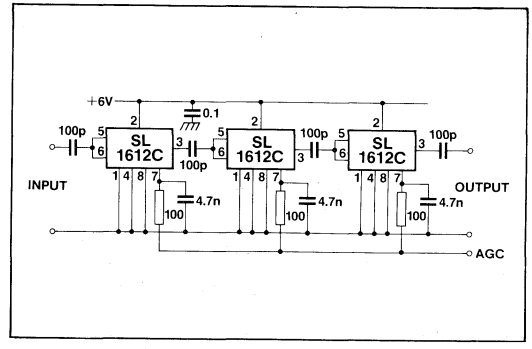


Fig. 9 IF amplifier using SL1612

SL1613C

WIDEBAND LOG IF STRIP AMPLIFIER

The SL1613C is a bipolar monolithic integrated circuit wideband amplifier intended primarily for use in successive detection logarithmic IF strips, operating at centre frequencies between 10MHz and 60MHz. The devices provide amplification, limiting and rectification, are suitable for direct coupling and incorporate supply line decoupling. The mid-band voltage gain of the SL1613C is typically 12dB.

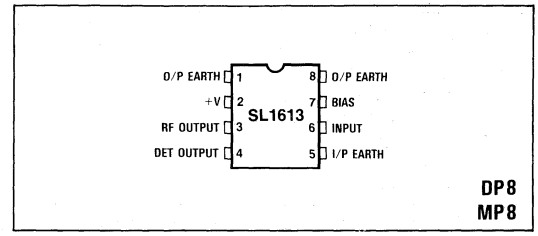


Fig. 1 Pin connections (top)

FEATURES

- Well Defined Gain
- 4.5dB Noise Figure
- High I/P Impedance
- Low O/P Impedance
- 150MHz Bandwidth
- On-Chip Supply Decoupling
- Low External Component Count

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	−55°C to +125°C
Operating temperature range	−30°C to +85°C
Maximum instantaneous voltage at video output	+12V
Supply voltage	9V

APPLICATIONS

- Logarithmic IF Strips with Gains up to 108dB and Linearity Better than 2dB
- Low Cost Radar
- Radio Telephone Field Strength Meters

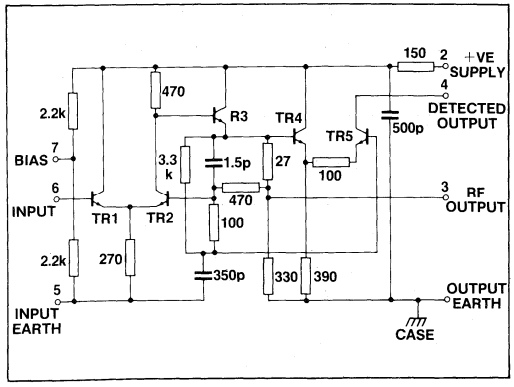


Fig. 2 Circuit diagram

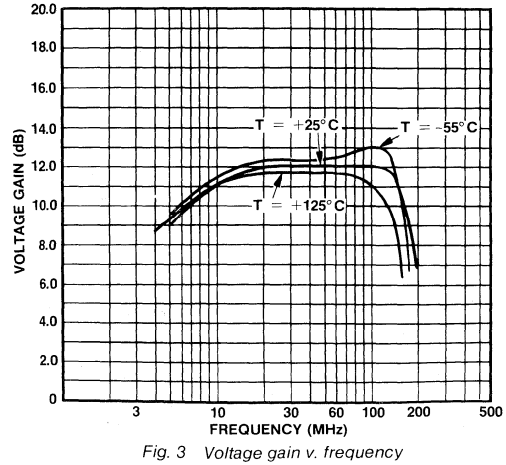


Fig. 3 Voltage gain v. frequency

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_A = +22°C ±2°C
Supply voltage = +6V
DC connection between input and bias pins

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Voltage gain	10	12	14	dB	f=30MHz, R_S=10Ω, C_L=8pF
Upper cut-off frequency (Fig. 3)		150		MHz	R_S=10Ω, C_L=8pF
Lower cut-off frequency (Fig. 3)		5		MHz	R_S=10Ω, C_L=8pF
Propagation delay		2		ns	
Max. rectified video output current (Figs. 4 and 5)	0.8	1	1.3	mA	f=60MHz, V_{in}=500mV rms
Variation of gain with supply voltage		0.7		dB/V	
Variation of maximum rectified output current with supply voltage		25		% / V	
Maximum input signal before overload		1.9		V rms	See Note 1
Noise figure (Fig. 6)		4.5		dB	f=60MHz, R_s=450Ω
Maximum RF output voltage		1.2		Vp-p	
Supply current		15	20	mA	

Note 1. Overload occurs when the input signal reaches a level sufficient to forward bias the base collector junction of TR1 on peak.

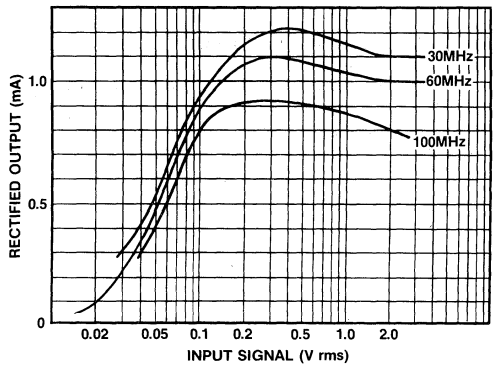


Fig. 4 Rectified output current v. input signal

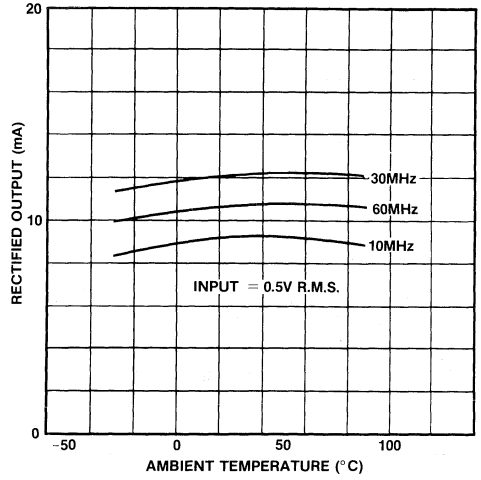


Fig. 5 Maximum rectified output current v. temperature

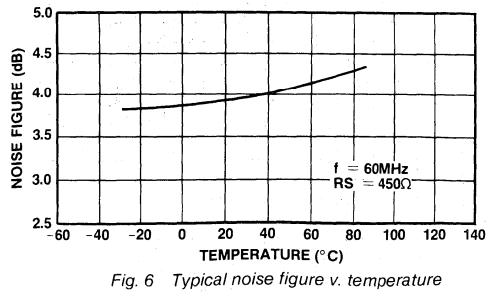


Fig. 6 Typical noise figure v. temperature

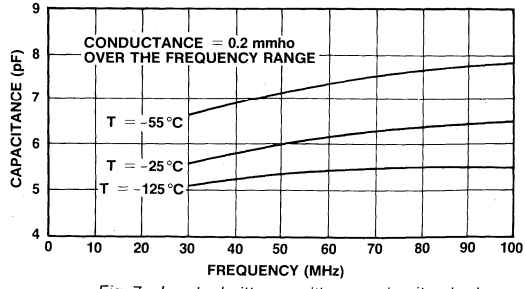


Fig. 7 Input admittance with open circuit output

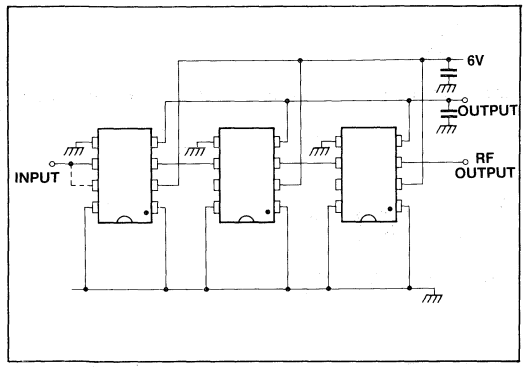


Fig. 8 Direct coupled amplifiers

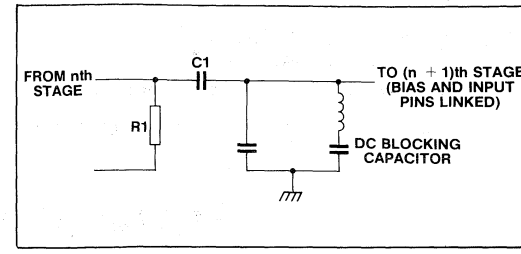


Fig. 9 Suitable interstage tuned circuit

OPERATING NOTES

The amplifiers are intended for use directly coupled, as shown in Fig. 8.

The seventh stage in an untuned cascade will be giving virtually full output on noise.

Noise may be reduced by inserting a single tuned circuit in the chain. As there is a large mismatch between stages a simple shunt or series circuit cannot be used. The choice of network is also controlled by the need to avoid distorting the logarithmic law; the network must give unity voltage transfer at resonance. A suitable network is shown in Fig. 9. The value of C1 must be chosen so that at resonance its admittance equals the total loss conductance across the tuned circuit. Resistor R1 may be introduced to improve the symmetry of filter response, providing other values are adjusted for unity gain at resonance.

A simple capacitor may not be suitable for decoupling the output line if many stages and fast rise times are required.

Values of positive supply line decoupling capacitor required for untuned cascades are given below. Smaller values can be used in high frequency tuned cascades.

The amplifiers have been provided with two earth leads to avoid the introduction of common earth lead inductance between input and output circuits. The equipment designer should take care to avoid the subsequent introduction of such inductance.

	Number of stages			
	6 or more	5	4	3
Minimum capacitance	30nf	10nF	3nF	1nF

The 500pF supply decoupling capacitor has a resistance of, typically, 10Ω. It is a junction type having a low breakdown voltage and consequently the positive supply current will increase rapidly if the supply voltage exceeds 7.5V (See Absolute Maximum Ratings).

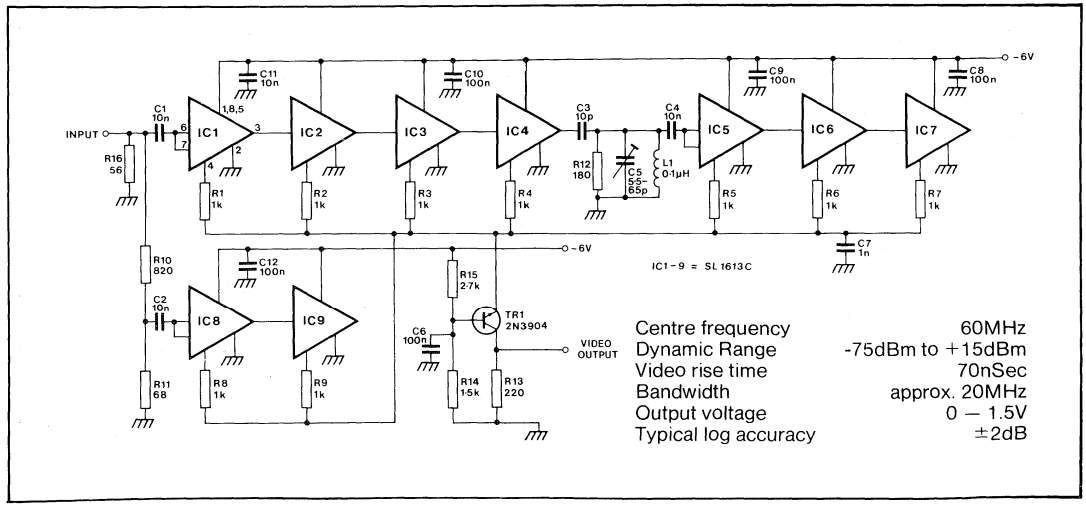


Fig. 10 Circuit diagram of low cost strip

PLESSEY
Semiconductors

SL1640C IS FOR MAINTENANCE PURPOSES ONLY AND IS NOT RECOMMENDED FOR NEW DESIGNS

SL1640C & SL1641C

DOUBLE BALANCED MODULATORS

The SL1640C and SL1641C are double balanced modulators intended for use in radio systems at frequencies up to 75MHz. The SL1640 has an integral output load resistor (Pin 5) together with an emitter follower output (Pin 6) whereas the SL1641 has a single output designed as a current drive to a tuned circuit.

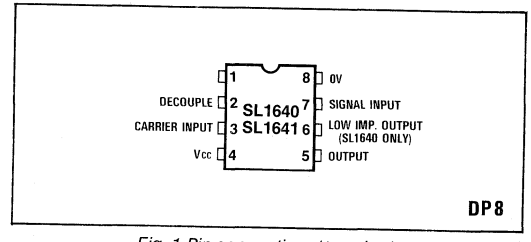


Fig. 1 Pin connections (top view)

FEATURES

- No External Bias Networks Needed
- Easy Interfacing
- Choice of Voltage or Current Outputs

APPLICATIONS

- Mixers In Radio Transceivers
- Phase Comparators
- Modulators

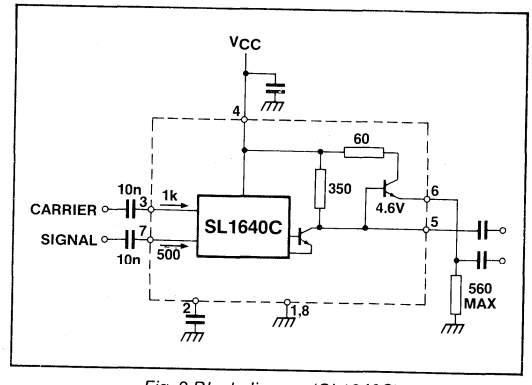


Fig. 2 Block diagram (SL1640C)

QUICK REFERENCE DATA

- Supply Voltage: 6V
- Conversion Gain: 0dB
- Maximum Inputs: 200mV rms

ABSOLUTE MAXIMUM RATINGS

Supply voltage 9V
Storage temperature: −55°C to +125°C

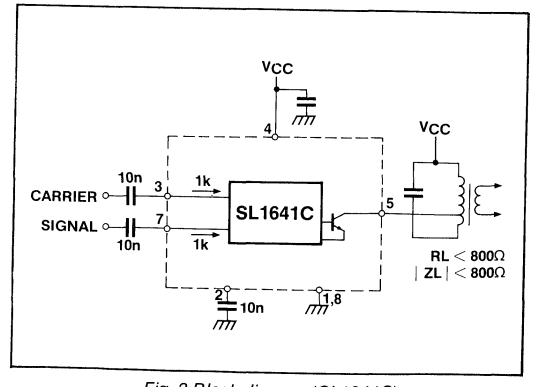


Fig. 3 Block diagram (SL1641C)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage V_{CC}: 6V
Ambient temperature: −30°C to +85°C

Characteristic	Circuit	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	SL1640C		12	18	mA	
	SL1641C		10	15	mA	
Conversion gain	SL1640C	−3	0	+3	dB	
Conversion transconductance	SL1641C	1.7	2.5	3.5	mmho	
Noise figure			10		dB	
Carrier input impedance			1		kΩ	
Signal input impedance	SL1640C		500		Ω	
	SL1641C		1		kΩ	
Maximum input voltage	SL1640C		210		mV rms	
	SL1641C		250		mV rms	
Signal leak	SL1640C		−30		dB	Signal: 70mV rms, 1.75MHz Carrier: 100mV rms, 28.25 MHz Output: 30MHz
Carrier leak	SL1640C		−30		dB	
Signal leak	SL1641C		−18		dB	Signal: 70mV rms, 30MHz Carrier: 100mV rms, 28.25 MHz Output: 1.75MHz
Carrier leak	SL1641C		−25		dB	
Intermodulation products	SL1640C		−45		dB	Signal1: 42.5mV rms, 1.75MHz Signal2: 42.5mV rms, 2MHz Carrier: 100mV rms, 28.25MHz Output: 29.75MHz
	SL1641C		−45		dB	Signal1: 42.5mV rms, 30MHz Signal2: 42.5mV rms, 31MHz Carrier:100mV rms, 28.25MHz Output: 2.75MHz

APPLICATION NOTES

The SL1640C and SL1641C require input and output coupling capacitors which normally should be chosen to present a low reactance compared with the input and output impedances (see Electrical Characteristics). However, for minimum carrier leak at high frequencies the signal input should be driven from a low impedance source, in which case the signal input capacitor reactance should be comparable with the source impedance. Pin 2 must be decoupled to earth via a capacitor which presents the lowest possible impedance at both carrier and signal frequencies. The presence of these frequencies at Pin 2 would give rise to poor rejection figures and to distortion.

The output of the SL1641C is an open collector. If both sidebands are developed across the load its dynamic impedance must be less than 800 ohms. If only one sideband is significant this may be raised to 1600 ohms and it may be further raised if the maximum input swing of 200mV rms is not used. The DC resistance of the load should not exceed 800 ohms. If the circuit is connected to a +6V supply and the load impedance to +9V, the load may be increased to 1.8 kilohms at AC or DC. This, of course increases the gain of the circuit.

There are two outputs from the SL1640C; one is a voltage source of output impedance 350 ohms and 8pF and the other is the emitter of an emitter follower connected to the first output. The output on pin 6 requires a discrete load resistor of not less than 1500 ohms to ground. The emitter follower output should not be used to drive capacitive loads as emitter followers act as detectors under such circumstances with resultant distortion and harmonic generation. Frequency-shaping components may be connected to the voltage output and the shaped signal taken from the emitter follower.

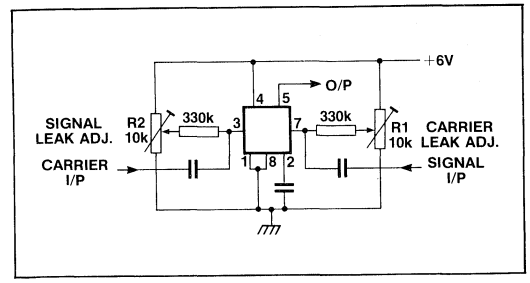


Fig. 4 Signal and carrier leak adjustment

Signal and carrier leak may be reduced by altering the bias on the carrier and signal input pins, as shown in Fig.4. With carrier but no signal R1 is adjusted for minimum carrier leak. A similar network is connected to the carrier input and with signal and carrier present, signal leak is minimised by means of R2.

PLESSEY
Semiconductors

SL2363C & SL2364C

VERY HIGH PERFORMANCE TRANSISTOR ARRAYS

The SL2363C and SL2364C are arrays of transistors internally connected to form a dual long-tailed pair with tail transistors. They are monolithic integrated circuits manufactured on a very high speed bipolar process which has a minimum useable f_T of 2.5GHz, (typically 5GHz).

The SL2363 is in a 10 lead TO5 encapsulation.

The SL2364 is in a 14 lead DIL plastic encapsulation and a high performance Dilmon encapsulation.

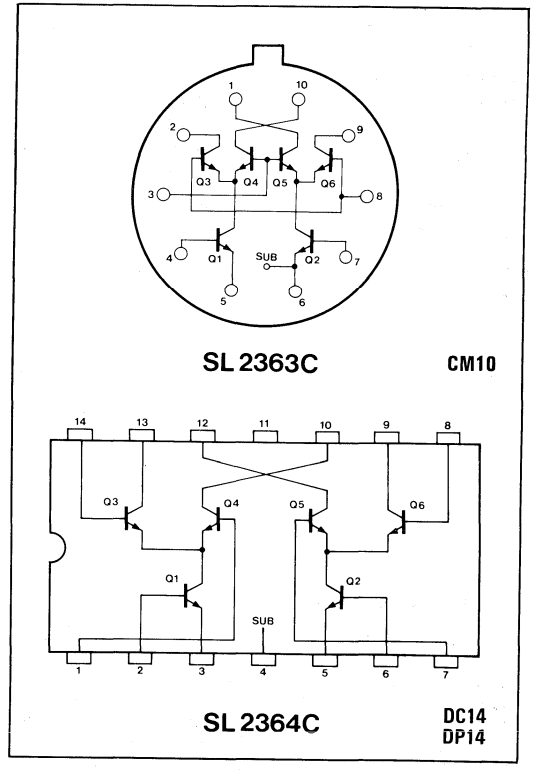


Fig. 1 Pin connections (top view)

FEATURES

- Complete Dual Long-Tailed Pair in One Package.
- Very High f_T – Typically 5 GHz
- Very Good Matching Including Thermal Matching

APPLICATIONS

- Wide Band Amplification Stages
- 140 and 560 MBit PCM Systems
- Fibre Optic Systems
- High Performance Instrumentation
- Radio and Satellite Communications

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ±2°C

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{CBO}	10	20		V	I_C = 10µA
LV_{CEO}	6	9		V	I_C = 5mA
BV_{EBO}	2.5	5.0		V	I_E = 10µA
BV_{CIO}	16	40		V	I_C = 10µA
h_{FE}	50	80			I_C = 8mA, V_{CE} = 2V
f_T	2.5	5		GHz	I_C (Tail) = 8mA, V_{CE} = 2V
ΔV_{BE} (See note 1)		2	5	mV	I_C (Tail) = 8 mA, V_{CE} = 2V
$\Delta V_{BE}/T_{AMB}$		-1.7		mV/° C	I_C (Tail) = 8 mA, V_{CE} = 2V
C_{CB}		0.5	0.8	pF	V_{CB} = 0
C_{CI}		1.0	1.5	pF	V_{CI} = 0

NOTE 1. ΔV_{BE} applies to $|V_{BEQ3} - V_{BEQ4}|$ and $|V_{BEQ5} - V_{BEQ6}|$

TYPICAL CHARACTERISTICS

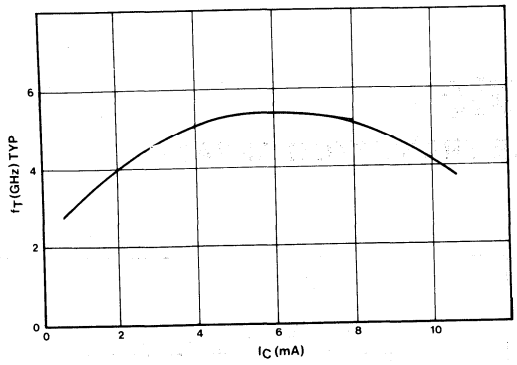


Fig. 2 Collector current

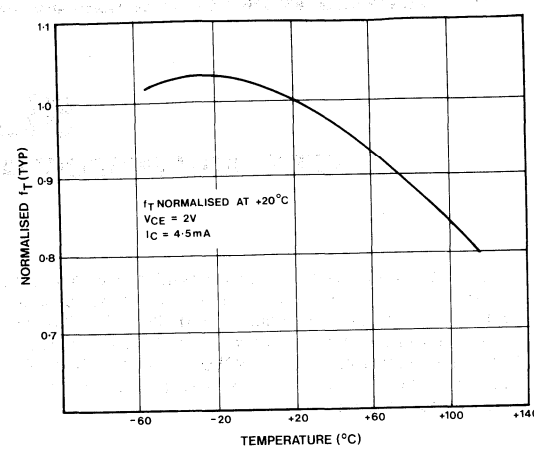


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature	−55°C to +150°C
Maximum junction temperature	+150°C

Package thermal resistance (°C/W):

Chip to case 65 (CM10)

Chip to ambient 225 (CM10) 175 (DP14)

V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

PLESSEY
Semiconductors

SL2365

VERY HIGH PERFORMANCE TRANSISTOR ARRAY

The SL2365 is an array of transistors internally connected to form a dual long-tail pair with current mirrors whose bases and collectors are connected internally. The ICs are manufactured on a very high speed bipolar process, which has a minimum usable f_T of 2.5GHz (typically 5GHz). The current mirror enables a well defined gain at low current levels to be achieved.

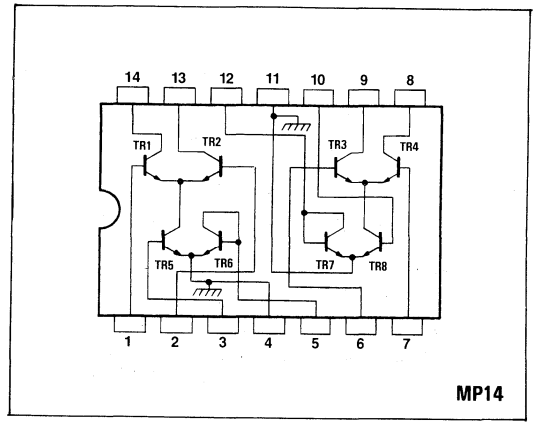


Fig.1 Pin connections - top view

FEATURES

- Complete Dual Long Tailed Pair in One Package
- Very High f_T - Typically 5GHz
- Well Defined Gain at Low Current Levels
- Available in Small Outline Package

ELECTRICAL CHARACTERISTICS

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
BV_{cbo}	10	20		V	$I_C = 10\mu A$
LV_{ceo}	6	9		V	$I_C = 5mA$
BV_{ebo}	2.5	5		V	$I_E = 10\mu A$
BV_{cio}	16	40		V	$I_C = 10\mu A$
H_{fe}	50	80			$I_C = 8mA$, $V_{ce} = 2V$
f_T	2.5	5		GHz	I_C (tail) $= 8mA$, $V_{ce} = 2V$
ΔV_{be}		2	5	mV	I_C (tail) $= 8mA$, $V_{ce} = 2V$
$\Delta V_{be}/T_{amb}$		-7		mV/°C	I_C (tail) $= 8mA$, $V_{ce} = 2V$
C_{CB}		0.5	0.8	pF	$V_{CB} = 0V$
C_{CI}		1.0	1.5	pF	$V_{CI} = 0V$

TYPICAL CHARACTERISTICS

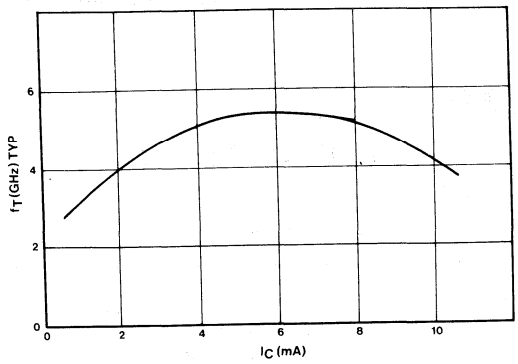


Fig. 2 Collector current

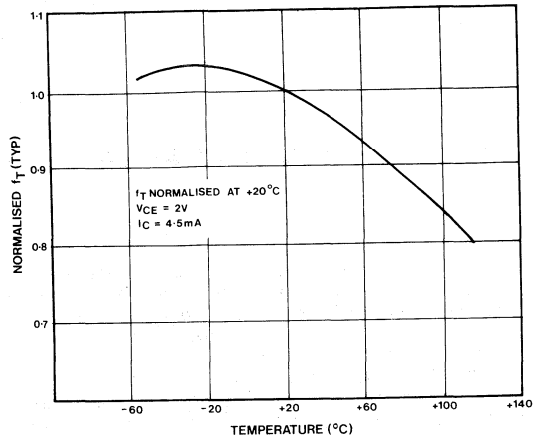


Fig. 3 Chip temperature

ABSOLUTE MAXIMUM RATINGS

Maximum individual transistor dissipation 200mW

Storage temperature −55°C to +150°C
Maximum junction temperature +150°C
Package thermal resistance (°C/W):
Chip to case 65 (CM10)
Chip to ambient 225 (CM10) 175 (DP14)
V_{CBO} = 10V, V_{EBO} = 2.5V, V_{CEO} = 6V, V_{CIO} = 15V, IC (any one transistor) = 20mA

The substrate should be connected to the most negative point of the circuit to maintain electrical isolation between the transistors.

SL2521B

1.3GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm 1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

The device is also available as the SL2522BC which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

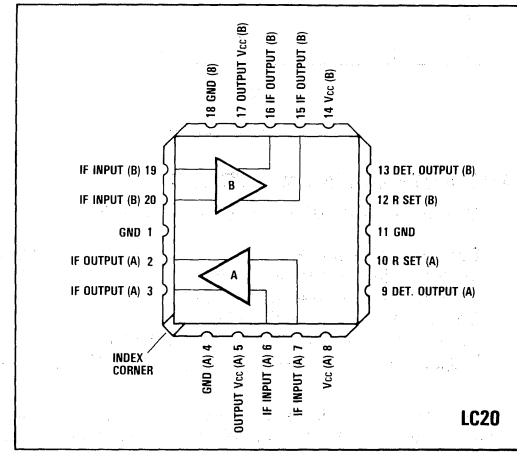


Fig.1 Pin connections - top view

FEATURES

- 1.3GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperature Stabilised
- Full Military Temperature Range/Surface Mountable

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

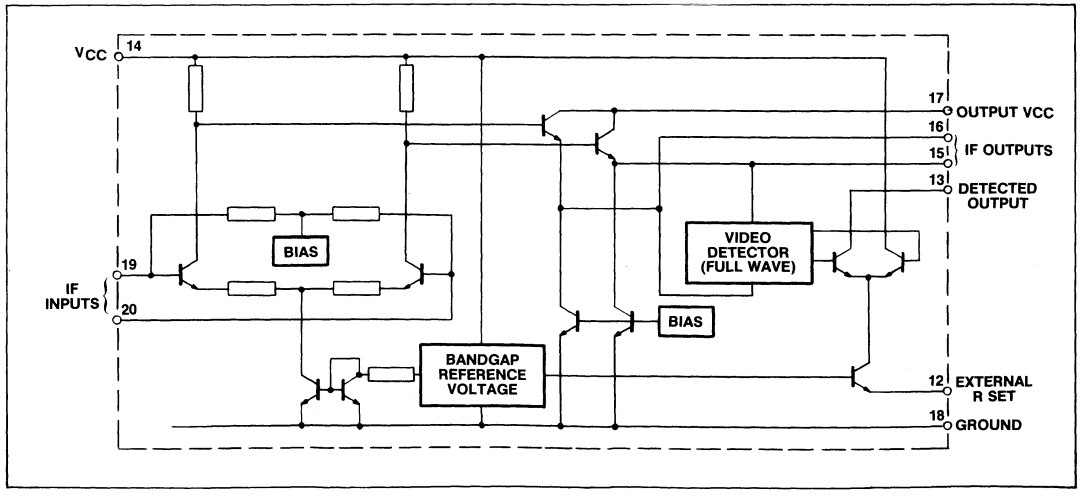


Fig.2 Circuit diagram (single stage B only)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 200MHz, T_{amb} = -30°C to +85°C, Input voltage = -30dBm, V_{CC} = 6V ± 0.1V, Source Impedance = 50Ω, Test Circuit = Fig.3, R_{set} = 300Ω. Tested as a dual stage.

Characteristics	Value						Units	Conditions	Notes
	50Ω Load			1kΩ Load					
	Min.	Typ.	Max.	Min.	Typ.	Max.			
Small signal gain (dual stage, single ended)	9.2	10.7	12.2	14.8	16.5	18.3	dB	T_{amb} = -30°C frequency = 200MHz	2
	9.8	11.0	12.2	15.8	17.0	18.2	dB	T_{amb} = +25°C frequency = 200MHz	
	9.7	11.2	12.4	15.8	17.3	18.8	dB	T_{amb} = +85°C frequency = 200MHz	2
	9.9	11.5	13.2	16.1	18.1	20.1	dB	T_{amb} = -30°C frequency = 500MHz	2
	10.2	11.4	12.7	16.3	18.0	19.8	dB	T_{amb} = +25°C frequency = 500MHz	
	9.7	11.2	12.7	15.6	17.6	19.6	dB	T_{amb} = +85°C frequency = 500MHz	2
Detected output current (max)	3.05	3.25	3.45	3.20	3.45	3.70	mA	T_{amb} = -30°C,V_{in} = 0dBm,f = 200MHz	2
	3.15	3.3	3.45	3.30	3.5	3.70	mA	T_{amb} = +25°C,V_{in} = 0dBm,f = 200MHz	
	3.10	3.3	3.50	3.30	3.55	3.80	mA	T_{amb} = +85°C,V_{in} = 0dBm,f = 200MHz	2
	2.8	3	3.2	2.8	3	3.2	mA	T_{amb} = -30°C,V_{in} = 0dBm,f = 500MHz	2
	2.9	3.05	3.2	2.8	3	3.2	mA	T_{amb} = +25°C,V_{in} = 0dBm,f = 500MHz	
	2.85	3.03	3.25	2.8	3	3.2	mA	T_{amb} = +85°C,V_{in} = 0dBm,f = 500MHz	2
Detected output current (no signal)				0.9	1.1	1.3	mA	T_{amb} = -30°C	2
				0.95	1.1	1.25	mA	T_{amb} = +25°C	
				0.9	1.1	1.3	mA	T_{amb} = +85°C	2
Upper cut off frequency (RF)				900	1100		MHz	-3dB w.r.t. 200MHz,T_{amb} = +25°C	1
Lower cut off frequency (RF)					0.35	1	MHz		
Detector cut off frequency					700		MHz	50% O/P current w.r.t. 200MHz	
Limited IF O/P voltage				105	120	145	mV	I/P voltage = 0dBm,T_{amb} = +25°C	
Phase variation with input level (normalised to -30dBm)		±2	±3				Degree	Frequency = 70MHz, -55 to +3dBm	
		±2	±3				Degree	Frequency = 200MHz, -55 to +3dBm	
Limited O/P var with temp.		±12	±25				mV		
Noise figure		12			9		dB		
Max I/P before overload					15		dBm		
Input impedance					1		kΩ	1kΩ in parallel with 2pF	
Output impedance					40		Ω		
Supply current					75	90	mA		
Variation of max detected current with V_{CC}					5		%/V	T_{amb} = +25°C	
Variation of small signal gain with V_{CC}					0.5		dB/V	T_{amb} = +25°C	

NOTES
1. Parameter guaranteed but not tested.
2. Tested at 25°C only, but guaranteed at temperature.

GENERAL DESCRIPTION

The SL2521 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See Figs.4 and 5.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of <±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{set} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (no video filter). The video bandwidth for a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 7° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

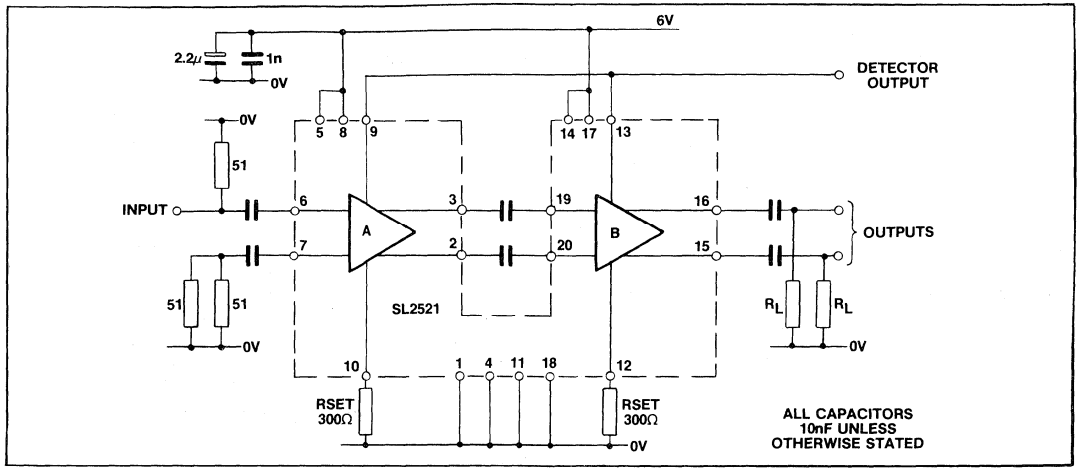


Fig.3 Test circuit

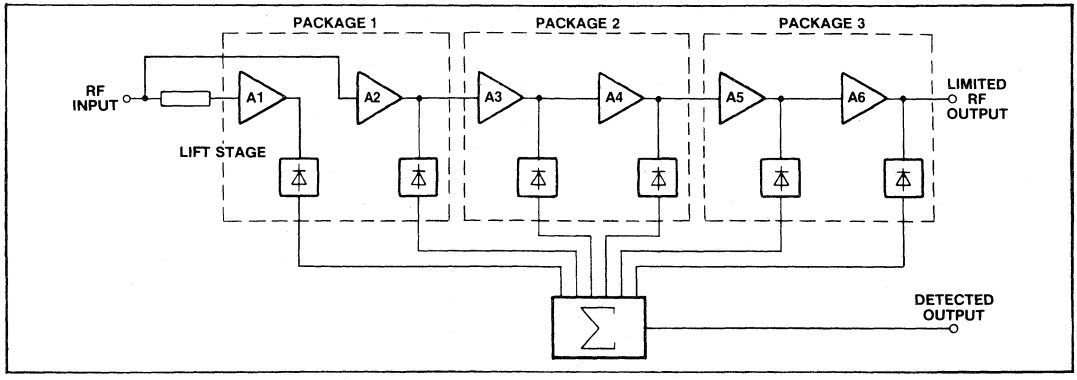


Fig.4 Schematic diagram showing configuration of SD amplifier

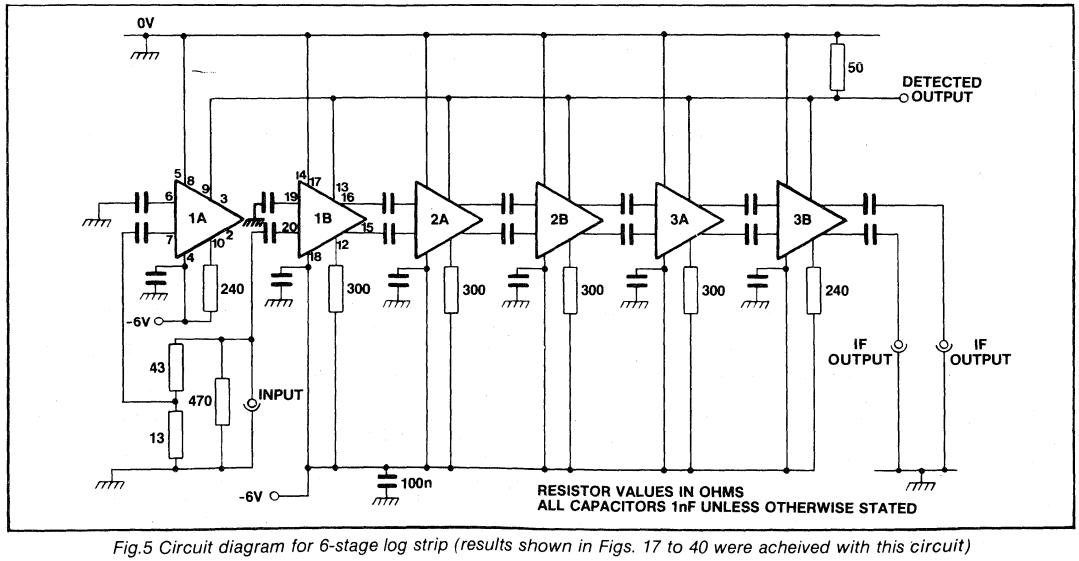


Fig.5 Circuit diagram for 6-stage log strip (results shown in Figs. 17 to 40 were acheived with this circuit)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER (i.e. 1 SL2521)

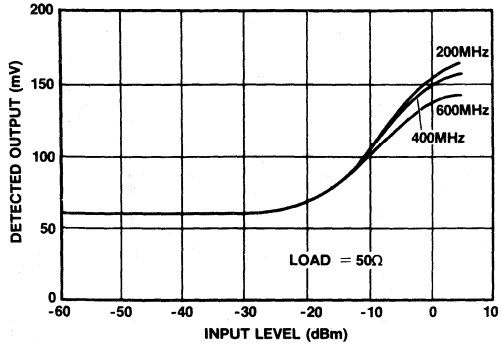


Fig.6 Detected O/P Vs input level at 200,400,600MHz for $R_L = 50\Omega$

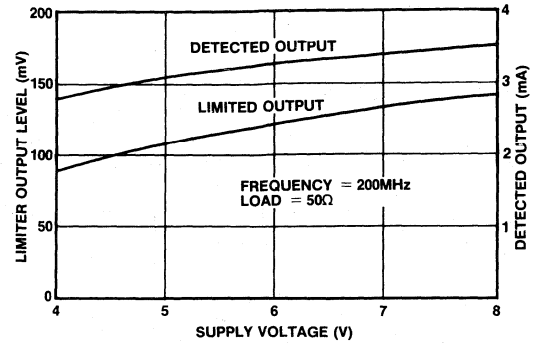


Fig.7 Output levels Vs supply voltage

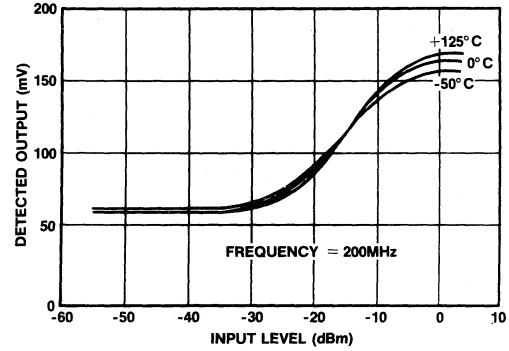


Fig.8 Detected output Vs input level and temperature

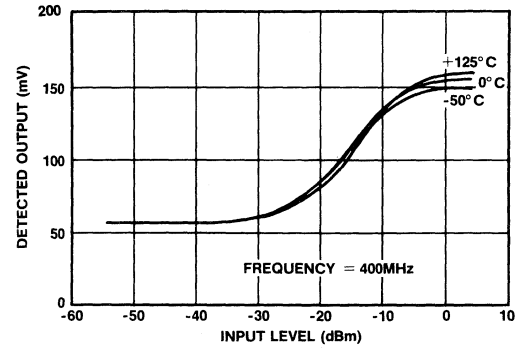


Fig.9 Detected output Vs input level and temperature

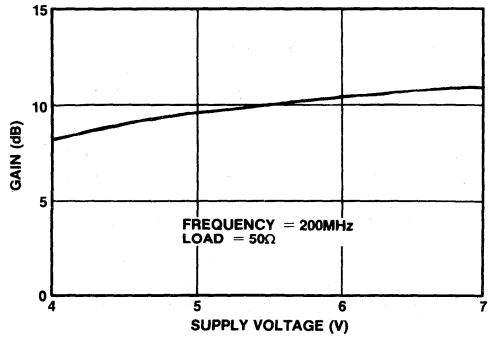


Fig.10 Gain Vs supply voltage

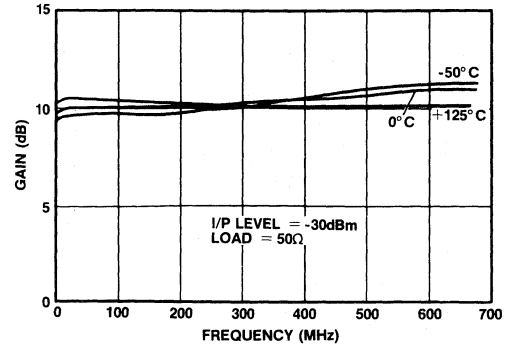


Fig.11 Gain Vs frequency of 2 amplifiers (1 SL2521)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER

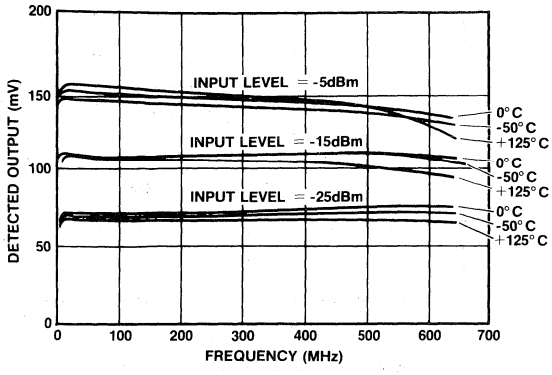


Fig.12 Detected output level Vs frequency and temperature

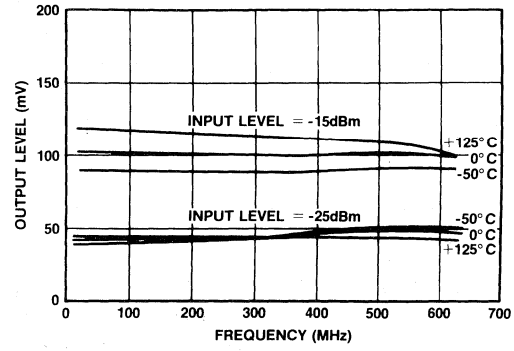


Fig.13 Limited output level Vs frequency and temperature

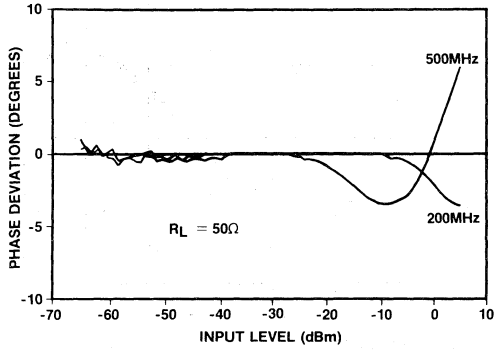


Fig.14 Normalised phase Vs input level at 200 and 500MHz for $R_L = 50\Omega$

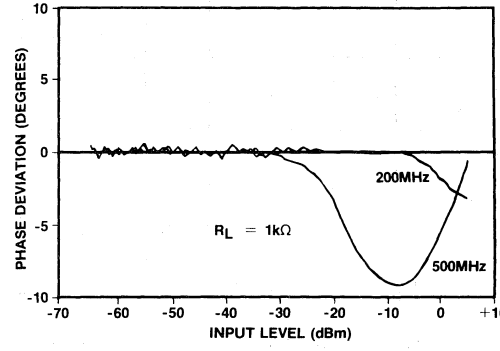


Fig.15 Normalised phase Vs input level at 200 and 500MHz for $R_L = 1k\Omega$

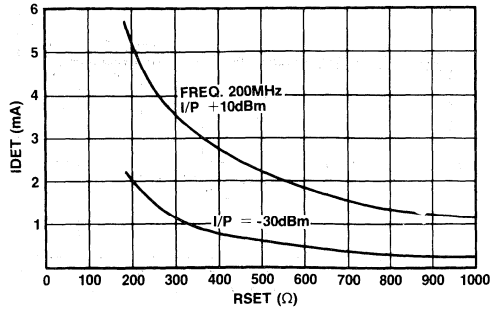


Fig.16 Detector current Vs R_{set} at 200MHz

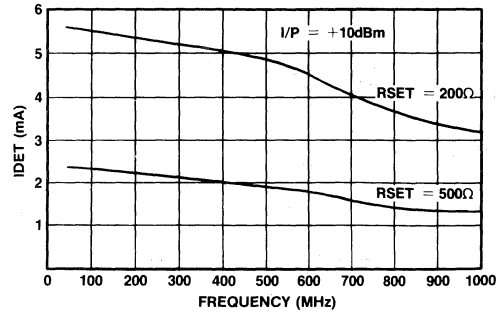


Fig.17 Detector current Vs frequency at $R_{set} = 200\Omega$ and 500Ω

TYPICAL CHARACTERISTICS FOR A SIX STAGE STRIP, USING THE VIDEO OUTPUT

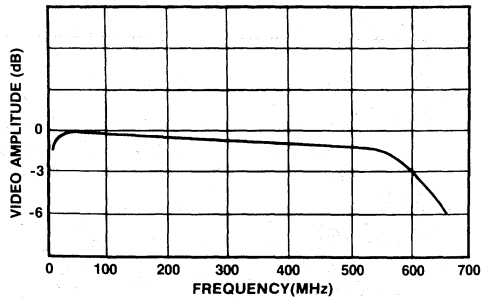


Fig.18 Video bandwidth (detector)

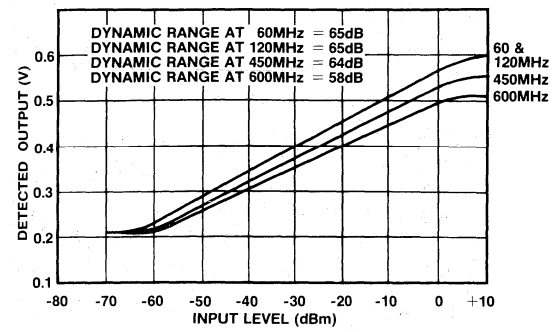


Fig.19 Video output Vs CW input at 60, 120, 450 and 600MHz at 25° C

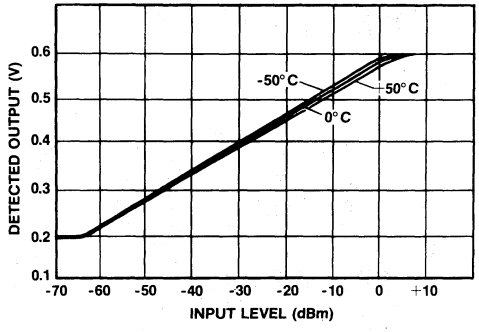


Fig.20 Detected output Vs input level and temperature at 60, 120MHz

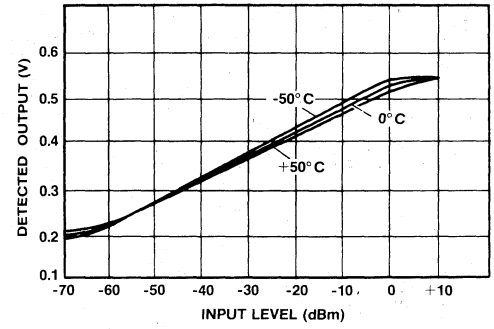


Fig.21 Detected output Vs input level and temperature at 450MHz

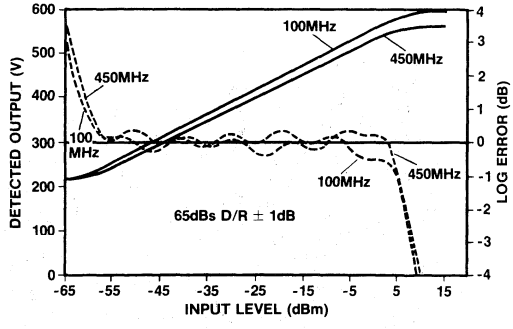


Fig.22 Detected O/P and log linearity at 450 and 100MHz

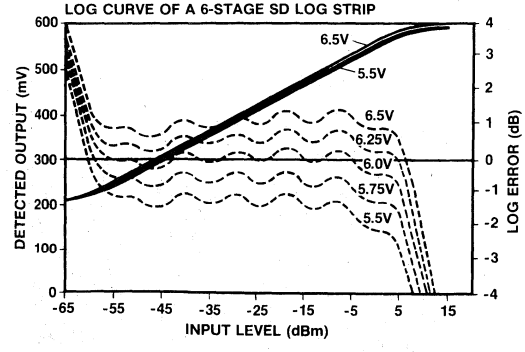


Fig.23 Logarithmic output Vs V_{CC}

SL2521: PULSE FIDELITY FOR A SIX STAGE STRIP

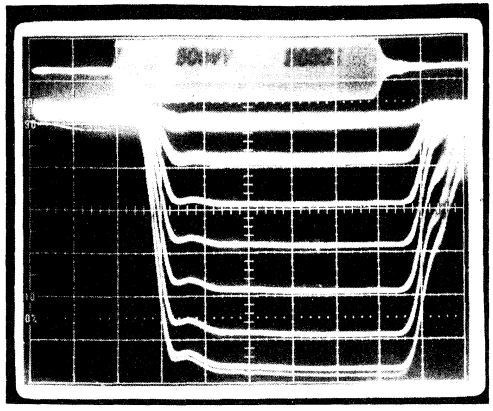


Fig.24 60ns I/P pulse. With low pass video filter. Horizontal = 10ns/div. Vertical = 50mV/div. Input level -70dBm to -10dBm

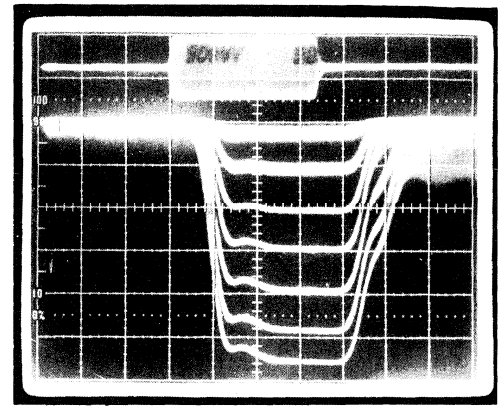


Fig.25 As Fig.25 with 35ns input pulse (Slight glitch on front edge is due to underdamping of video filter)

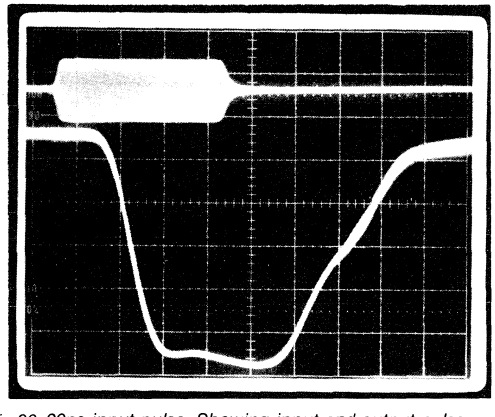


Fig.26 20ns input pulse. Showing input and output pulse with low pass video filter. Horizontal = 5ns/div. Vertical = 50mV/div; -10dBm input.

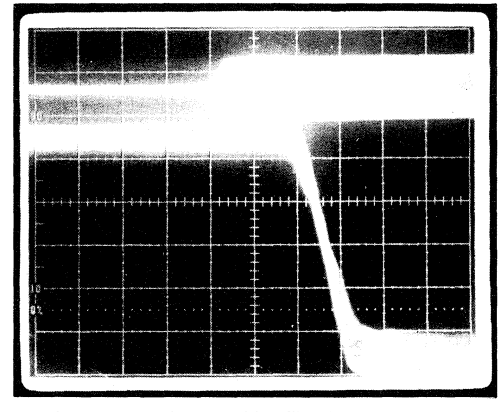


Fig.27 20ns input pulse. No video filter leading edge only. Horizontal = 2ns/div; -10dBm input level.

SL2521: LIMITING CHARACTERISTICS

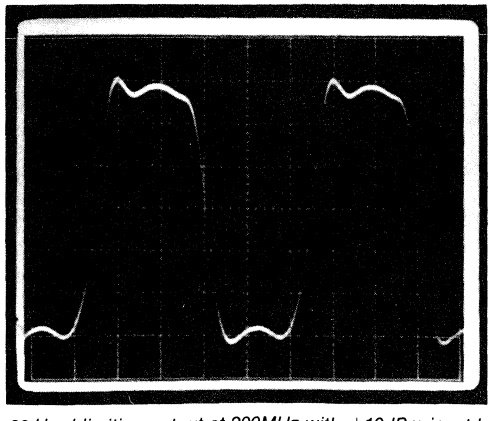


Fig.28 Hard limiting output at 200MHz with +10dBm input level

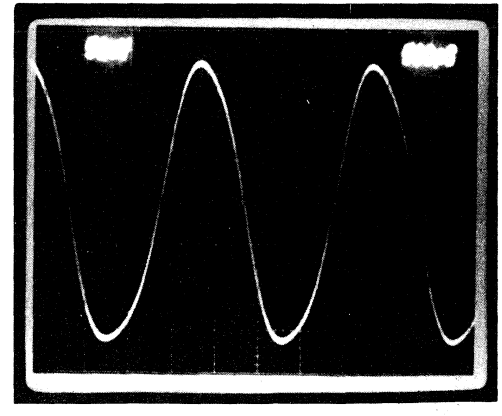


Fig.29 Hard limiting output at 500MHz with +10dBm input level

TYPICAL CHARACTERISTICS OF A SIX STAGE STRIP AS A LOW PHASE SHIFT WIDEBAND LIMITER

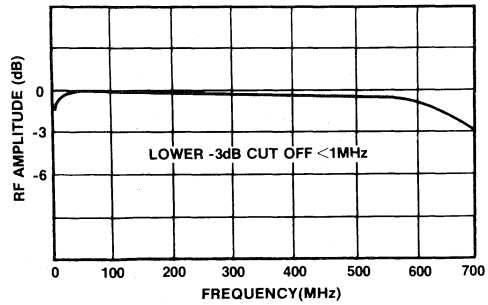


Fig.30 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

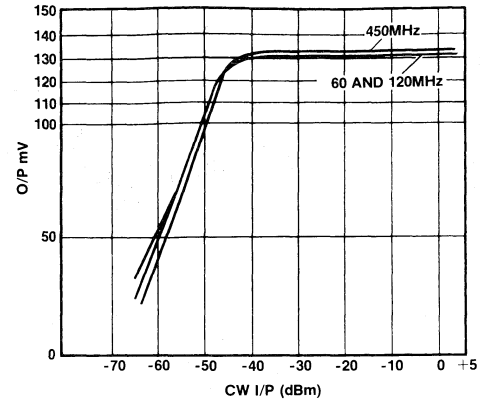


Fig.31 IF limiting characteristic at 60, 120 and 450MHz

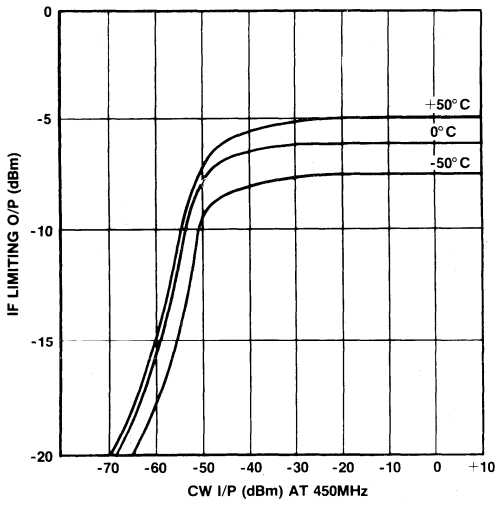


Fig.32 Limiting characteristic Vs temperature at 450MHz

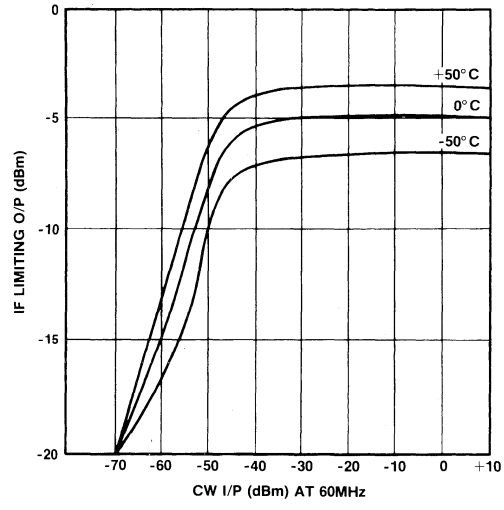


Fig.33 Limiting characteristic Vs temperature at 60MHz

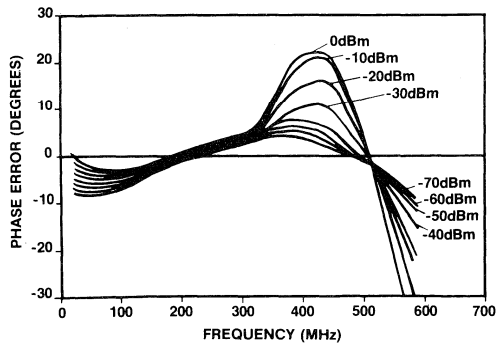


Fig.34 Departure from linear phase

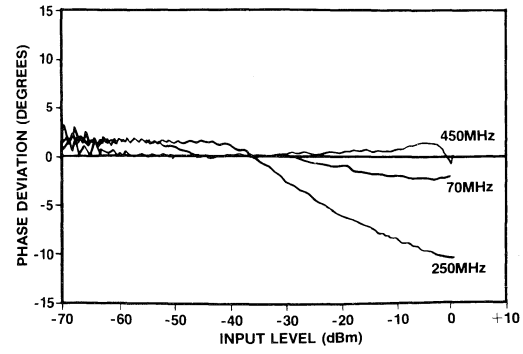


Fig.35 Normalised phase Vs input level

WIDEBAND LIMITER CHARACTERISTICS

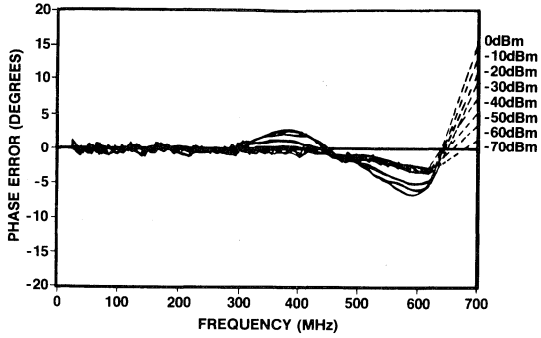


Fig.36 Phase tracking Vs frequency of two SD log strips (typical)

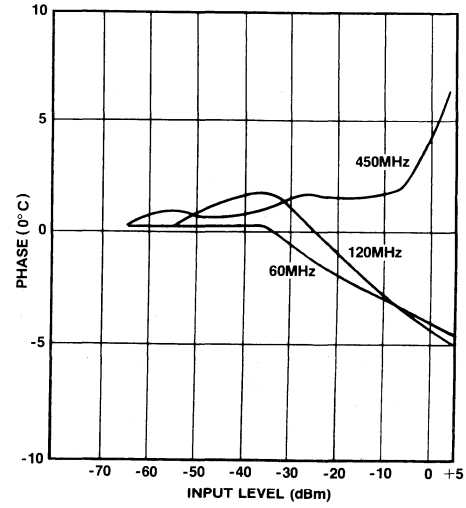


Fig.37 Phase change Vs input level at 60, 120 and 450MHz

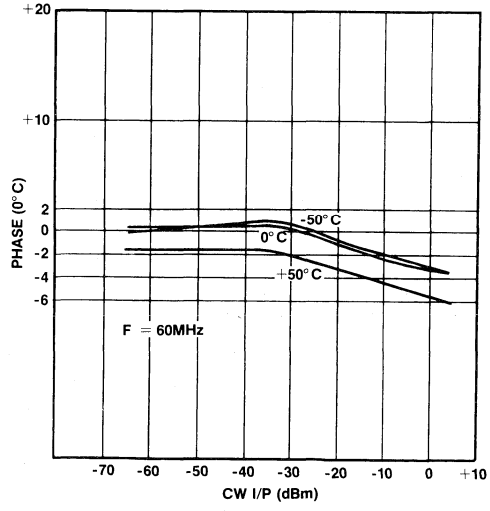


Fig.38 Phase change Vs temperature at 60MHz

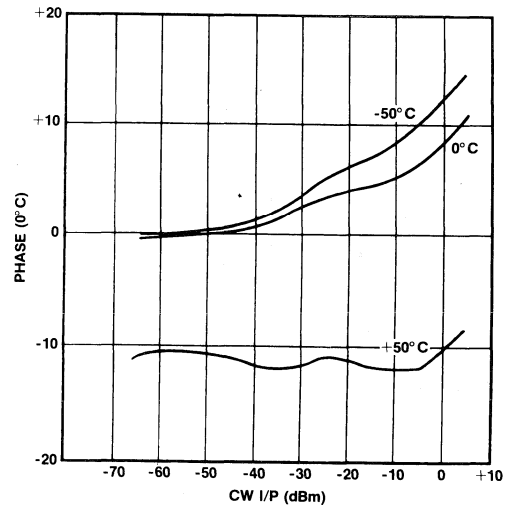


Fig.39 Phase change Vs temperature at 450MHz

IMPEDANCE OR ADMITTANCE CO-ORDINATES

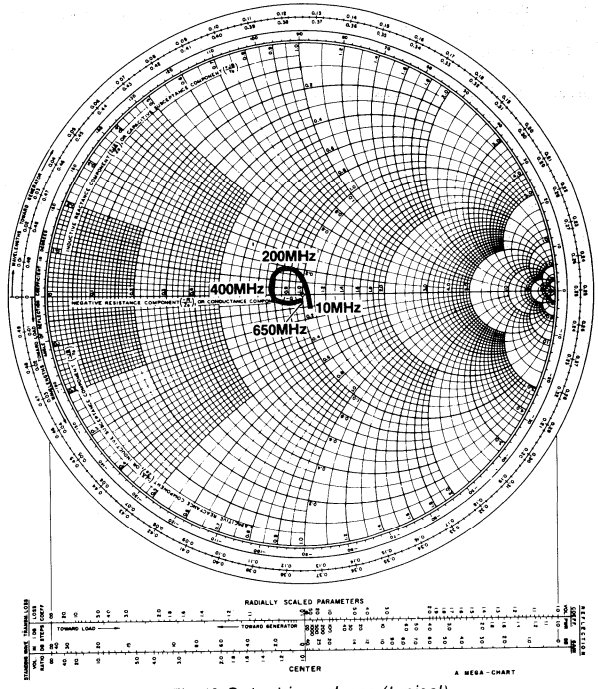


Fig.40 Output impedance (typical)

IMPEDANCE OR ADMITTANCE CO-ORDINATES

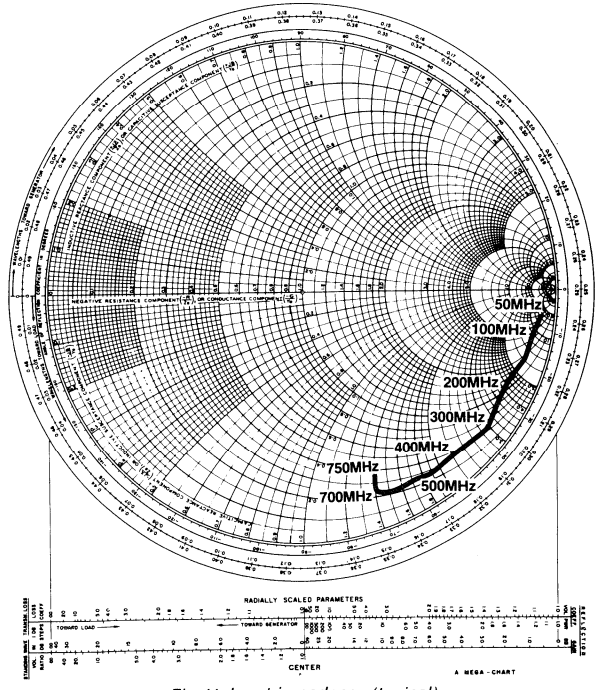


Fig.41 Input impedance (typical)

FUTURE DEVELOPMENTS

The SL2521B is guaranteed for operation over the temperature range -30 °C to +85 °C. A second selection will be offered with tighter limits on gain and detected output current. This will be designated the SL2521A.

For full Military operation an SL2522B will be offered. This will be guaranteed for operation over the temperature range -55 °C to +125 °C.

Quality

All standard product i.e. the SL2521B is visually inspected to MIL-STD-883 Method 2010, and assembled in accordance with the rules as defined in the MIL-883 Handbook.

Screening to e offered will be to:

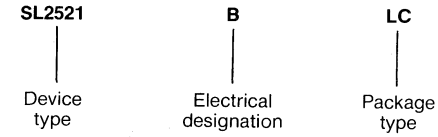
MIL-STD-883C Level B
Customer Procured Specifications

Please enquire for latest status of all variants.

RADIATION HARD PRODUCT

Information available on request.

ORDERING INFORMATION



I.E:-

SL2521 B LC -30 °C to +85 °C guaranteed.
SL2522 BC LC -55 °C to +125 °C with MIL-883C screening.

PLESSEY
Semiconductors

SL2521C

1.0GHz DUAL WIDEBAND LOGARITHMIC AMPLIFIER

The SL2521 is a revolutionary monolithic integrated circuit designed on an advanced 3 micron oxide isolated bipolar process. The amplifier is a successive detection type which provides linear gain and accurate logarithmic signal compression over a wide bandwidth.

When six stages (three SL2521s) are cascaded the strip can be used for IFs between 30-650MHz whilst achieving greater than 65dB dynamic range with a log accuracy of $<\pm 1.0$dB. The balanced limited output also offers accurate phase information with input amplitude. One log strip therefore offers limited IF output, phase and video information.

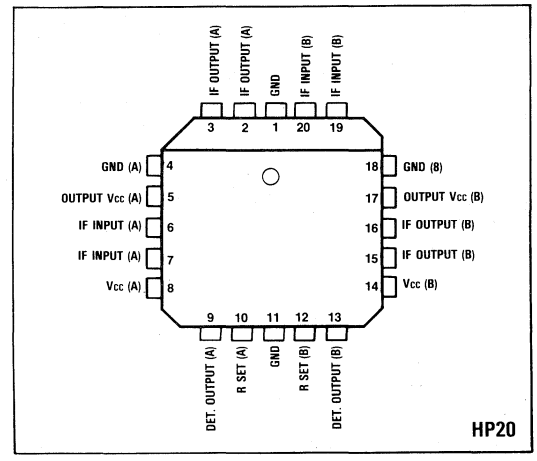


Fig.1 Pin connections - top view

FEATURES

- 1.0GHz Bandwidth (-3dB)
- Balanced IF Limiting
- 3ns Rise Times/5ns Fall Times (Six Stages)
- 20ns Pulse Handling (Six Stages)
- Temperture Stabilised
- Surface Mountable

APPLICATIONS

- Ultra Wideband Log Receivers
- Channelised Receivers
- Monopulse Applications

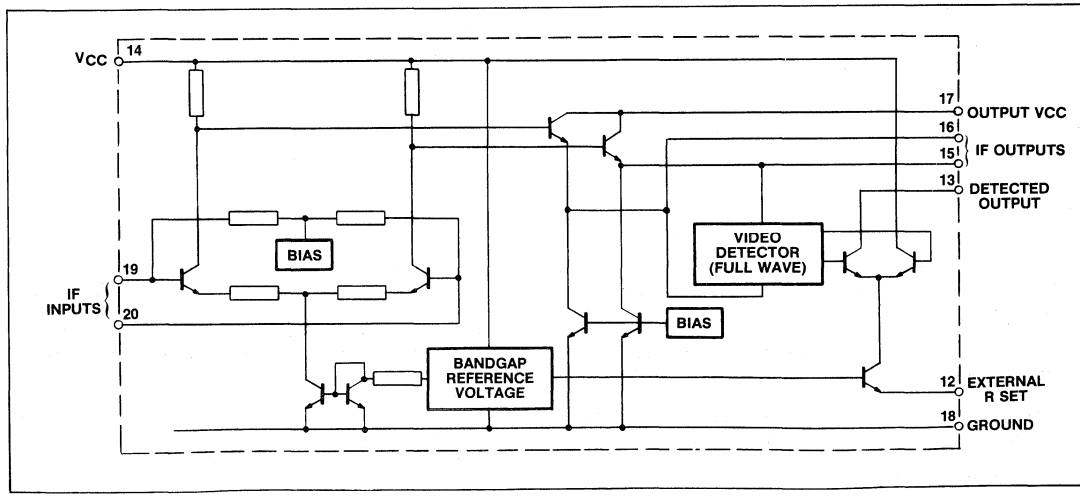


Fig.2 Circuit diagram (single stage B only)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Frequency = 200MHz, T_{amb} = -30°C to +85°C, Input voltage = -30dBm, V_{CC} = 6V ± 0.1V, Source Impedance = 50Ω, Test Circuit = Fig.3, R_{set} = 300Ω.

Characteristics	Value						Units	Conditions	Notes
	50Ω Load			1kΩ Load					
	Min.	Typ.	Max.	Min.	Typ.	Max.			
Small signal gain (dual stage, single ended)	8.7	10.7	12.7	14.3	16.5	19.2	dB	T_{amb} = -30°C frequency = 200MHz	2
	9.3	11.0	12.7	15.3	17.0	18.7	dB	T_{amb} = +25°C frequency = 200MHz	
	9.2	11.2	12.9	15.3	17.3	19.3	dB	T_{amb} = +85°C frequency = 200MHz	2
	9.4	11.5	13.7	15.6	18.1	20.6	dB	T_{amb} = -30°C frequency = 500MHz	2
	9.7	11.4	13.2	15.8	18.0	20.3	dB	T_{amb} = +25°C frequency = 500MHz	
	9.2	11.2	13.2	15.1	17.6	20.1	dB	T_{amb} = +85°C frequency = 500MHz	2
Detected output current (max)	2.95	3.25	3.55	3.10	3.45	3.8	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 200MHz	2
	3.05	3.3	3.55	3.2	3.5	3.8	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 200MHz	
	3.0	3.3	3.5	3.2	3.55	3.9	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 200MHz	2
	2.7	3	3.3	2.7	3	3.3	mA	T_{amb} = -30°C, V_{in} = 0dBm, f = 500MHz	2
	2.8	3.05	3.3	2.7	3	3.3	mA	T_{amb} = +25°C, V_{in} = 0dBm, f = 500MHz	
	2.75	3.03	3.35	2.7	3	3.3	mA	T_{amb} = +85°C, V_{in} = 0dBm, f = 500MHz	2
Detected output current (no signal)				0.8	1.2	1.4	mA	T_{amb} = -30°C	2
				0.85	1.2	1.35	mA	T_{amb} = +25°C	
				0.8	1.2	1.4	mA	T_{amb} = +85°C	2
Upper cut off frequency (RF)					1000		MHz	-3dB w.r.t. 200MHz, T_{amb} = +25°C	1
Lower cut off frequency (RF)					0.35	2	MHz		
Detector cut off frequency					600		MHz	50% O/P current w.r.t. 200MHz	
Limited IF O/P voltage				90	120		mV	I/P voltage = 0dBm, T_{amb} = +25°C	
Phase variation with input level (normalised to -30dBm)		±2					Degree	Frequency = 70MHz, -55 to +3dBm	
		±4					Degree	Frequency = 200MHz, -55 to +3dBm	
Limited O/P var with temp.		±12					mV		
Noise figure		12			9		dB		
Max I/P before overload					15		dBm		
Input impedance					1		kΩ	1kΩ in parallel with 2pF	
Output impedance					40		Ω		
Supply current					75	90	mA		
Variation of max detected current with V_{CC}					5		%/V	T_{amb} = +25°C	
Variation of small signal gain with V_{CC}					0.5		dB/V	T_{amb} = +25°C	

NOTES
1. Parameter guaranteed but not tested.
2. Tested at 25°C only, but guaranteed at temperature.

GENERAL DESCRIPTION

The SL2521 is primarily intended for use in Radar and EW receivers. Six stages (3 chip carriers) can be cascaded to form a very wideband logarithmic amplifier offering >65dB of input dynamic range, with pulse handling of better than 25ns. (See Figs.4 and 5.)

A six stage strip also offers balanced IF limiting, linearity (log accuracy) of <±1.0dB, temperature stabilisation and programmable detector characteristics.

The detector has an external resistor set pin which allows the major characteristics of the detector to be programmed. With a six stage strip it is possible to vary the value of R_{set} on each detector and so improve the overall log error/linearity.

The detector is full wave and good slew rates are achieved with 2ns rise and 5ns fall times (nc video filter). The video bandwidth for a six stage strip is typically 600MHz (-3dB).

The amplifier also offers balanced IF limiting, low phase shift versus input amplitude, and at an IF of 120MHz, less than 7° of phase change is achievable over the input level of -55dBm to +5dBm.

The IF and Video ports can be used simultaneously so offering phase, frequency and pulse (video) information. A slight loss of dynamic range (2dB) will be observed when the IF ports are used in conjunction with the video.

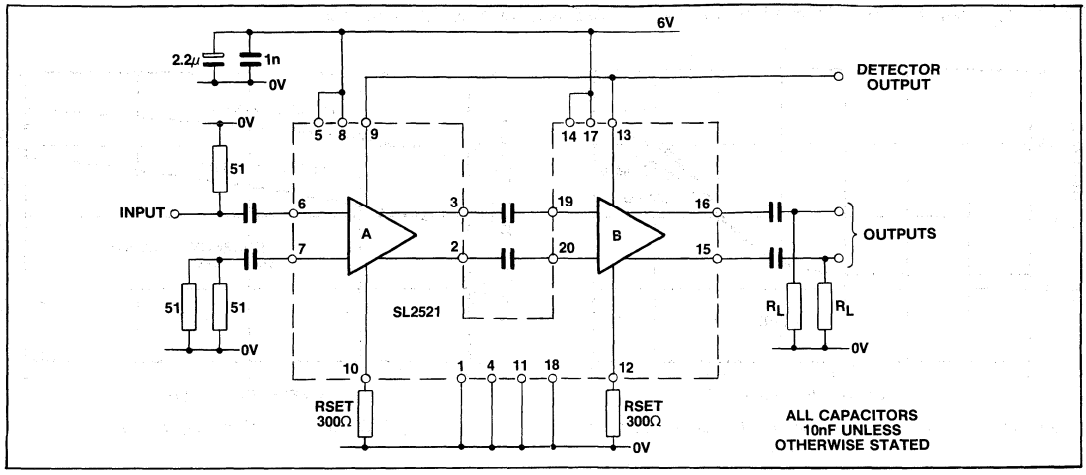


Fig.3 Test circuit

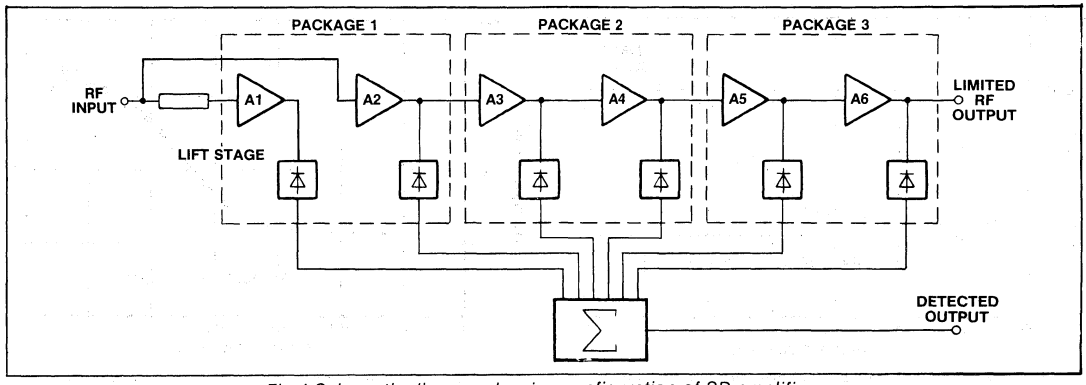


Fig.4 Schematic diagram showing configuration of SD amplifier

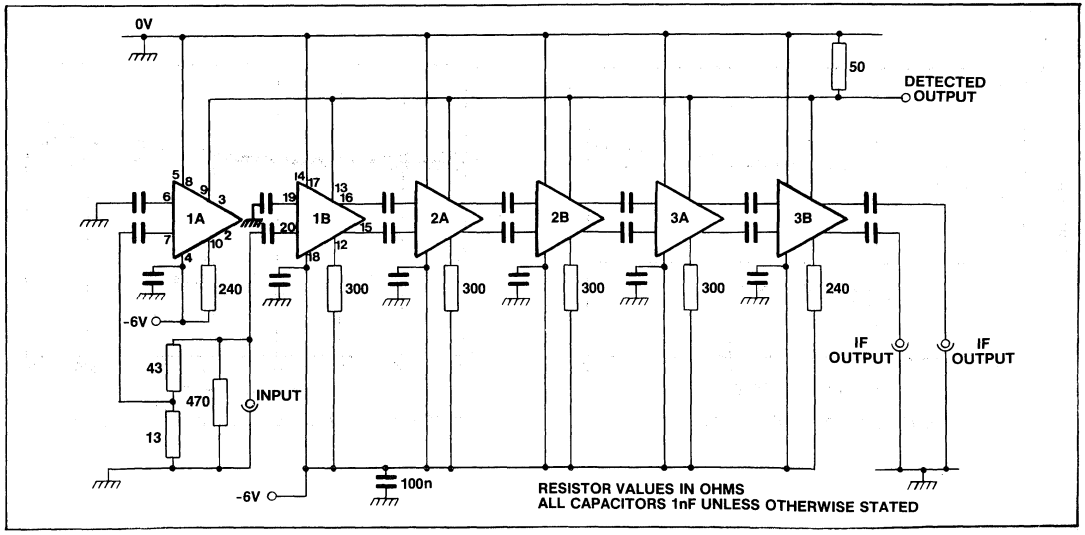


Fig.5 Circuit diagram for 6-stage log strip (results shown in Figs. 17 to 40 were acheived with this circuit)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER (i.e. 1 SL2521)

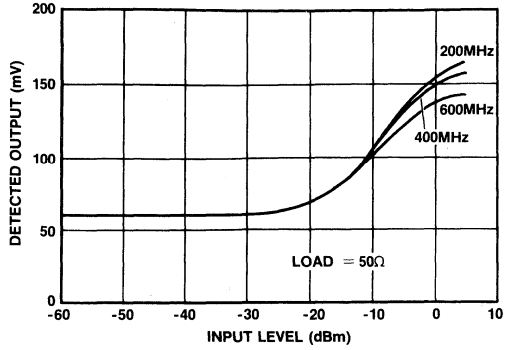


Fig.6 Detected O/P Vs input level at 200,400,600MHz for $R_L = 50\Omega$

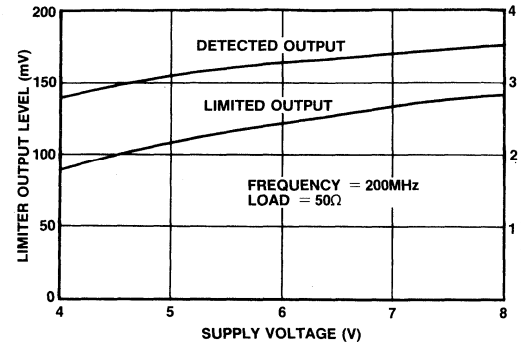


Fig.7 Output levels Vs supply voltage

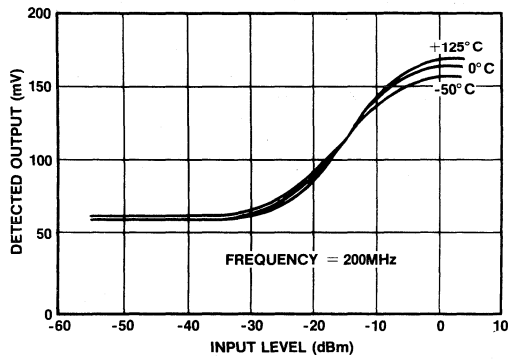


Fig.8 Detected output Vs input level and temperature

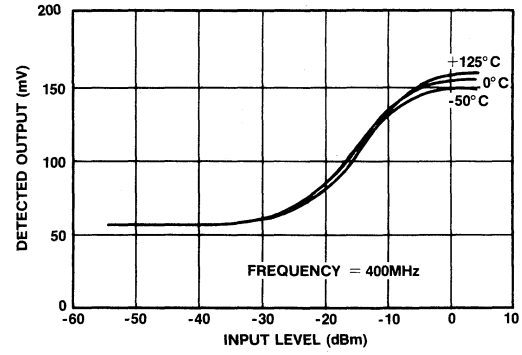


Fig.9 Detected output Vs input level and temperature

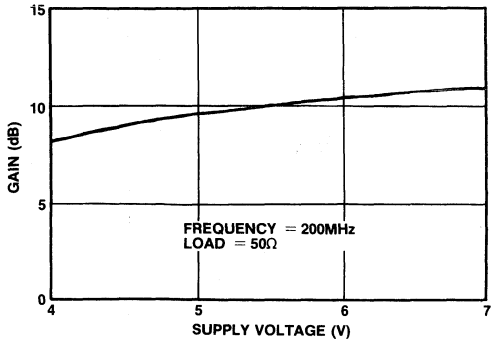


Fig.10 Gain Vs supply voltage

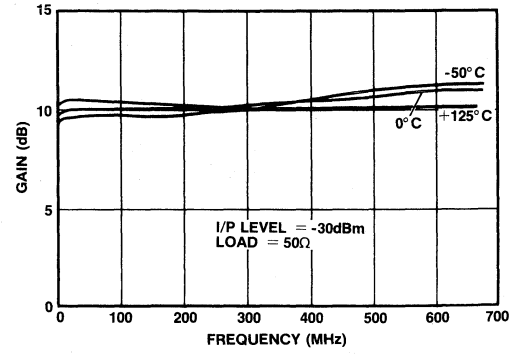


Fig.11 Gain Vs frequency of 2 amplifiers (1 SL2521)

TYPICAL CHARACTERISTICS FOR A DUAL STAGE AMPLIFIER

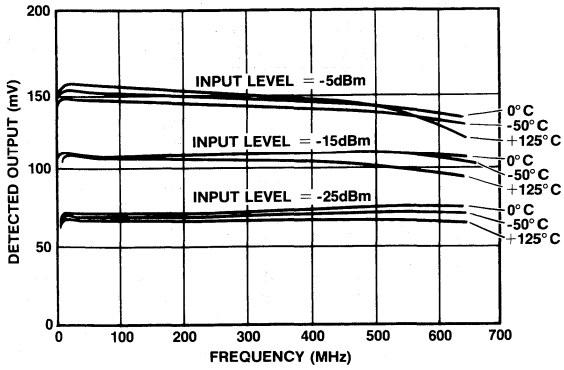


Fig.12 Detected output level Vs frequency and temperature

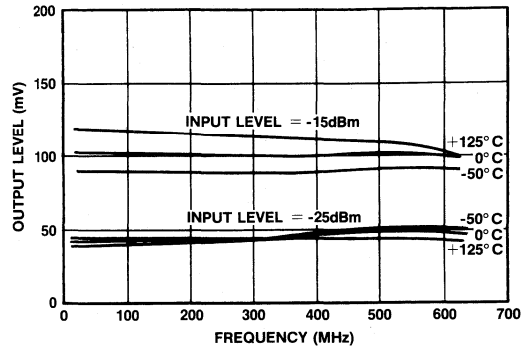


Fig.13 Limited output level Vs frequency and temperature

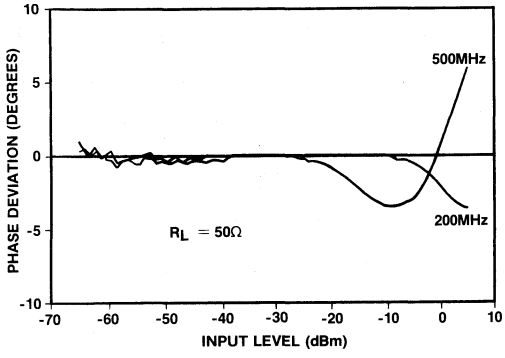


Fig.14 Normalised phase Vs input level at 200 and 500MHz for $R_L = 50\Omega$

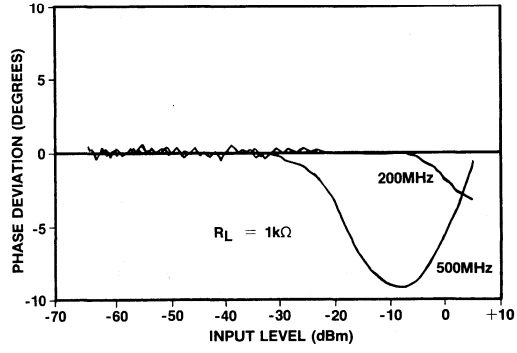


Fig.15 Normalised phase Vs input level at 200 and 500MHz for $R_L = 1k\Omega$

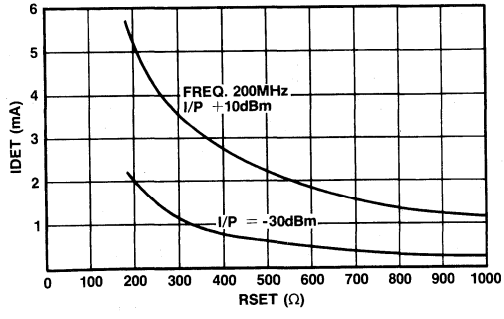


Fig.16 Detector current Vs R_{set} at 200MHz

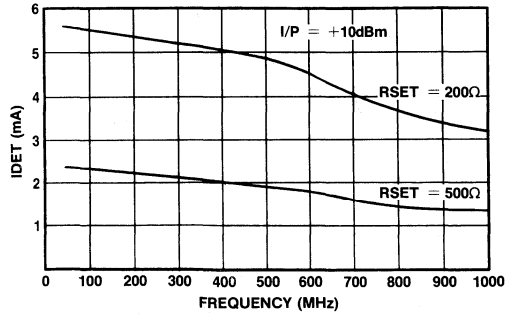


Fig.17 Detector current Vs frequency at $R_{set} = 200\Omega$ and 500Ω

TYPICAL CHARACTERISTICS FOR A SIX STAGE STRIP, USING THE VIDEO OUTPUT

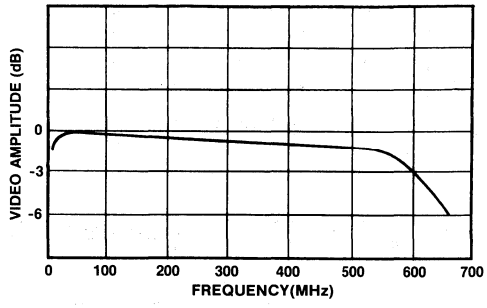


Fig.18 Video bandwidth (detector)

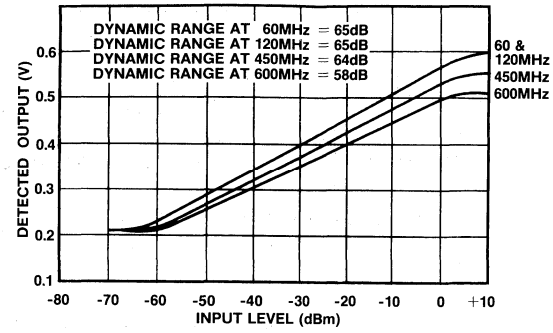


Fig.19 Video output Vs CW input at 60, 120, 450 and 600MHz at 25° C

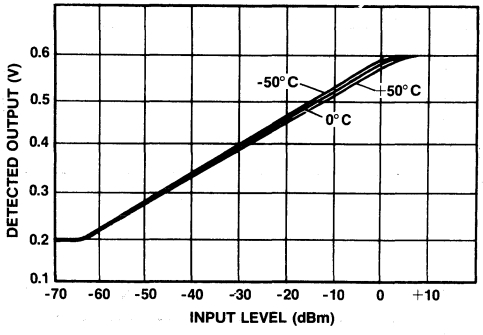


Fig.20 Detected output Vs input level and temperature at 60, 120MHz

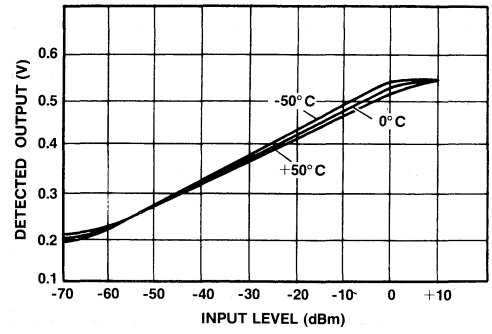


Fig.21 Detected output Vs input level and temperature at 450MHz

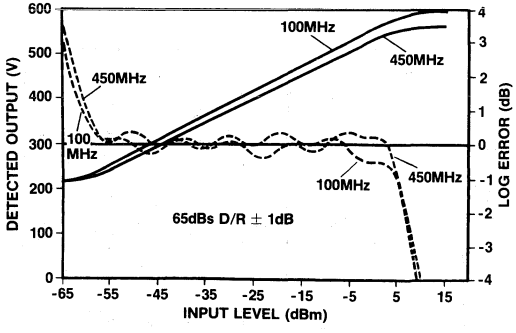


Fig.22 Detected O/P and log linearity at 450 and 100MHz

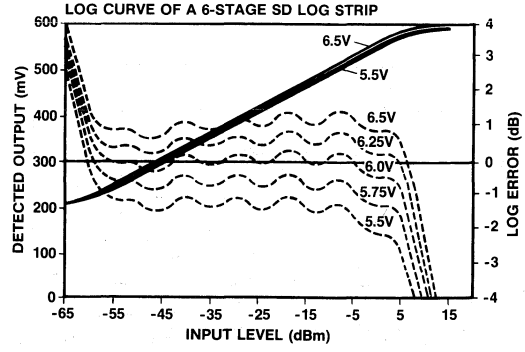


Fig.23 Logarithmic output Vs Vcc

SL2521: PULSE FIDELITY FOR A SIX STAGE STRIP

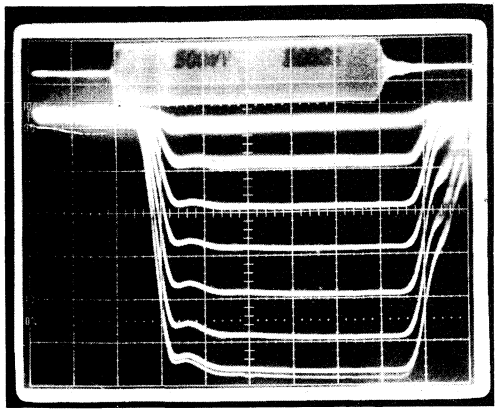


Fig.24 60ns I/P pulse. With low pass video filter. Horizontal = 10ns/div. Vertical = 50mV/div. Input level -70dBm to -10dBm

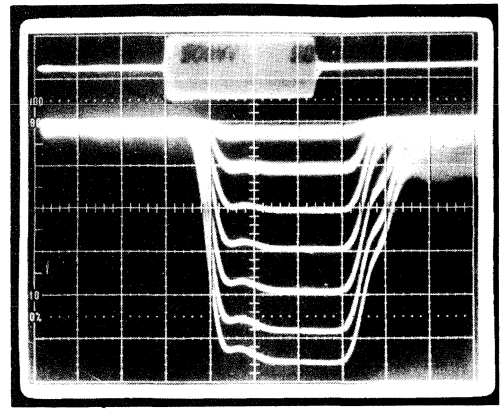


Fig.25 As Fig.25 with 35ns input pulse (Slight glitch on front edge is due to underdamping of video filter)

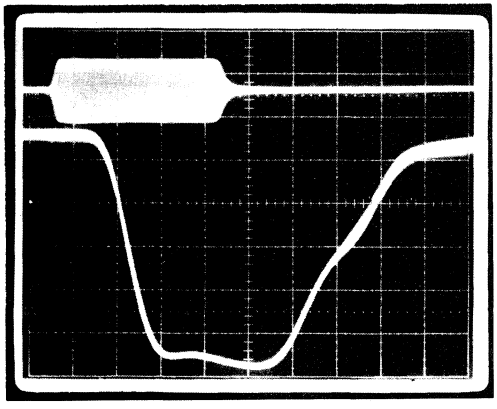


Fig.26 20ns input pulse. Showing input and output pulse with low pass video filter. Horizontal = 5ns/div. Vertical = 50mV/div; -10dBm input.

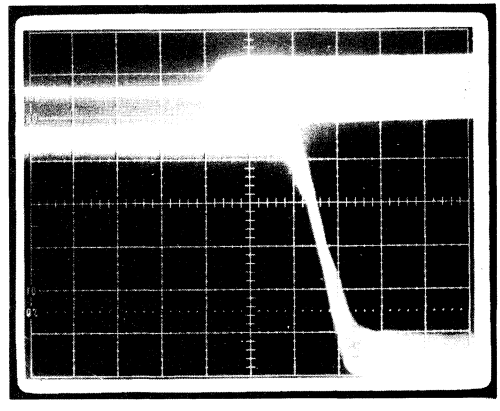


Fig.27 20ns input pulse. No video filter leading edge only. Horizontal = 2ns/div; -10dBm input level.

SL2521: LIMITING CHARACTERISTICS

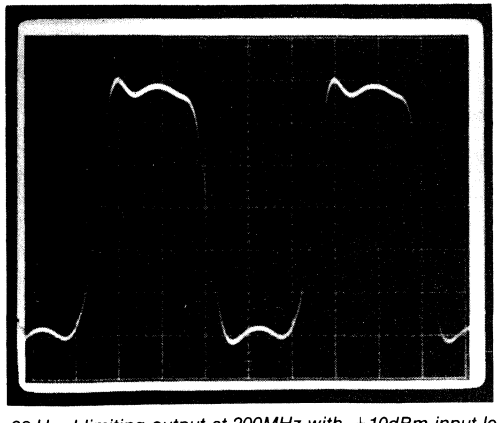


Fig.28 Hard limiting output at 200MHz with +10dBm input level

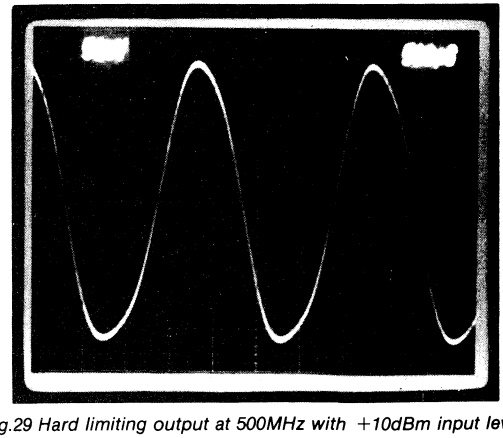


Fig.29 Hard limiting output at 500MHz with +10dBm input level

TYPICAL CHARACTERISTICS OF A SIX STAGE STRIP AS A LOW PHASE SHIFT WIDEBAND LIMITER

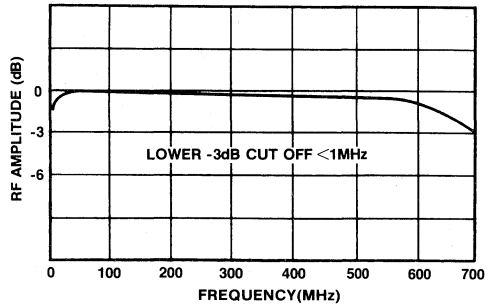


Fig.30 IF bandwidth measured from output 1. Output 2 terminated into 50Ω

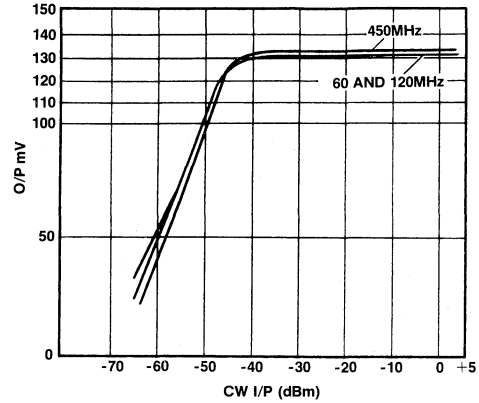


Fig.31 IF limiting characteristic at 60, 120 and 450MHz

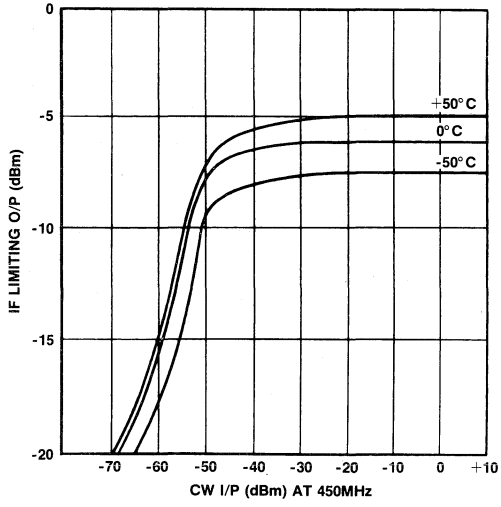


Fig.32 Limiting characteristic Vs temperature at 450MHz

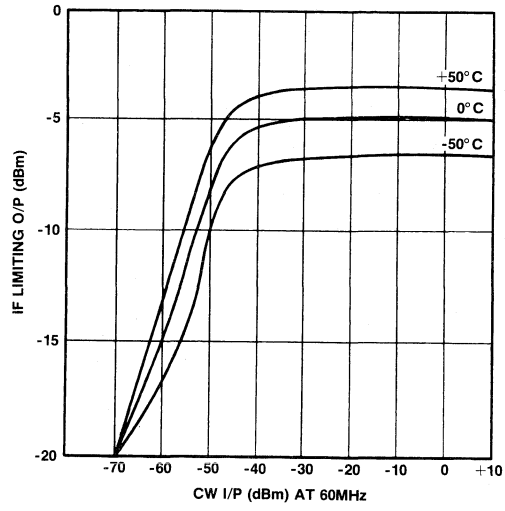


Fig.33 Limiting characteristic Vs temperature at 60MHz

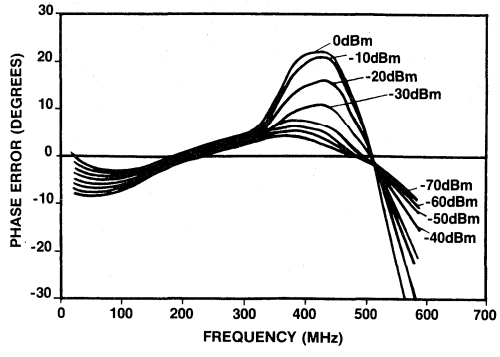


Fig.34 Departure from linear phase

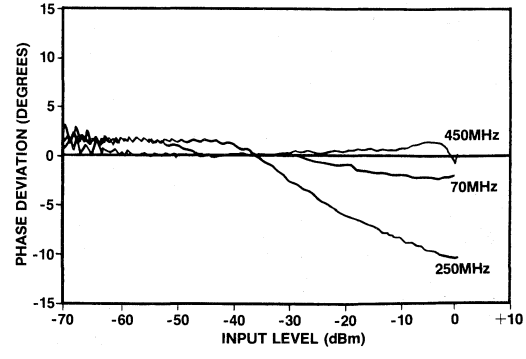


Fig.35 Normalised phase Vs input level

WIDEBAND LIMITER CHARACTERISTICS

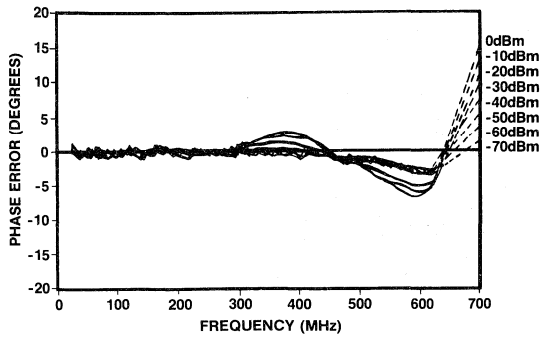


Fig.36 Phase tracking Vs frequency of two SD log strips (typical)

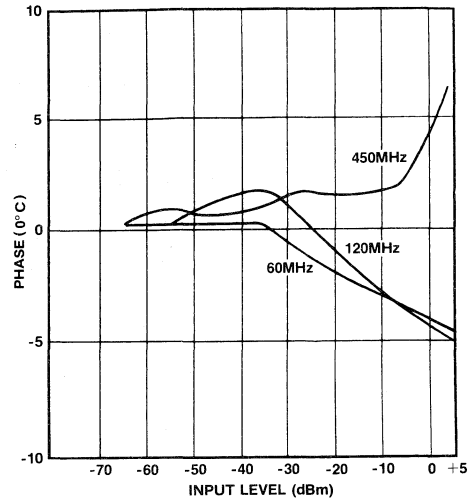


Fig.37 Phase change Vs input level at 60, 120 and 450MHz

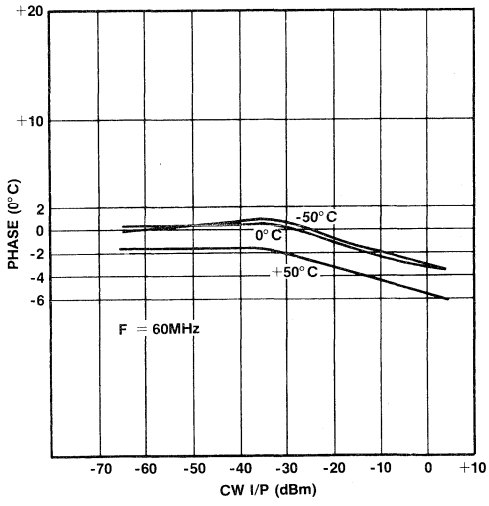


Fig.38 Phase change Vs temperature at 60MHz

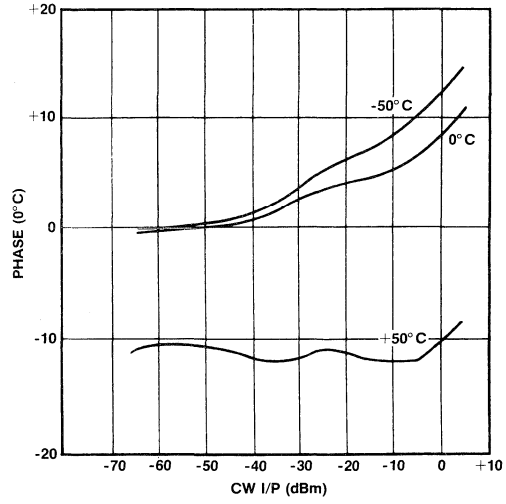


Fig.39 Phase change Vs temperature at 450MHz

IMPEDANCE OR ADMITTANCE CO-ORDINATES

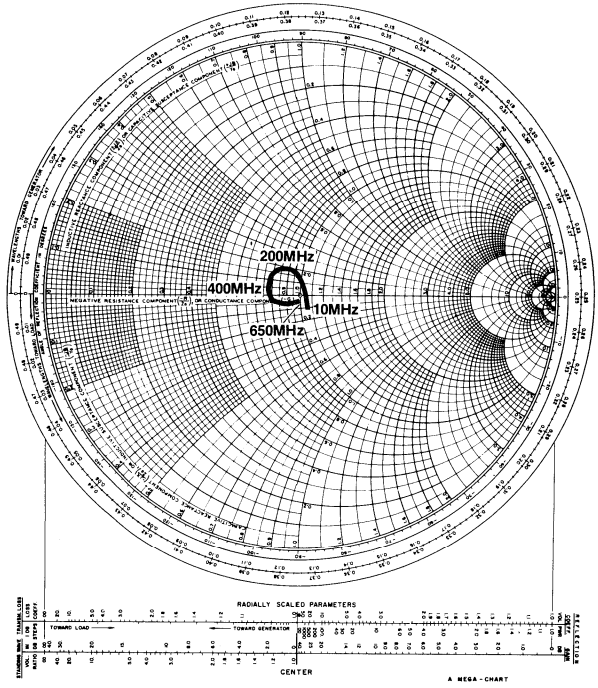


Fig.40 Output impedance (typical)

IMPEDANCE OR ADMITTANCE CO-ORDINATES

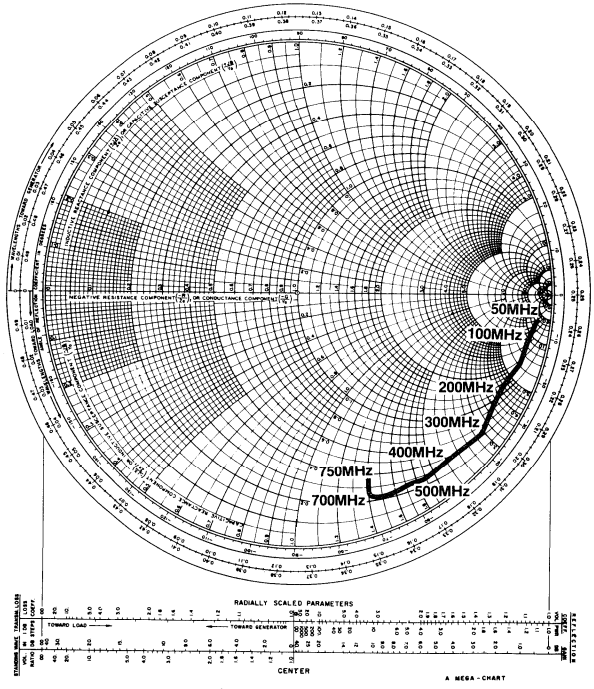


Fig.41 Input impedance (typical)

PLESSEY
Semiconductors

SL2541B

800MHz HIGH SLEW RATE OP-AMP

The Plessey SL2541B combines high slew rate and fast settling times with the flexibility of standard operational amplifier configurations.

To cover the many requirements of high speed op-amp applications the SL2541 has been designed such that many of its important parameters can be externally programmed. These include open loop gain, output current, supply voltage range and output DC offset. Included within the device is a band gap reference for good temperature stability and a separate video speed buffer.

The SL2541 is capable of driving directly into 50Ω with bandwidths in excess of 800MHz.

FEATURES

- 1400/μs Slew Rate (Rising)
- 900V/μs Slew Rate (Falling)
- Fast Settling Time, 30ns to 0.5%
- Full Power Bandwidth of 40MHz
- ±15mA Output Current (Programmable)
- Linear Phase Response

APPLICATIONS

- Radar, Sonar Processors
- Fast Settling Pulse Amplifiers
- Digital and Wideband Analog Communications
- Base Band and Video Communications
- Fast A to D, D to A Conversion

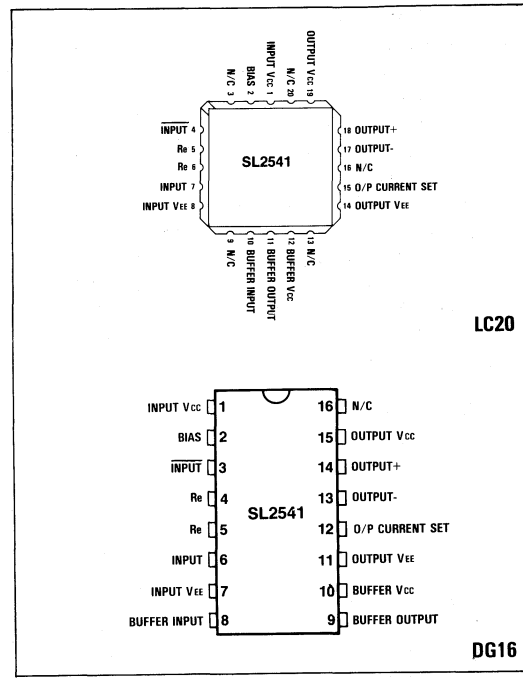


Fig.1 Pin connections - top view

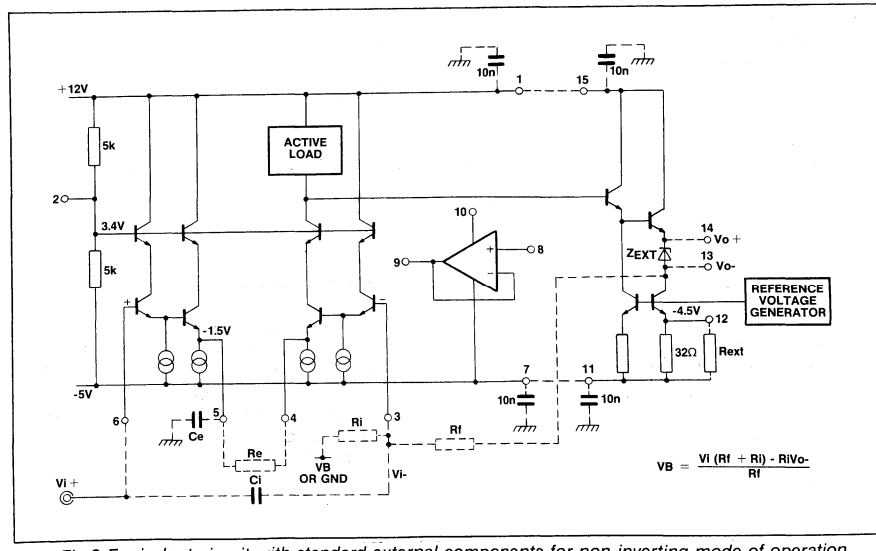


Fig.2 Equivalent circuit with standard external components for non-inverting mode of operation

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 25°C, V_{CC} = +12V, V_{EE} = -5V

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Input characteristics					
Input offset voltage (Note 1)		10		mV	R_L = 1.2kΩ, R_e = 39Ω
Input offset voltage drift		20		μV/°C	R_L = 1.2kΩ, R_e = 390Ω (Note 1)
Input bias current			20	μA	
Input resistance		250		Ω	Open loop impedance at 500MHz
Input capacitance		3.5		pF	(C and R in parallel)
Input signal handling (p-p)			20	V	V_{CC} = +15V, V_{EE} = -15V.See Biasing Conditions.
Transfer characteristics					
Common mode rejection ratio	47			dB	At DC
Gain bandwidth product		2.5		GHz	R_L = 50Ω, V_{out} = 100mV, x10 gain
Open loop gain	45	70		dB	Single ended drive
Non-inverting bandwidth		800		MHz	x2 gain, 50Ω load
Inverting bandwidth		220		MHz	x10 gain, 50Ω load
On-chip buffer bandwidth		60		MHz	R_L = 1kΩ to V_{EE}
Noise figure		8		dB	x2 gain non-inverting, R_S = 50Ω at f = 100MHz
Output characteristics					
Output current		±10	±15	mA	See biasing conditions, programmable
Full power bandwidth		40		MHz	x10 inverting, 10V p-p, R_L = 1.2kΩ
Output resistance		10		Ω	Open loop measurement
Output signal handling (p-p)		-	12	V	V_{CC} = +15V, V_{EE} = -15V
Transient response					
Rise time		1.6		ns	
Fall time		3.2		ns	
Overshoot		10		%	R_L = 1.2kΩ
Slew rate (rising edge)		1400		V/μs	x2 gain non-inverting
Slew rate (falling edge)		900		V/μs	10% to 90% measurement
Settling time to 0.5 %		30		ns	
Settling time to 0.1 %		40		ns	
Power requirements					
Supply voltage V_{EE} to V_{CC}	14		30	V	
Supply voltage range V_{CC}	+9		+15	V	
V_{EE}	-5		-15	V	
Supply current		25		mA	No load, V_{EE} = -5V, V_{CC} = +12V
Power supply rejection ratio		40		dB	
Buffer output current		15		mA	Pull-down resistor required

NOTE
1. Input offset is dependent on R_e. For lowest offset R_e = 10 ohms.

ORDERING INFORMATION

SL2541B DG -30°C to +85°C
SL2541B LC -30°C to +85°C
SL2541AC DG -55°C to +125°C To MIL-883C
SL2541AC LC -55°C to +125°C Class B

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{EE})	35V
Input Voltage (Inv I/P to Non-Inv I/P)	±10V
Storage Temperature	-65°C to +175°C
Chip Operating Temperature	+175°C
Operating Temperature: DIL	-55°C to +125°C
Thermal Resistances:	
Chip-to-Ambient: DIL	125°C/W
Chip-to-Case: DIL	40°C/W

APPLICATION NOTES

The SL2541 may be used as a high frequency, non-saturating amplifier in any of the usual op-amp configurations (amplifiers, integrators). In most applications, the output of the SL2541 is taken from pin 13 ($V_{out}-$), but DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 ($V_{out}+$), see Fig.2. Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to V_B.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give different DC levels at the output.

Biasing Conditions (25° C)

For undistorted outputs the peak signal voltages on Vo +, Vo-, and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geqslant \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leqslant V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geqslant V_{EE} + 1.4V$

D. $Vi+$ and $Vi- \leqslant \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+$ and $Vi- \geqslant V_{EE} + 3.2V$

For applications using symmetrical supplies, the peak input voltage should be below ground by 0.9V. If this is not acceptable then pin 12 of the device can be redefined externally. See Fig.2 and Biasing Condition D.

Rx is used to balance the offset voltage between the two inputs (see Fig.3).

Bias voltage values at several nodes are indicated on Fig.2.

R_{ext} is connected from pin 12 to pin 11 (V_{EE}) to increase output bias current I_{out}. This current should not exceed 30mA. The value of R_{ext} is calculated as follows:

$$R_{ext} = \left[\frac{500}{I_{out} - 10}\right]\Omega$$

where I_{out} is in mA.

Buffer

The on-chip buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. A ground plane should be used to minimise any earth induced currents between the input and output circuits. The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be located close to the device supply pins. Signal source and load should be located close to the circuit with good termination. For 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition type.

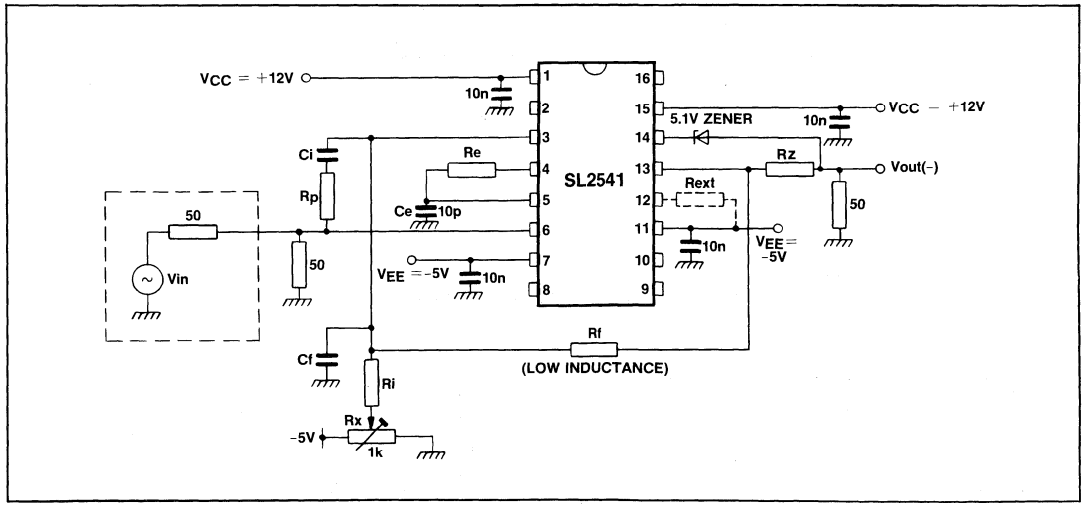


Fig.3 Test/applications circuit for SL2541 in non-inverting mode of operation

Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor (R_e) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain is decreased the value of R_e should be increased. A graph of recommended value of R_e with gain is given in Fig 8.

Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and provide DC offset at the output. Although some power is dissipated in the external Zener, a heatsink on the SL2541 will be necessary if the power exceeds 800mW dissipation.

Bandwidth Compensation

When operated at inverting mode any peaking due to board and component strays can be compensated by the following methods.

A. A capacitor of small value between the two inputs will roll off high frequency pass band region e.g. 1.8pF is used for x1 and x10 gain settings with PCB layout shown in Fig.18.

B. A capacitor of suitable value across the input resistor to compensate for any strays from the other input to ground. e.g. 10pF used for x10 gain frequency response.

C. A resistor of suitable value (R_Z) in series with the Zener diode does reduce the high frequency peak and also adjusts the output voltage swing. (See Fig.3) e.g. a 56Ω resistor used for x20 gain frequency response.

In non-inverting mode of operation when using method **A** a resistor of suitable value in series with a small capacitor used is to compensate the bandwidth. e.g. a 680Ω resistor with 1.8pF capacitor in series is used to increase the passband region to 800MHz at x2 gain settings.

Generally, a combination of these three methods will keep the response stable and eliminate the peaking at other operating conditions.

Also in inverting mode a decoupling capacitor from pin 5 will increase the first pole roll off and hence reduce the noise bandwidth. For example a 10pF capacitor will increase the roll off from 38dB/dec to 63dB/dec.

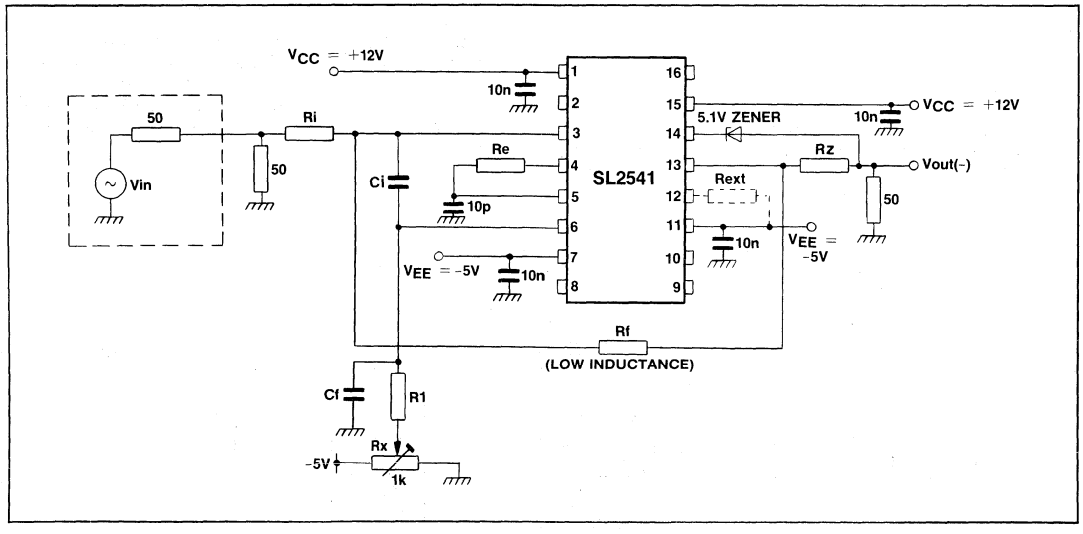


Fig.4 Test/applications circuit for SL2541 in inverting mode of operation

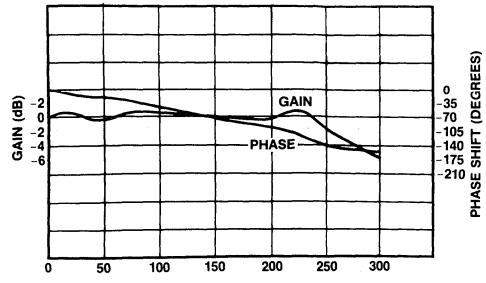


Fig.5 Typical frequency/phase performance graphs for circuit of Fig.4. Inverting, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

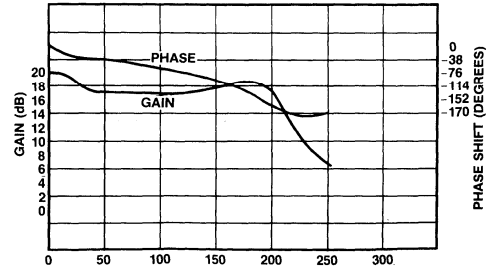


Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.4. Inverting, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

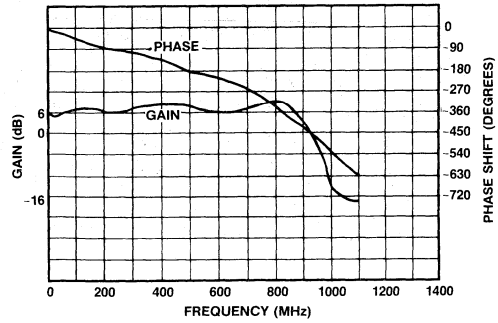


Fig.7 Typical frequency/phase performance graphs for the circuit of Fig.3, non-inverting, x2 gain, 50Ω load, V_{CC} = +12V, V_{EE} = -5V

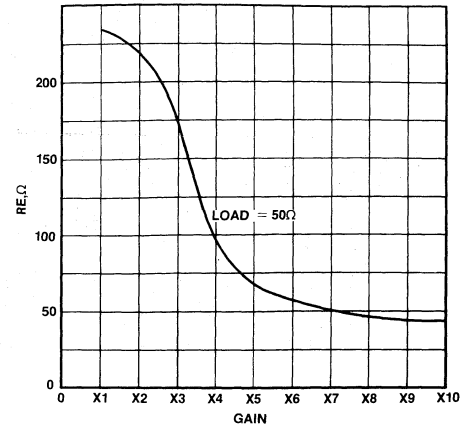


Fig.8 Typical closed loop gain v. typical values of the degeneration resistor R_e

Response	Gain	R_f(Ω)	R_i(Ω)	R_1(Ω)	Zener	R_Z	R_e(Ω)	C_f(pF)	R_p(Ω)	C_f(pF) load	V_{out} (p-p) into 1.2kΩ
Fig.5	x1	470	470	470	5.1V	56	220	1.8	-	10	8V
Fig.6	x10	4.7k	470	470	5.1V	56	39	-	-	3.3	7V
Fig.7	x2	560	560	-	5.1V	100	220	1.8	680	-	5V

Table 1 Recommended component values for the applications circuits of Figs. 3 and 4

NOTE
C_i, C_f, R_p, R_z are compensation network components and are partly dependent on layout and board strays.

TIME DOMAIN RESPONSE GRAPHS FOR THE TEST CIRCUIT OF FIG.3. NON-INVERTING, x2, LOAD 1.2kΩ

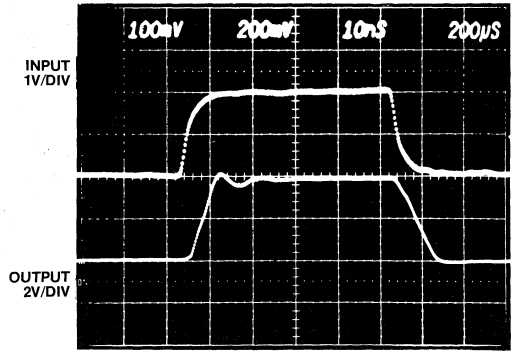


Fig.9 Large signal pulse response

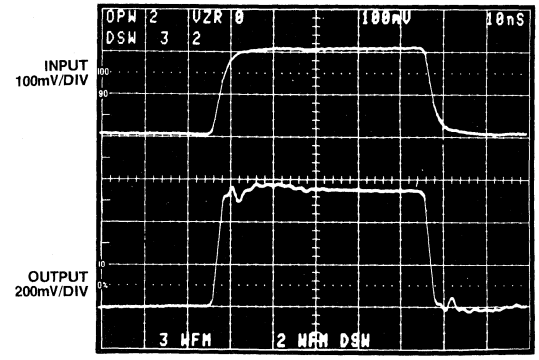


Fig.10 Small signal pulse response

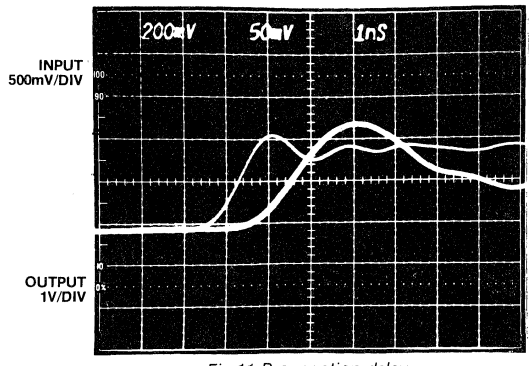


Fig.11 Propagation delay

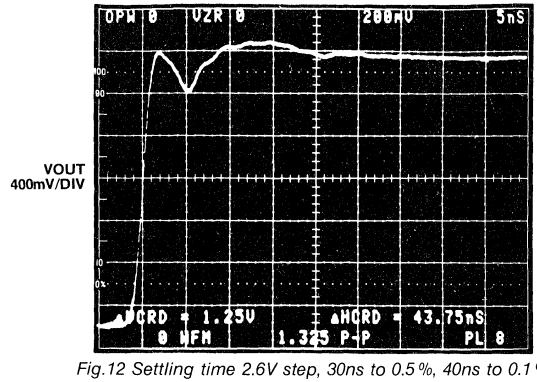


Fig.12 Settling time 2.6V step, 30ns to 0.5%, 40ns to 0.1%

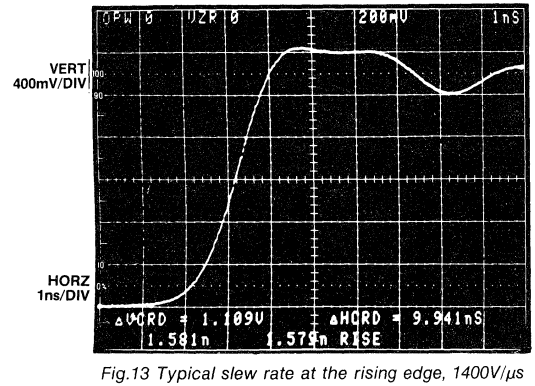


Fig.13 Typical slew rate at the rising edge, 1400V/μs

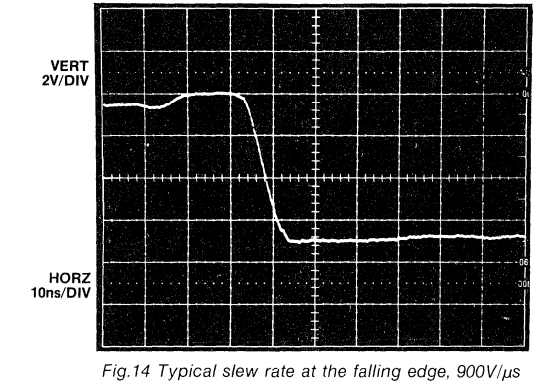


Fig.14 Typical slew rate at the falling edge, 900V/μs

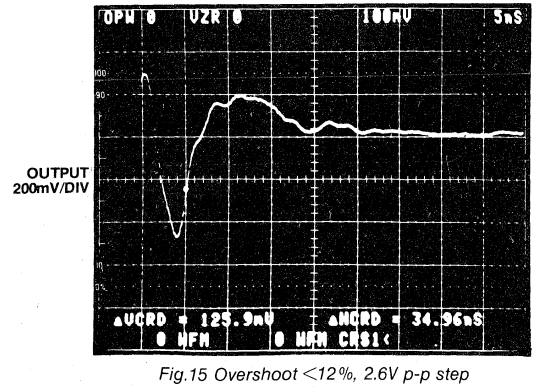


Fig.15 Overshoot <12%, 2.6V p-p step

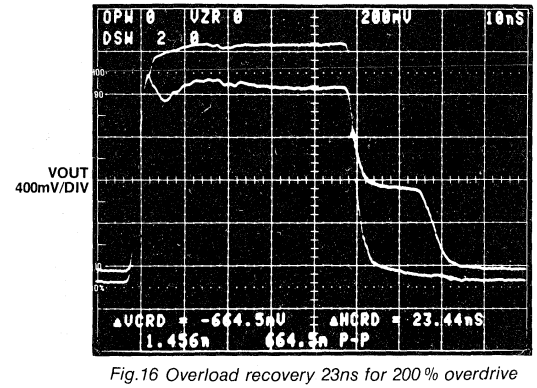


Fig.16 Overload recovery 23ns for 200% overdrive

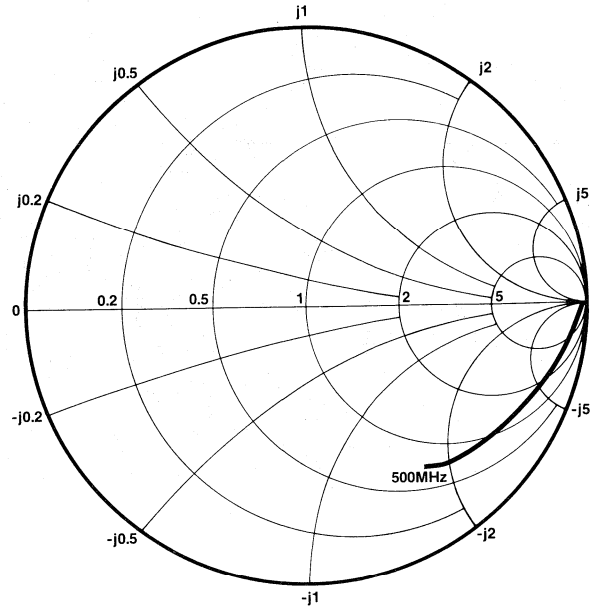


Fig.17 SL2541 open circuit dynamic input impedance normalised to 50Ω. 100MHz frequency markers (see Electrical Characteristics table).

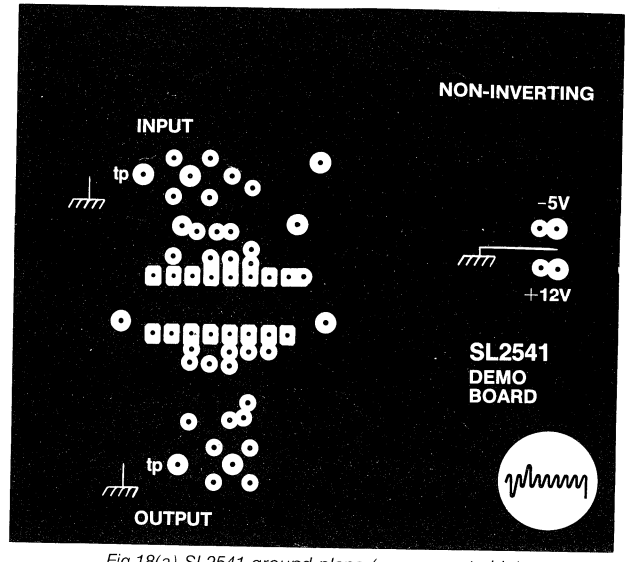


Fig.18(a) SL2541 ground plane (component side)

NOTE: Input and output are sub-vis type 50-ohm connectors. RF is on the track side. Gold socket pins are used to mount the SL2541 for test circuit.

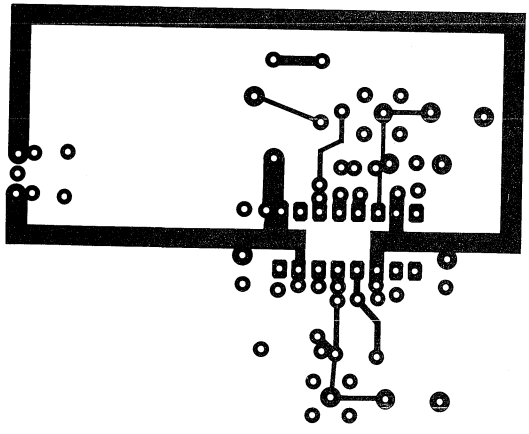


Fig.18(b) SL2541 PCB, track side

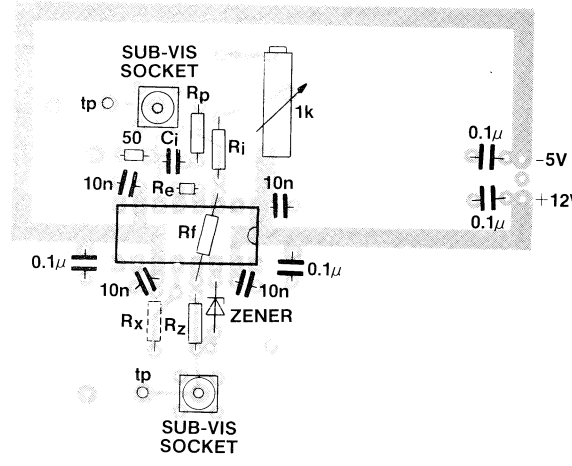


Fig 18(c) SL2541 PCB, component location

Fig.18 PCB layout of SL2541 demonstration board for the circuit of Fig.3 (scale 1:1)

PLESSEY
Semiconductors

SL3127C

HIGH FREQUENCY NPN TRANSISTOR ARRAY

The SL3127C is a monolithic array of five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.6dB. The SL3127C is pin compatible with the CA3127.

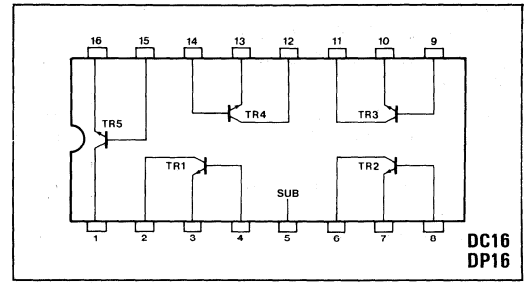


Fig.1 Pin connections SL3127

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.6dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

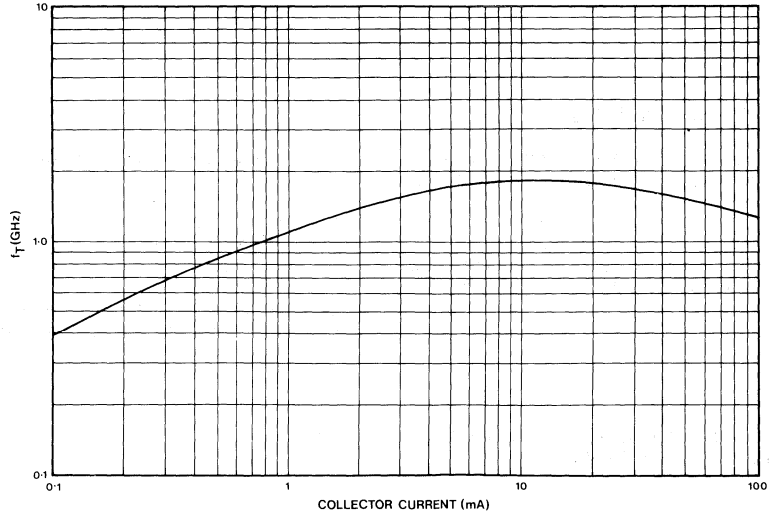


Fig.2 Transition frequency (f_T) v. collector current (V_{CB}=2V, f=200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	I_C = 10μA, I_E = 0
Collector emitter breakdown	LV_{CEO}	15	18		V	I_C = 1mA, I_B = 0
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	I_C = 10μA, I_R = I_C = 0
Base to isolation breakdown	BV_{BIO}	10	20		V	I_B = 10μA, I_C = I_E = 0
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	V_{CE} = 6V, I_C = 1mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	I_C = 10mA, I_B = 1mA
Emitter base leakage current	I_{EBO}		0.1	1	μA	V_{EB} = 4V
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	I_C = 10mA, I_B = 1mA
Base emitter voltage difference, all transistors	ΔV_{BE}		0.45	5	mV	V_{CE} = 6V, I_C = 1mA
Input offset current	ΔI_B		0.2	3	μA	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		μV/°C	V_{CE} = 6V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	V_{CE} = 6V, I_C = 1mA
Static forward current ratio	H_{FE}	35	95			V_{CE} = 6V, I_C = 5mA
		35	100			V_{CE} = 6V, I_C = 0.1mA
		40	100			V_{CE} = 6V, I_C = 1mA
Collector base leakage	I_{CBO}		0.3		nA	V_{CB} = 16V
Collector isolation leakage	I_{CIO}		0.6		nA	V_{CI} = 20V
Base isolation leakage	I_{BIO}		100		nA	V_{BI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CB} = 0V
Collector isolation capacitance	C_{CI}		0.8		pF	V_{CI} = 0V
Dynamic characteristics						
Transition frequency	f_T		1.6		GHz	V_{CE} = 6V, I_C = 5mA
Wideband noise figure	NF		3.6		dB	f = 60MHz, V_{CC} = 6V, I_C = 2mA, R_S = 200Ω
Knee of 1/f noise curve			1		kHz	f = 60MHz, V_{CC} = 6V, I_C = 2mA, R_S = 200Ω

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 20 volt
V_{EB} = 4.0 volt
V_{CE} = 15 volt
V_{CI} = 20 volt
I_C = 20 mA
Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DC16	DP16
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100°C/watt.

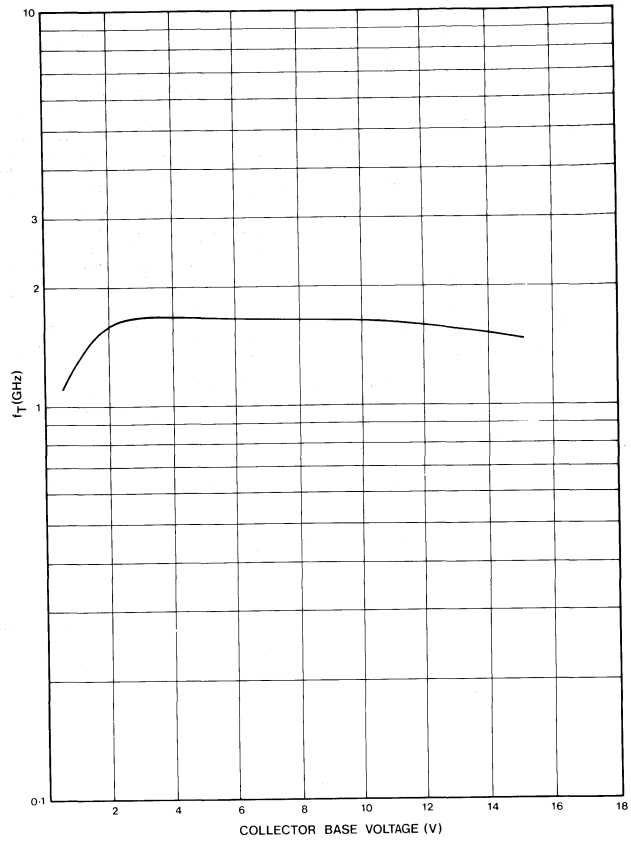


Fig.3 Transition frequency (f_T) v. collector base voltage
(I_C = 5mA, Frequency = 200MHz)

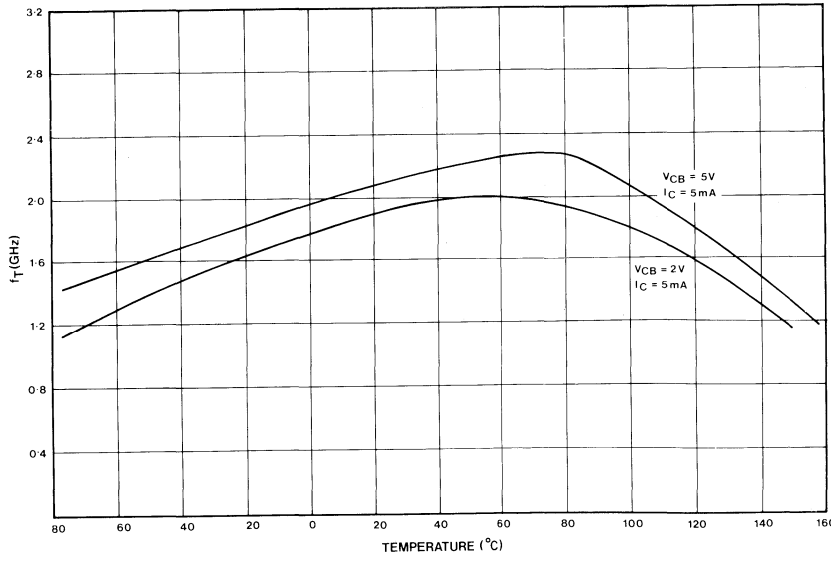


Fig.4 Variation of transition frequency (f_T) with temperature

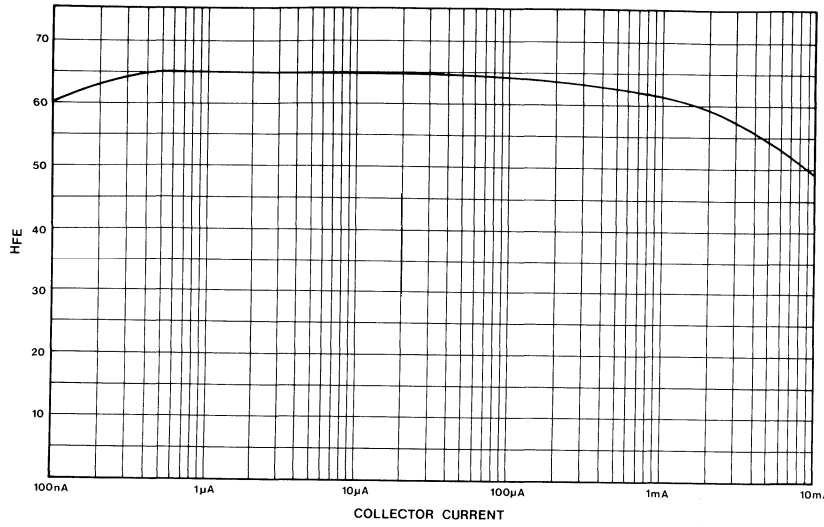


Fig.5 DC current gain v. collector current

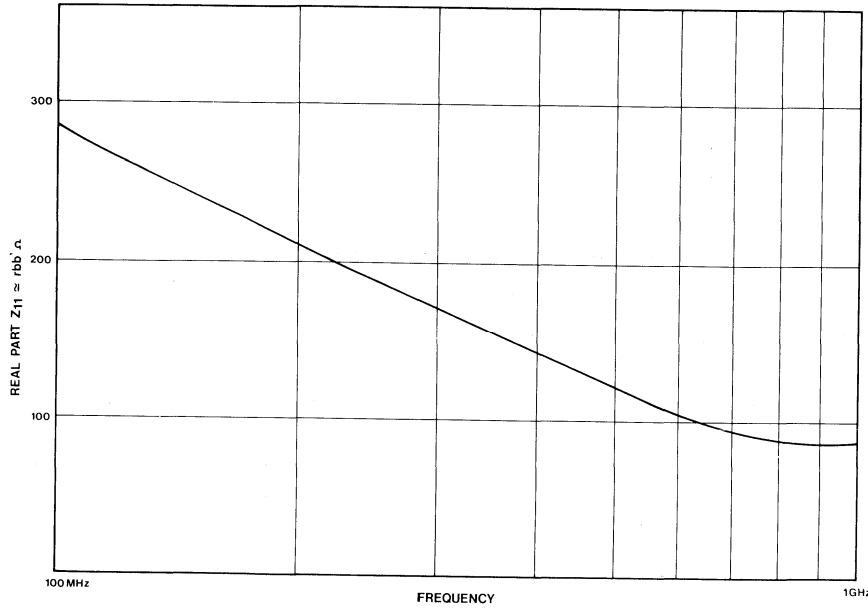


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r_{bb'}$)

SL3145C,E

1.6GHz NPN TRANSISTOR ARRAYS

The SL3145C is a monolithic array of five high frequency low current NPN transistors. The SL3145C consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_{TS} of 1.6GHz and wideband noise figures of 3.0dB. The device is pin compatible with the CA3046. The SL3145E has guaranteed C_{CB} and f_T figures.

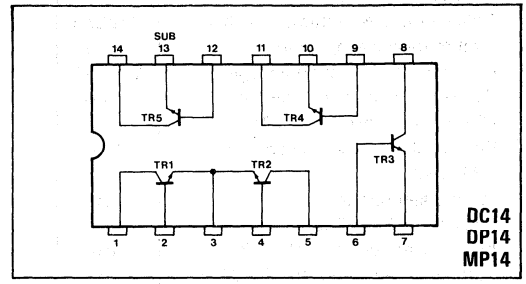


Fig.1 Pin connections SL3145

FEATURES

- f_T Typically 1.6 GHz
- Wideband Noise Figure 3.0dB
- V_{BE} Matching Better Than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

Ordering information	
SL3145C-DC	Ceramic/Metal
SL3145C-DP	Plastic
SL3145E-DP	Plastic

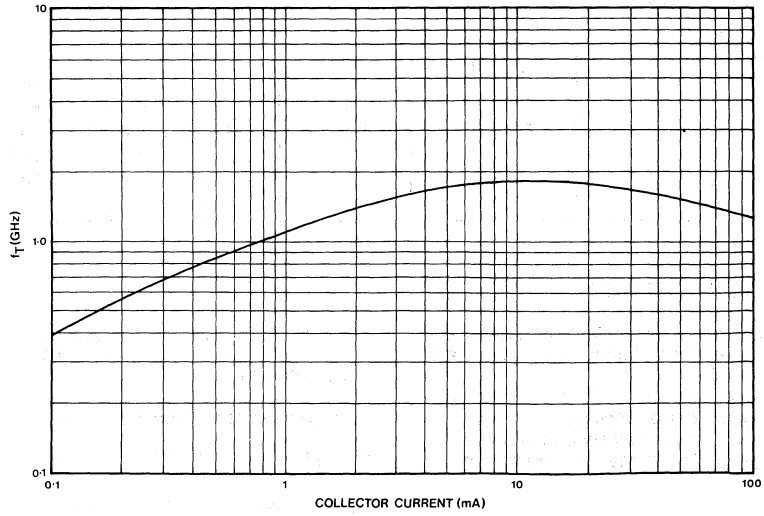


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Static characteristics						
Collector base breakdown	BV_{CBO}	20	30		V	$I_C = 10\mu A, I_E = 0$
Collector emitter breakdown	LV_{CEO}	15	18		V	$I_C = 1mA, I_B = 0$
Collector substrate breakdown (isolation)	BV_{CIO}	20	55		V	$I_C = 10\mu A, I_R = I_E = 0$
Base to isolation breakdown	BV_{BIO}	10	20		V	$I_B = 10\mu A, I_C = I_E = 0$
Base emitter voltage	V_{BE}	0.64	0.74	0.84	V	$V_{CE} = 6V, I_C = 1mA$
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.26	0.5	V	$I_C = 10mA, I_B = 1mA$
Emitter base leakage current	I_{EBO}		0.1	1	μA	$V_{EB} = 4V$
Base emitter saturation voltage	$V_{BE(SAT)}$		0.95		V	$I_C = 10mA, I_B = 1mA$
Base emitter voltage difference, all transistors except TR1,TR2	ΔV_{BE}		0.45	5	mV	$V_{CE} = 6V, I_C = 1mA$
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.35	5	mV	$V_{CE} = 6V, I_C = 1mA$
Input offset current (except for TR1, TR2)	ΔI_B		0.2	3	μA	$V_{CE} = 6V, I_C = 1mA$
Input offset current TR1, TR2	ΔI_B		0.2	2	μA	$V_{CE} = 6V, I_C = 1mA$
Temperature coefficient of ΔV_{BE}	$\frac{\partial \Delta V_{BE}}{\partial T}$		2.0		$\mu V/°C$	
Temperature coefficient of V_{BE}	$\frac{\partial V_{BE}}{\partial T}$		-1.6		mV/°C	$V_{CE} = 6V, I_C = 1mA$
Static forward current ratio	H_{FE}	40	100			$V_{CE} = 6V, I_C = 1mA$
Collector base leakage	I_{CBO}		0.3		nA	$V_{CB} = 16V$
Collector isolation leakage	I_{CIO}		0.6		nA	$V_{CI} = 20V$
Base isolation leakage	I_{BIO}		100		nA	$V_{BI} = 5V$
Emitter base capacitance	C_{EB}		0.4		pF	$V_{EB} = 0V$
Collector base capacitance						
SL3145C	C_{CB}		0.4		pF	$V_{CB} = 0V$
SL3145E			0.4	1.1	pF	$V_{CB} = 0V$
Collector isolation capacitance	C_{CI}		0.8		pF	$V_{CI} = 0V$
Dynamic characteristics						
Transition frequency						
SL3145C	f_T		1.6		GHz	$V_{CE} = 6V, I_C = 5mA$
SL3145E		1.2			GHz	$V_{CE} = 6V, I_C = 10mA$
Wideband noise frequency	NF		3.0		dB	$V_{CE} = 2V, R_S = 1k\Omega$ $I_C = 100\mu A, f = 60MHz$
Knee of 1/f noise curve			1		kHz	$V_{CE} = 6V, R_S = 200\Omega$ $I_C = 2mA$

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life maybe shortened or specified parameters may be degraded.

All electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

$V_{CB} = 20$ volt
$V_{EB} = 4.0$ volt
$V_{CE} = 15$ volt
$V_{CI} = 20$ volt
$I_C = 20$ mA

Maximum individual transistor dissipation 200 mWatt
Storage temperature −55°C to 150°C
Max junction temperature 150°C

Package thermal resistance (°C/watt):−

Package Type	DC14	DP14
Chip to case	40	
Chip to ambient	120	180

NOTE:
If all the power is being dissipated in one transistor, these thermal resistance figures should be increased by 100° C/watt.

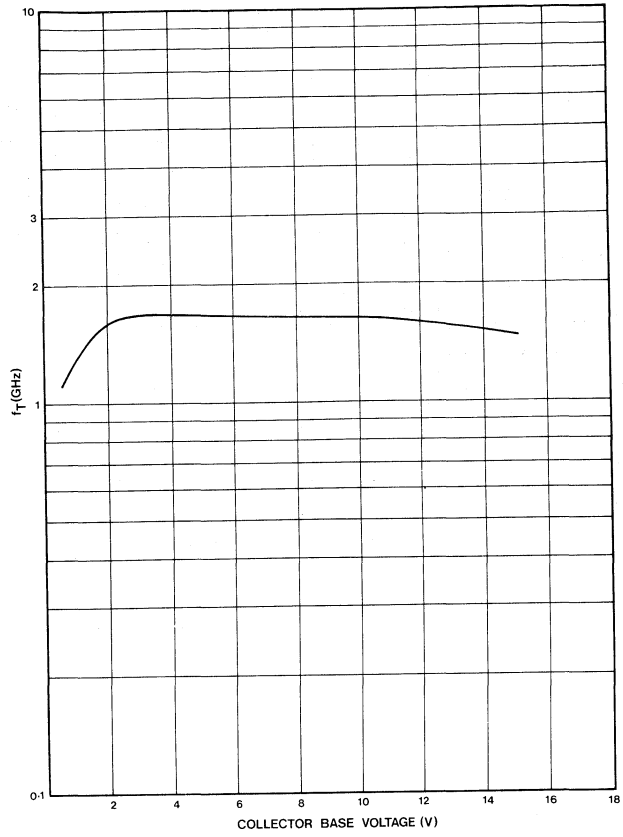


Fig.3 Transition frequency (f_T) v. collector base voltage (I_C = 5mA, frequency = 200MHz)

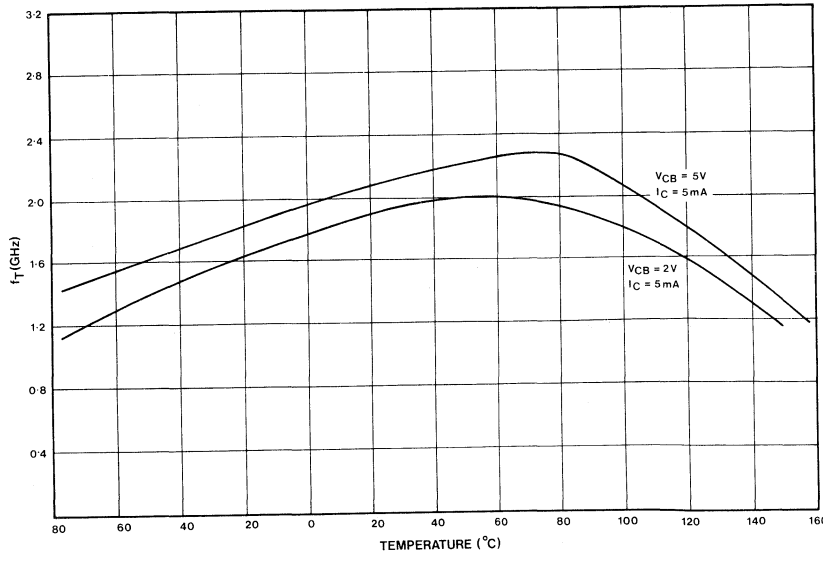


Fig.4 Variation of transition frequency (f_T) with temperature

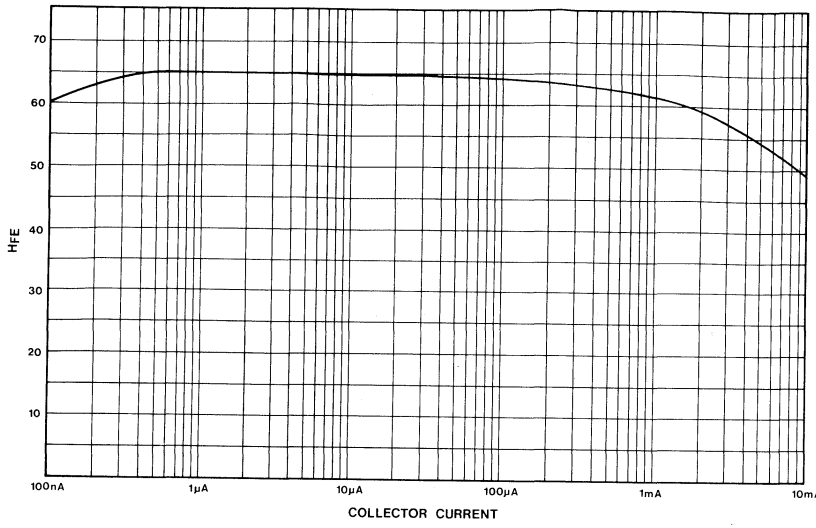


Fig.5 DC current gain v. collector curent

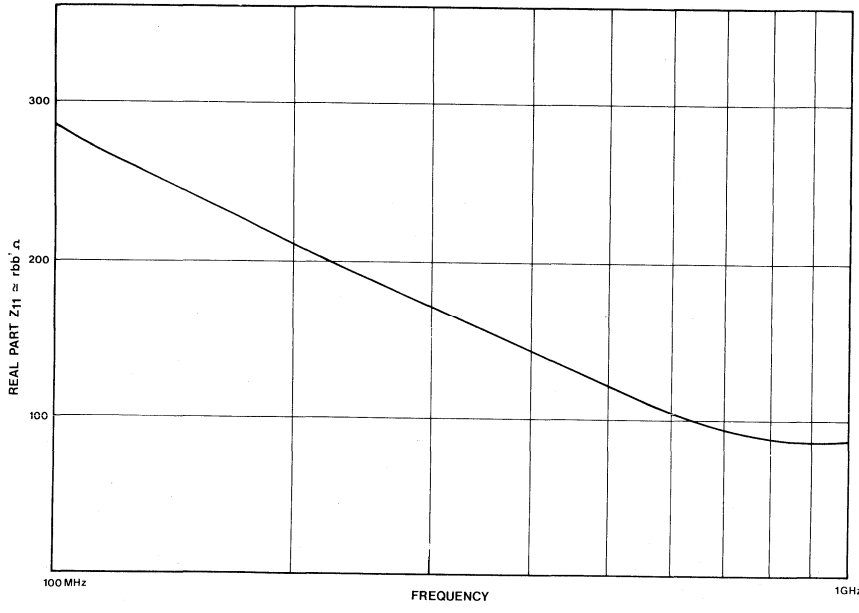


Fig.6 Z_{11} (derived from scattering parameters) v. frequency ($Z_{11} \simeq r66'$)

PLESSEY
Semiconductors

SL3227

3GHz NPN TRANSISTOR ARRAYS

The SL3227 is a monolithic array of the five high frequency low current NPN transistors in a 16 lead DIL package. The transistors exhibit typical f_T of 3GHz and wideband noise figures of 2dB. The SL3227 is pin compatible with the CA3127 and SL3127.

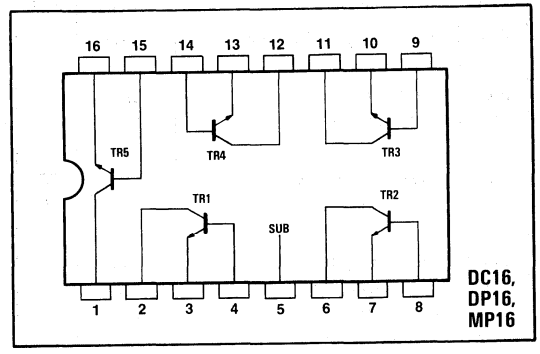


Fig.1 Pin connections - SL3227

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching better than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All Electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10V
V_{EB} = 2.5V
V_{CE} = 6V
V_{CI} = 15V
I_C = 20mA
Maximum individual transistor dissipation 200mW
Storage temperature -55° C to +150° C
Max. junction temperature +150° C

Package thermal resistance (° C/watt)

Package Type	DC16	DP16	MP16
Chip to Case	40		
Chip to Ambient	120	180	200

NOTE: If all the power is being dissipated in one transistor these thermal resistance figures should be increased by 100° C/watt.

ORDERING INFORMATION

SL3227 DC Ceramic/Metal
SL3227 DP Plastic
SL3227 MP Miniature Plastic

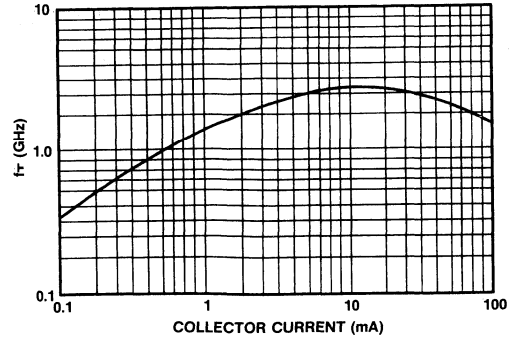


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = 22°C \pm 2°C$

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	$I_C = 10\mu A$
Collector isolation breakdown	BV_{CIO}	16	40		V	$I_C = 10\mu A$
Base emitter breakdown	BV_{EBO}	2.5	5.0		V	$I_E = 10\mu A$
Collector emitter breakdown	LV_{CEO}	6	9		V	$I_C = 5mA$
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	$I_C = 10mA$, $I_B = 1mA$
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	$V_{CE} = 2V$, $I_C = 1mA$
Base emitter voltage difference all transistors	ΔV_{BE}		0.45	5.0	mV	$V_{CE} = 2V$, $I_C = 1mA$
Input offset current	ΔI_B		0.2	3	μA	$V_{CE} = 2V$, $I_C = 1mA$
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		mV/°C	$V_{CE} = 2V$, $I_C = 1mA$
Static forward current ratio	H_{fe}	35	80			$V_{CE} = 2V$, $I_C = 5mA$
		35	95			$V_{CE} = 2V$, $I_C = 0.1mA$
		40	85			$V_{CE} = 2V$, $I_C = 1mA$
Emitter base leakage	I_{EBO}		15		nA	$V_{EB} = 2V$
Collector base leakage	I_{CBO}		5		pA	$V_{CB} = 10V$
Collector isolation leakage	I_{CIO}		5		pA	$V_{CI} = 16V$
Emitter base capacitance	C_{EB}		0.7		pF	$V_{EB} = 0V$
Collector base capacitance	C_{CB}		0.4		pF	$V_{CI} = 0V$
Collector isolation capacitance	C_{CI}		1.5	2.0	pF	$V_{CI} = 0V$

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	$V_{CE} = 2V$, $I_C = 5mA$
Wideband noise figure	NF		2.0		dB	$f = 60MHz$ $V_{CC} = 6V$
Knee of NF noise curve			1		kHz	$I_C = 1mA$
						$R_S = 1k\Omega$

PLESSEY
Semiconductors

SL3245

3GHz NPN TRANSISTOR ARRAY

The SL3245 is a monolithic array of five high frequency low current NPN transistors. The SL3245 consists of 3 isolated transistors and a differential pair in a 14 lead DIL package. The transistors exhibit typical f_T of 3GHz and wideband noise figures of 2dB. The device is pin compatible with the SL3045C and SL3145.

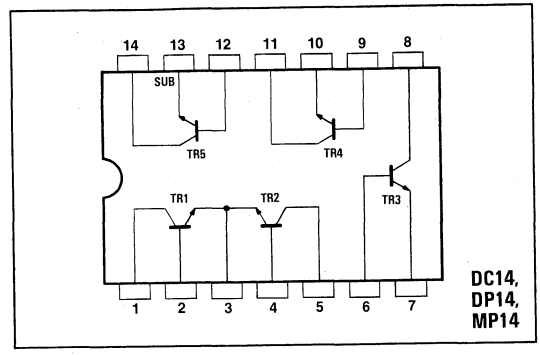


Fig.1 Pin connections - SL3245

FEATURES

- f_T Typically 3GHz
- Wideband Noise Figure 2.0dB
- V_{BE} Matching better than 5mV

APPLICATIONS

- Wide Band Amplifiers
- PCM Regenerators
- High Speed Interface Circuits
- High Performance Instrumentation Amplifiers
- High Speed Modems

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

All Electrical ratings apply to individual transistors. Thermal ratings apply to the total package.

The isolation pin (substrate) must be connected to the most negative voltage applied to the package to maintain electrical isolation.

V_{CB} = 10V
V_{EB} = 2.5V
V_{CE} = 6V
V_{CI} = 15V
I_C = 20mA
Maximum individual transistor dissipation 200mW
Storage temperature -55° C to +150° C
Max. junction temperature +150° C

Package thermal resistance (° C/watt)

Package Type	DC14	DP14	MP14
Chip to Case	40		
Chip to Ambient	120	180	200

NOTE: If all the power is being dissipated in one transistor these thermal resistance figures should be increased by 100° C/watt.

ORDERING INFORMATION

SL3245 DC Ceramic/Metal
SL3245 DP Plastic
SL3245 MP Miniature Plastic

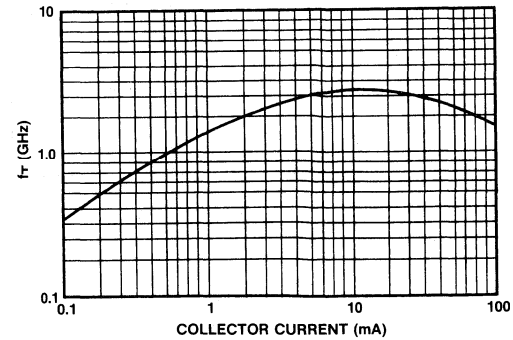


Fig.2 Transition frequency (f_T) v. collector current (V_{CB} = 2V, f = 200MHz)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 22°C ± 2°C

Static Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Collector base breakdown	BV_{CBO}	10	20		V	I_C = 10μA
Collector isolation breakdown	BV_{CIO}	16	40		V	I_C = 10μA
Base emitter breakdown	BV_{EBO}	2.5	5.0		V	I_E = 10μA
Collector emitter breakdown	LV_{CEO}	6	9		V	I_C = 5mA
Collector emitter saturation voltage	$V_{CE(SAT)}$		0.22	0.5	V	I_C = 10mA, I_B = 1mA
Base emitter voltage	V_{BE}	0.73	0.78	0.81	V	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference (except TR1, TR2)	ΔV_{BE}		0.45	5.0	mV	V_{CE} = 2V, I_C = 1mA
Base emitter voltage difference TR1, TR2	ΔV_{BE}		0.33	5.0	mV	V_{CE} = 2V, I_C = 1mA
Input offset current (except TR1,TR2)	ΔI_B		0.2	3	μA	V_{CE} = 2V, I_C = 1mA
Input offset current TR1,TR2	ΔI_B		0.2	2	μA	V_{CE} = 2V, I_C = 1mA
Temperature coefficient of V_{BE}	$\frac{\Delta V_{BE}}{T}$		-1.69		mV/°C	V_{CE} = 2V, I_C = 1mA
Static forward current ratio	H_{fe}	35	80			V_{CE} = 2V, I_C = 5mA
		35	90			V_{CE} = 2V, I_C = 0.1mA
		40	85			V_{CE} = 2V, I_C = 1mA
Emitter base leakage	I_{EBO}		10		nA	V_{EB} = 2V
Collector base leakage	I_{CBO}		5		pA	V_{CB} = 10V
Collector isolation leakage (TR1-TR4)	I_{CIO}		10		pA	V_{CI} = 16V
Collector isolation leakage (TR5)	I_{CIO}		10		pA	V_{CI} = 5V
Emitter base capacitance	C_{EB}		0.4		pF	V_{EB} = 0V
Collector base capacitance	C_{CB}		0.4		pF	V_{CI} = 0V
Collector isolation capacitance	C_{CI}		1.4	2.0	pF	V_{CI} = 0V

Dynamic Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Transition frequency	f_T		3		GHz	V_{CE} = 2V, I_C = 5mA
Wideband noise figure	NF		2.0		dB	f = 60MHz V_{CC} = 6V I_C = 1mA
Knee of NF noise curve			1		kHz	R_S = 1kΩ

PLESSEY
Semiconductors

SL6140

400MHz WIDEBAND AGC AMPLIFIER

The SL6140 is an integrated broadband AGC amplifier, designed on an advanced 3-micron all implanted bipolar process. The amplifier provides over 15dB of linear gain into 50Ω at 400MHz.

Accurate gain control is also provided with over 70dB of dynamic range.

The SL6140 provides over 45dB of voltage gain with an R_L of 1kΩ.

FEATURES

- 400MHz Bandwidth (R_L = 50 Ohms)
- High Voltage Gain 45dB (R_L = 1kOhm)
- 70dB Gain Control Range
- High Output Level at Low Gain
- Accurate Gain Control
- Full Military Temperature Range (LC Only)
- MC1590 Replacement with Improved Performance

APPLICATIONS

- RF/IF Amplifier
- High Gain Mixers
- Video Amplifiers

ORDERING INFORMATION

SL6140 MP (Industrial - Miniature Plastic DIL package)
SL6140 B LC (Military - LCC package)
SL6140 CM (Military - Metal Can package)

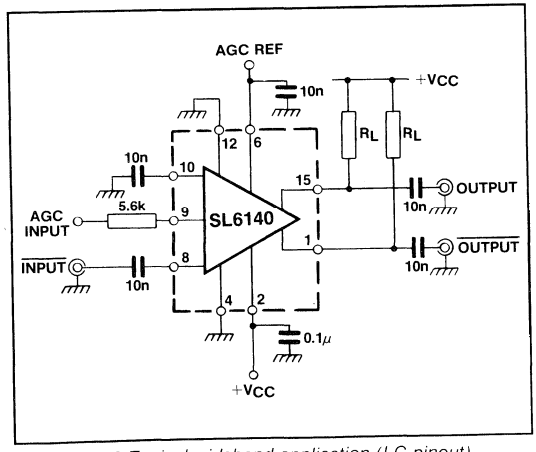
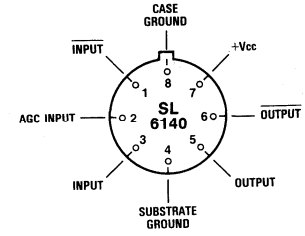
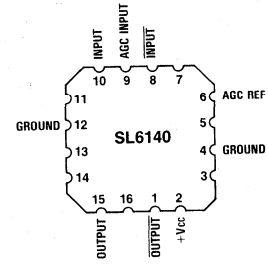


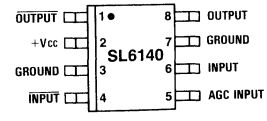
Fig.2 Typical wideband application (LC pinout)



CM8



LC16



MP8

Fig.1 Pin connections - top view

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = 25 °C, V_{CC} = +12V

Characteristic	Pin (LC)	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	2,15,1	-	19	23	mA	V_{CC} +12V
Output stage current	15,1 (sum)	5	7	9	mA	V_{CC} = +12V
Output current matching (magnitude of difference of output currents)	15,1	-	0.5	-	mA	
AGC range	9	60	75	-	dB	See Fig.4
Voltage gain (single ended)	15,1	40	45	-	dB	R_L = 1kΩ See Fig.5
			55		dB	Tuned input and output
	15,1	-	15	-	dB	R_L = 50Ω
Bandwidth (-3dB)	15,1	-	25	-	MHz	R_L = 1kΩ See Fig.5
	15,1	-	400	-	MHz	R_L = 50Ω
Maximum output level (single ended)						
0dB AGC	15,1	2.5	3.5	-	V	
-30dB AGC	15,1	2.5	3.5		p-p	R_L = 1kΩ

DESCRIPTION

The SL6140 (Fig.3) is a high gain amplifier with an AGC control capable of reducing the gain of the amplifier by over 70dB. The gain is adjusted by applying a voltage to the AGC input via an external resistor, the value of which adjusts the curve of gain reduction versus control voltage (see Fig.4). As the output stage of the amplifier is an open collector the voltage gain is determined by R_L. With a load resistance of 1kΩ the single ended voltage gain is 45dB and with a load resistance of 50Ω the voltage gain is 15dB (20 log V_{OUT}/V_{IN}). Another parameter that depends on the load resistance is the bandwidth: 25MHz for R_l = 1kΩ, as compared with 400MHz for R_L = 50Ω. So R_L is chosen to give either the required bandwidth or voltage gain for the circuit.

Fig.7 shows the input impedance of the device. Accurate impedance matching to both inputs and outputs of this device (by resonant circuit or other means) can raise the gain to 55dB but for most circumstances a 50Ω source impedance is adequate.

The AGC reference output (on pin 6 of LC version only) can be used to monitor the gain of the amplifier accurately over the full temperature range.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	+15V
Input voltage (differential)	+5V
AGC supply	V_{CC}
Storage temperature	-55 °C to +125 °C
Operating temperature	
SL6140 MP	0 °C to 70 °C
SL6140 B LC/CM	-30 °C to +125 °C

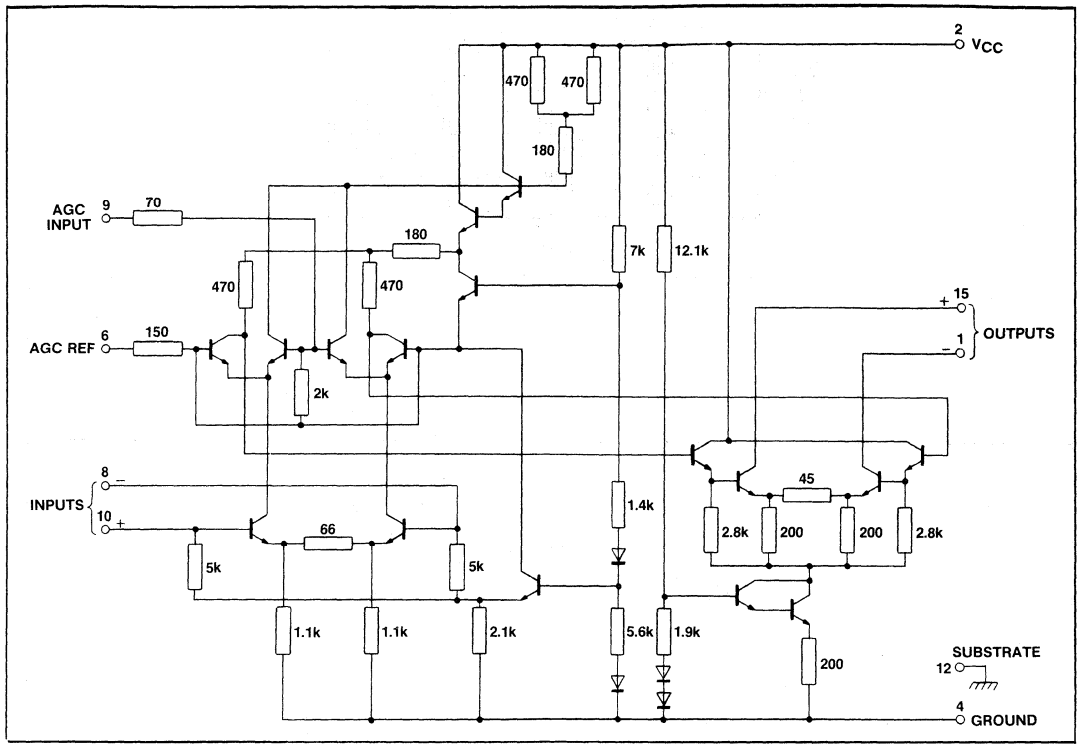


Fig.3 Full circuit diagram of SL6140 (LC pinout)

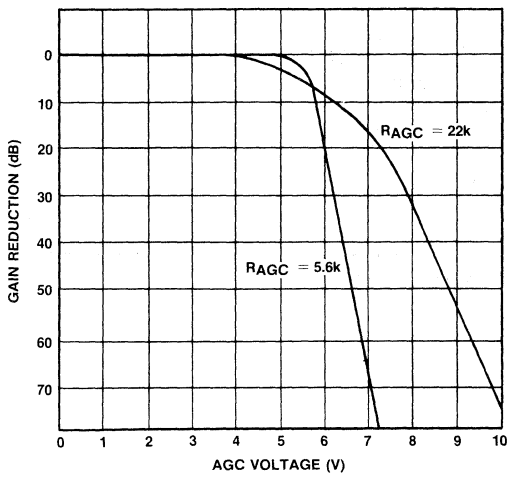


Fig.4 Gain reduction v. AGC voltage

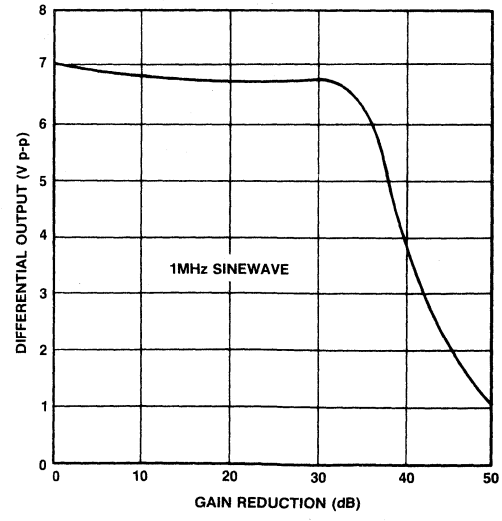


Fig.5 Voltage gain v. frequency

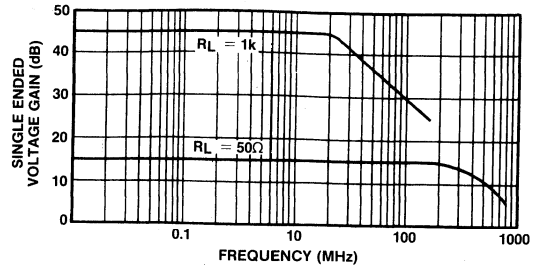


Fig.6 Maximum differential output v. gain reduction

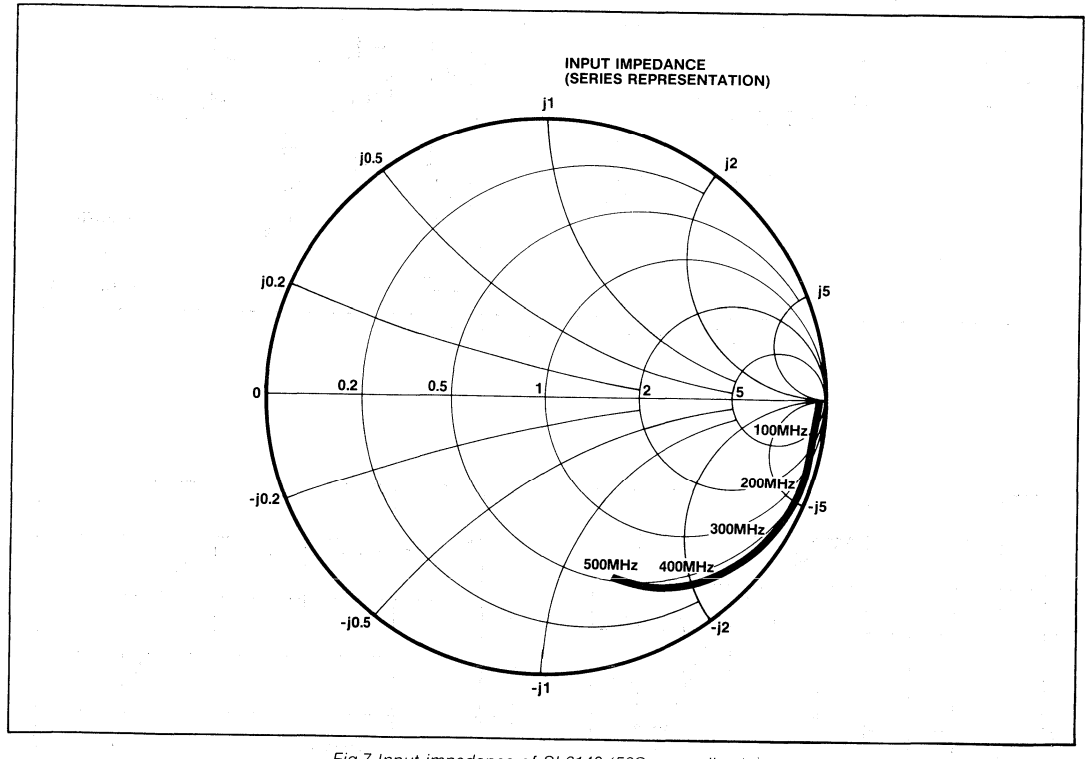


Fig.7 Input impedance of SL6140 (50Ω normalised)

PLESSEY
Semiconductors

SL6270C

GAIN CONTROLLED MICROPHONE PREAMPLIFIER/VOGAD

The SL6270 is a silicon integrated circuit combining the functions of audio amplifier and voice operated gain adjusting device (VOGAD).

It is designed to accept signals from a low sensitivity microphone and to provide an essentially constant output signal for a 50dB range of input. The dynamic range, attack and decay times are controlled by external components.

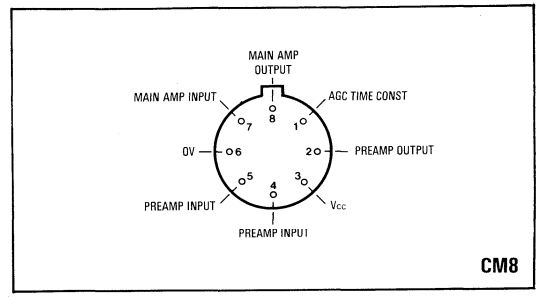


Fig.1 Pin connections, SL6270 - CM (bottom view)

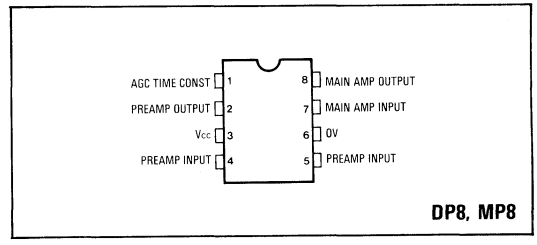


Fig.2 Pin connectons, SL6270 - DP (top view)

FEATURES

- Constant Output Signal
- Fast Attack
- Low Power Consumption
- Simple Circuitry

APPLICATIONS

- Audio AGC Systems
- Transmitter Overmodulation Protection
- Tape Recorders

QUICK REFERENCE DATA

- Supply Voltage: 4.5V to 10V
- Voltage Gain: 52dB

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 12V
Storage temperature: −55°C to +125°C

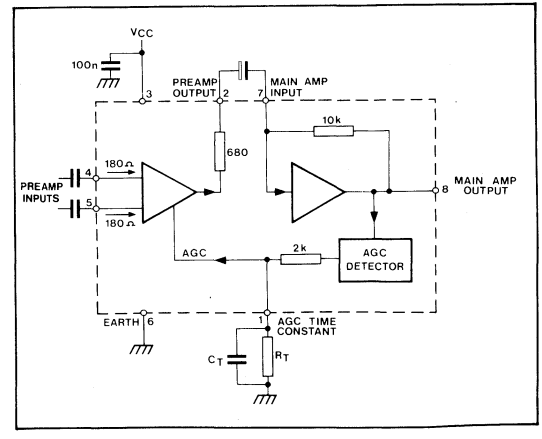
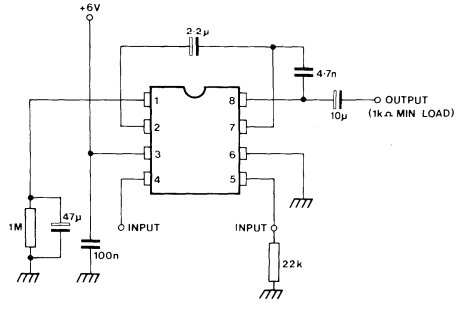


Fig.3 SL6270 block diagram

ELECTRICAL CHARACTERISTICS

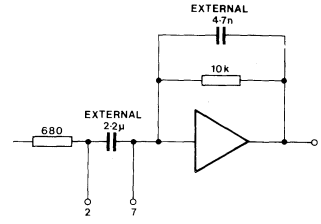
Test conditions (unless otherwise stated):
Supply voltage Vcc: 6V
Input signal frequency: 1kHz
Ambient temperature: −30°C to +85°C
Test circuit shown in Fig. 4

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5	10	mA	
Input impedance		150		Ω	Pin 4 or 5
Differential input impedance		300		Ω	
Voltage gain	40	52		dB	72μV rms input pin 4
Output level	55	90	140	mV rms	4mV rms input pin 4
THD		2	5	%	90mV rms input pin 4
Equivalent noise input voltage		1		μV	300Ω source, 400Hz to 25kHz bandwidth



N.B. If input not AC coupled the resistance between pins 4 and 5 must be less than 10 ohms.

Fig.4 SL6270 test and application circuit



Voltage gain = $\frac{10k\Omega}{680\Omega}$

Upper frequency response 10kΩ/4.7nF = 3kHz
Lower frequency response 680Ω/2.2μF = 300Hz

Fig.5 SL6270 frequency response

APPLICATION NOTES

Voltage gain

The input to the SL6270 may be single ended or differential but must be capacitor coupled. In the single-ended mode the signal can be applied to either input, the remaining input being decoupled to ground. Input signals of less than a few hundred microvolts rms are amplified normally but as the input level is increased the AGC begins to take effect and the output is held almost constant at 90mV rms over an input range of 50dB.

The dynamic range and sensitivity can be reduced by reducing the main amplifier voltage gain. The connection of a 1k resistor between pins 7 and 8 will reduce both by approximately 20dB. Values less than 680Ω are not advised.

Frequency response

The low frequency response of the SL6270 is determined by the input, output and coupling capacitors. Normally the coupling capacitor between pins 2 and 7 is chosen to give a -3dB point at 300Hz, corresponding to 2.2μF, and the other capacitors are chosen to give a response to 100Hz or less.

The SL6270 has an open loop upper frequency response of a few MHz and a capacitor should be connected between pins 7 and 8 to give the required bandwidth.

Attack and delay times

Normally the SL6270 is required to respond quickly by holding the output level almost constant as the input is increased. This 'attack time', the time taken for the output to return to within 10% of the original level following a 20dB increase in input level, will be approximately 20ms with the circuit of Fig.4. It is determined by the value of the capacitor connected between pin 1 and ground and can be calculated approximately from the formula:

$$\text{Attack time} = 0.4\text{ms}/\mu\text{F}$$

The decay time is determined by the discharge rate of the capacitor and the recommended circuit gives a decay rate of 20dB/second. Other values of resistance between pin 1 and ground can be used to obtain different results.

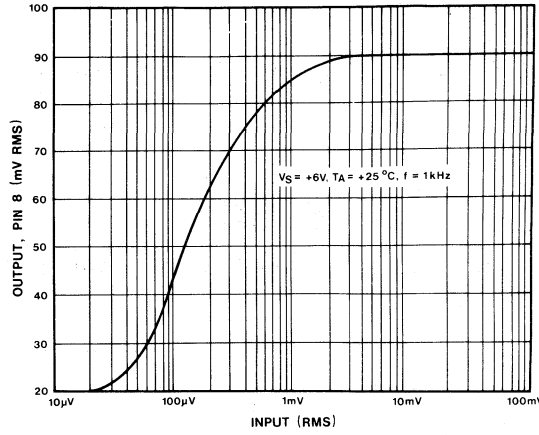


Fig. 6 Voltage gain (single ended input) (typical)

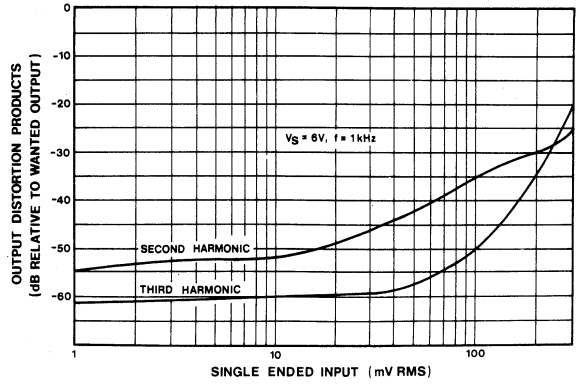


Fig. 7 Overload characteristics (typical)

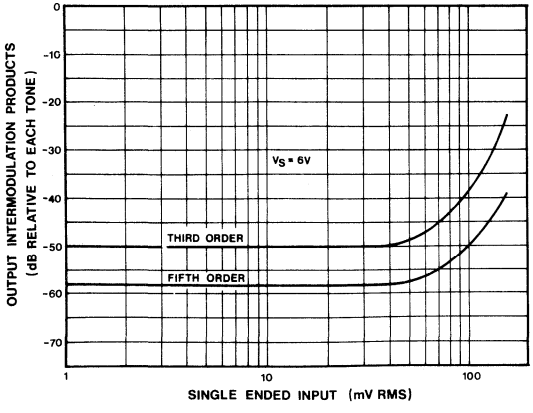


Fig. 8 Typical Intermodulation distortion (1.55 and 1.85kHz tones)

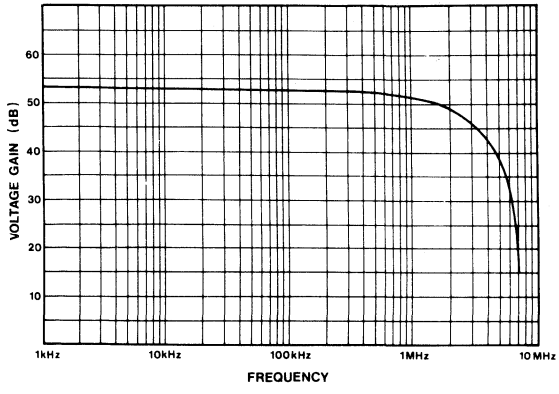


Fig. 9 Open loop frequency response (typical)

SL6310C

500mW SWITCHABLE AUDIO AMPLIFIER/OP AMP

The SL6310C is a low power audio amplifier which can be switched off by applying a mute signal to the appropriate pin. Despite the low quiescent current consumption of 5mA (only 0.6mA when muted) a minimum output power of 400mW is available into an 8Ω load from a 9V supply.

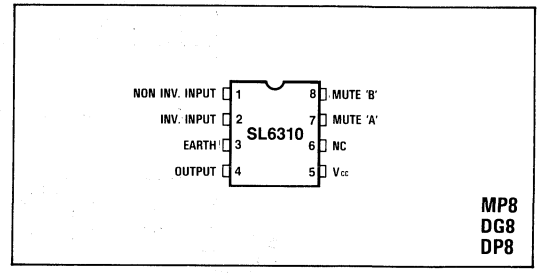


Fig.1 Pin connections SL6310 - (top view)

FEATURES

- Can be Muted with High or Low State Inputs
- Operational Amplifier Configuration
- Works Over Wide Voltage Range

APPLICATIONS

- Audio Amplifier for Portable Receivers
- Power Op. Amp
- High Level Active Filter

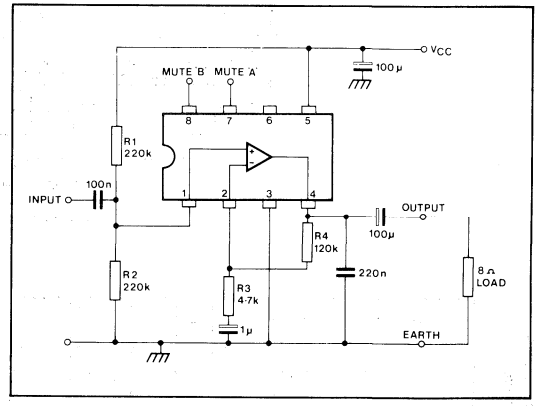


Fig.2 SL6310 test circuit

QUICK REFERENCE DATA

- Supply Voltage : 4.5V to 13.6V
- Voltage Gain : 70dB
- Output into 8Ω on 9V Supply : 400mW (min.)

ABSOLUTE MAXIMUM RATINGS

Supply voltage : 15V
Storage temperature : −55°C to +125°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage Vcc: 9V
Ambient temperature: −30°C to +85°C
Mute facility: Pins 7 and 8 open circuit frequency = 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		5.0	7.5	mA	
Supply current muted (A)		0.55	1	mA	Pin 7 via 470k to earth
Supply current muted (B)		0.6	0.9	mA	Pin 8 = Vcc
Input offset voltage		2	20	mV	Rs ⩽ 10k
Input offset current		50	500	nA	
Input bias current (Note 1)		0.2	1	μA	
Voltage gain	40	70		dB	
Input voltage range		2.1		V	Vcc = 4.5V
		10.6		V	Vcc = 13V
CMRR	40	60		dB	Rs⩽10k
Output power	400	500		mW	RL = 8Ω
THD		0.4	3	%	POUT = 400mW, Gain = 28dB

NOTE
1. The input bias current flows **out** of pins 1 and 2 due to PNP input stage

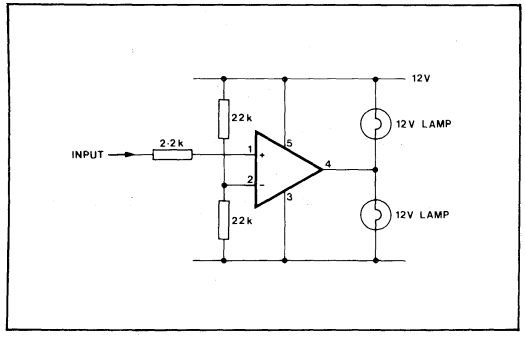


Fig.3 SL6310 lamp driver

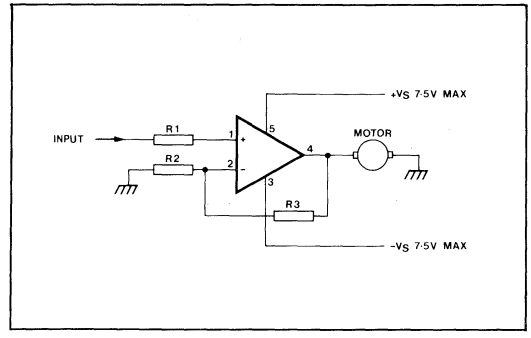


Fig.4 SL6310 servo amplifier

OPERATING NOTES

Mute facility

The SL6310 has twomute control pins to allow easy interfacing to inputs of high or low levels. Mute control 'A', pin 7, is left open circuit or connected to a voltage within 0.65 volt of Vcc (via a 100kΩ resistor) for normal operation. When the voltage on pin 7 is reduced to within 1 volt of earth (via a 100kΩ resistor) the SL6310 is muted.

Audio amplifier

As the SL6310 is an operational amplifier it is easy to obtain the voltage gain and frequency response required. To keep the input impedance high it is wise to feed the signal to the non-inverting input as shown in Fig.2. In this example the input impedance is approximately 100kΩ. The voltage gain is determined by the ratio (R3 + R4)/R3 and should be between 3 and 30 for best results. The capacitor in series with R3, together with the input and output coupling capacitors, determines the low frequency rolloff point. The upper frequency limit is set by the device but can be restricted by connecting a capacitor across R4.

Operational amplifier

It is impossible to list all the application possibilities in a single data sheet but the SL6310 offers considerable advantages over conventional devices in high output current applications such as lamp drivers (Fig.3) and servo amplifiers (Fig.4).

Buffer and output stages for signal generators are another possibility together with active filter sections requiring high output current.

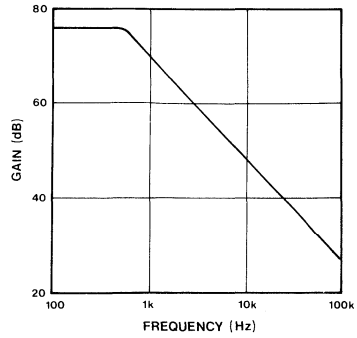


Fig.5 Gain v. frequency

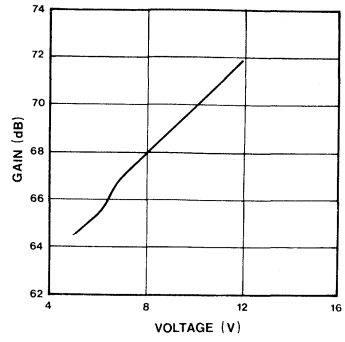


Fig.6 Gain v. supply voltage

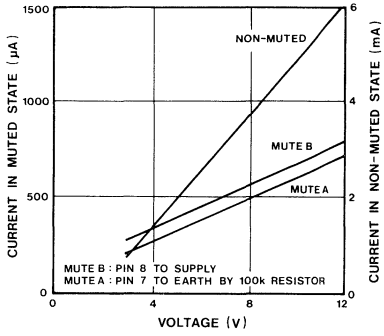


Fig.7 Supply current v. supply voltage

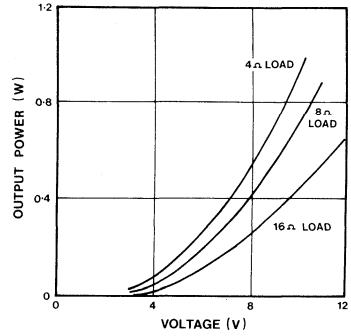


Fig.8 Output power v. supply voltage at 5% (max) distortion

PLESSEY
Semiconductors

SL6440A & C

HIGH LEVEL MIXER

The SL6440 is a double balanced mixer intended for use in radio systems up to 150MHz. A special feature of the circuit allows external selection of the DC operating conditions by means of a resistor connected between pin 11 (bias) and V_{CC}. When biased for a supply current of 50mA the SL6440 offers a 3rd order intermodulation intercept point of typically +30dBm, a value previously unobtainable with integrated circuits. This makes the device suitable for many applications where diode ring mixers had previously been used and offers the advantages of a voltage gain, low local oscillator drive requirement and superior isolation.

The SL6440C is in a 16-lead DIL plastic package (DP), and is specified for operation from -30°C to +85°C; the SL6440A is in a ceramic DIL package (DG) and has military temperature range specification of -55°C to +125°C.

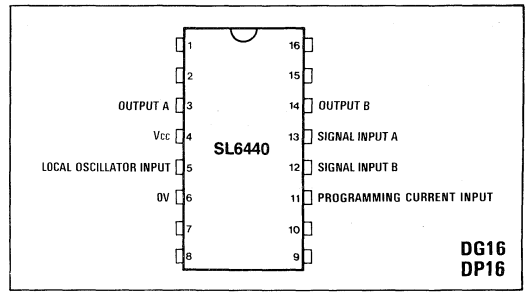


Fig.1 Pin connections - top view

FEATURES

- +30dBm Input Intercept Point
- +15dBm Compression Point (1dB)
- Programmable Performance
- Full Military Temperature Range (SL6440A)

APPLICATIONS

- Mixers in Radio Transceivers
- Phase Comparators
- Modulators

ABSOLUTE MAXIMUM RATINGS

Supply voltage and output pins	15V
Maximum power dissipation	1200mW
(Derate above 25°C: 8mW/°C)	
Storage temperature range	-65°C to +150°C
Programming current into pin 11	50mA

THERMAL CHARACTERISTICS

Thermal resistance: θ_{JA}	125°C/W
θ_{JC}	40°C/W
Time constant: Junction-Ambient	1.9 mins
Maximum chip temperature	150°C

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC1} = 12V; V_{CC2} = 10V; I_P = 25mA; T_{amb} = -55°C to +125°C (SL6440A), -30°C to +85°C (SL6440C)
Local oscillator input level = 0dBm; Test circuit Fig.2.

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Signal frequency 3dB point	100	150		MHz	
Oscillator frequency 3dB point	100	150		MHz	
3rd order input intercept point		+30		dBm	
Third order intermodulation distortion		-60		dB	} Two 0dBm input
Second order intermodulation distortion		-75		dB	} Signals
1dB compression point		15		dBm	V_{CC1} = 15V V_{CC2} = 12V
					V_{CC1} = 12V V_{CC2} = 10V
Noise figure		11		dB	Fig.8 test circuit
Conversion gain		-1		dB	50Ω load Fig.2
Carrier leak to signal input	-40			dB	Test circuit Fig.8
Level of carrier at IF output		-25		dBm	See applications information
Supply current		7		mA	I_P = 0
Supply current (total from V_{CC1} & V_{CC2})		60		mA	
Local oscillator input	100	250	500	mV rms	I_P = 35mA
Local oscillator input impedance		1.5		kΩ	
Signal input impedance		500		Ω	Single ended
		1000		Ω	Differential

NOTE Supply current in Pin 3 is equal to that in Pin 14 and is equal to I_p. See over. V_{pin11} 3 V_{be} 2.1V.

CIRCUIT DESCRIPTION

The SL6440 is a high level mixer designed to have a linear RF performance. The linearity can be programmed using the I_P pin (11).

The output pins are open collector outputs so that the conversion gain and output loads can be chosen for the specific application.

Since the outputs are open collectors they should be returned to a supply $V_{CC}1$ through a load.

The choice of $V_{CC}1$ is important since it must be ensured that the voltage on pins 3 and 14 is not low enough to saturate the output transistors and so limit the signal swing unnecessarily. If the voltage on pins 3 and 14 is always greater than $V_{CC}2$ the outputs will not saturate. The output frequency response will reduce as the output transistors near saturation.

Minimum $V_{CC}1$ = $(I_P \times RL) + V_S + V_{CC}2$
where I_P = programmed current
RL = DC load resistance
V_S = max signal swing at output
if the signal swing is not known:
minimum $V_{CC}1$ = $2\,(I_P \times RL) + V_{CC}2$

In this case the signal will be limiting at the input before the output saturates.

The device has a separate supply ($V_{CC}2$) for the oscillator buffer (pin 4).

The current (I_P) programmed into pin 11 can be supplied via a resistor from $V_{CC}1$ or from a current source.

The conversion gain is equal to

$$GdB = 20 \text{ Log } \frac{RL\ I_P}{56.61\ I_P + 0.0785} \text{ for single-ended output}$$

$$GdB = 20 \text{ Log } \frac{2\ RL\ I_P}{56.61\ I_P + 0.0785} \text{ for differential output}$$

Device dissipation is calculated using the formula

mW diss = $2\ I_P\ V_O + V_P\ I_P + V_{CC}2$ Diss
where V_O = voltage on pin 3 or pin 14
V_P = voltage on pin 11
I_P = programming current (mA)
$V_{CC}2$ Diss = dissipation obtained from graph (Fig.6)

As an example Fig. 7 shows typical dissipations assuming $V_{CC}1$ and V_O are equal. This may not be the case in practice and the device dissipation will have to be calculated for any particular application.

Fig.5 shows the intermodulation performance against I_P. The curves are independent of $V_{CC}1$ and $V_{CC}2$ but if $V_{CC}1$ becomes too low the output signal swing cannot be accommodated, and if $V_{CC}2$ becomes too low the circuit will not provide enough drive to sink the programmed current. Examples are shown of performance at various supply voltages.

The current in pin 14 is equal to the current in pin 3 which is equal to the current in pin 11.

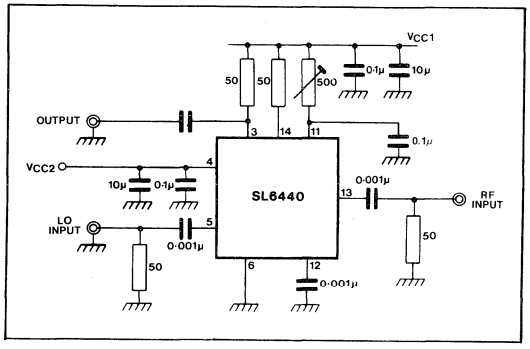


Fig.2 Typical application and test circuit

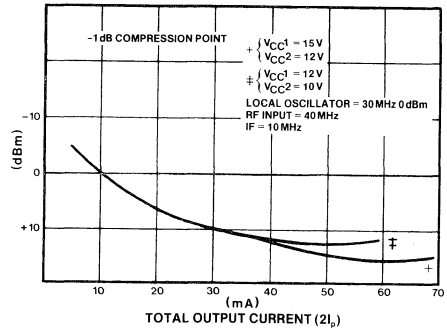


Fig.3 Compression point v. total output current

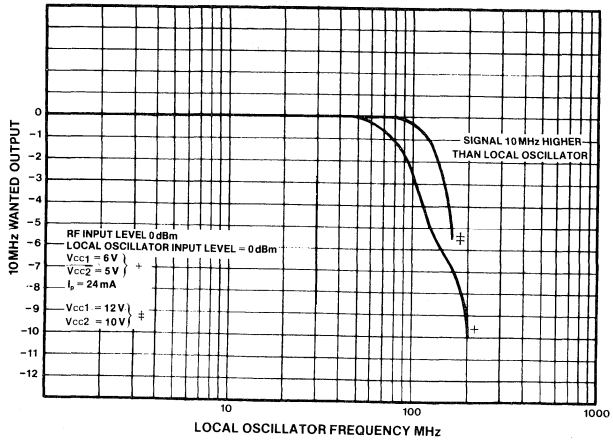


Fig.4 Frequency response at constant output IF

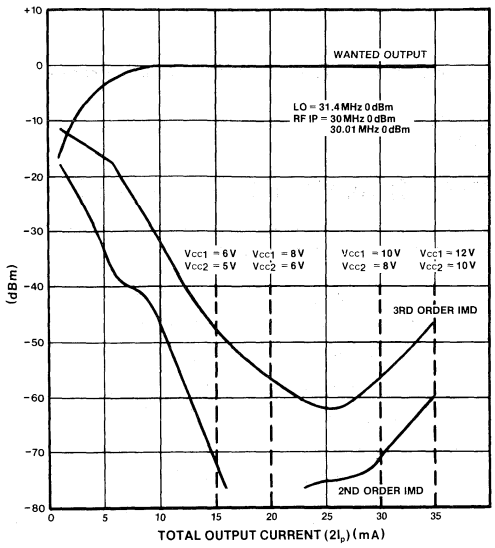


Fig.5 Intermodulation v. programming current

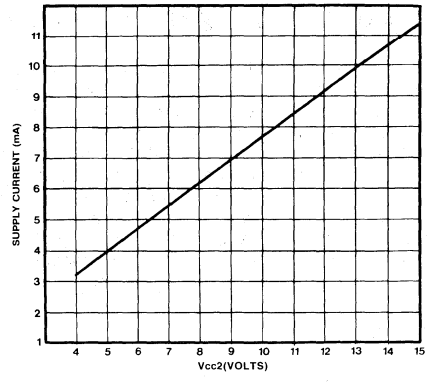


Fig.6 Supply current v. Vcc2 (I_P = 0)

APPLICATIONS

The SL6440 can be used with differential or single-ended inputs and outputs. A balanced input will give better carrier leak. The high input impedance allows step-up transformers to be used if desired, whilst high output impedance allows a choice of output impedance and conversion gain.

Fig. 2 shows the simplest application circuit. The input and output are single-ended and I_P is supplied from Vcc1 via a resistor. Increasing RL will increase the conversion gain, care being taken to choose a suitable value for Vcc1.

Fig. 8 shows an application with balanced input, for improved carrier leak, and balanced output for increased conversion gain. A lower Vcc1 giving lower device dissipation can be used with this arrangement.

DESIGN PROCEDURE

1. Decide on input configuration using local oscillator data. If using transformer on input, decide on ratio from noise considerations.
2. Decide on output configuration and value of conversion gain required.
3. Decide on value of I_P and Vcc2 using intermodulation and compression point graphs.
4. Using values of conversion gain, Vcc2, load and I_P already chosen, decide on value of Vcc1.
5. Calculate device dissipation and decide whether heatsink is required from maximum operating temperature considerations.

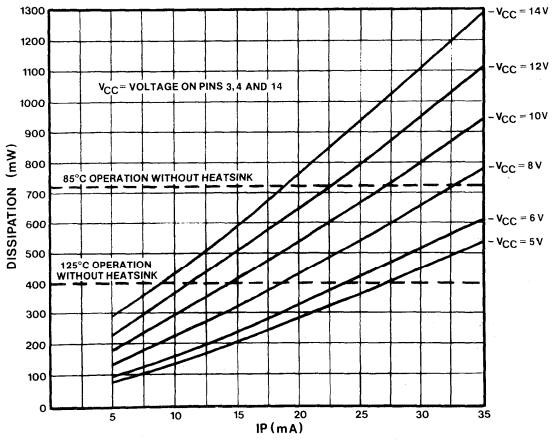


Fig.7 Device dissipation v. I_P

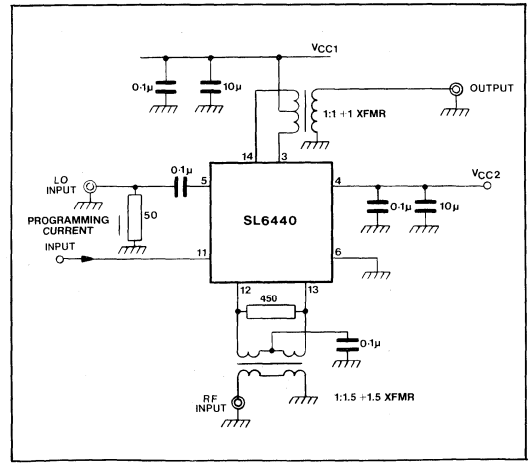


Fig.8 Typical application circuit for highest performance

PLESSEY
Semiconductors

SL6601C

FM IF, PLL DETECTOR (DOUBLE CONVERSION) AND RF MIXER

The SL6601 is a straight through or single conversion IF amplifier and detector for FM radio applications. Its minimal power consumption makes it ideal for hand held and remote applications where battery conservation is important. Unlike many FM integrated circuits, the SL6601 uses an advanced phase locked loop detector capable of giving superior signal-to-noise ratio with excellent co-channel interference rejection, and operates with an IF of less than 1MHz. Normally the SL6601 will be fed with an input signal of up to 17MHz: there is a crystal oscillator and mixer for conversion to the IF amplifier, a PLL detector and squelch system.

FEATURES

- High Sensitivity: 2μV Typical
- Low Power: 2·3mA Typical at 7V
- Advanced PLL Detector
- Available in Miniature 'Chip Carrier' Package
- 100% Tested for SINAD

APPLICATIONS

- Low Power NBFM Receivers
- FSK Data Equipment
- Cellular Radio Telephones

QUICK REFERENCE DATA

- Supply Voltage 7V
- 50dB S/N Ratio

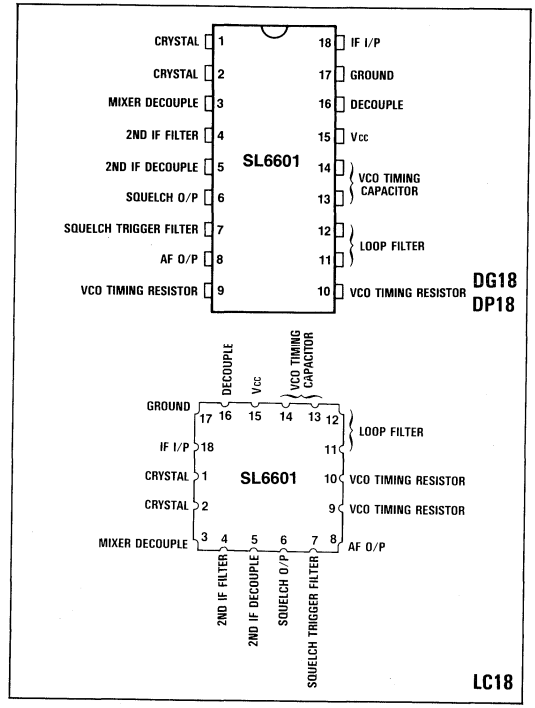


Fig.1 Pin connections - top view

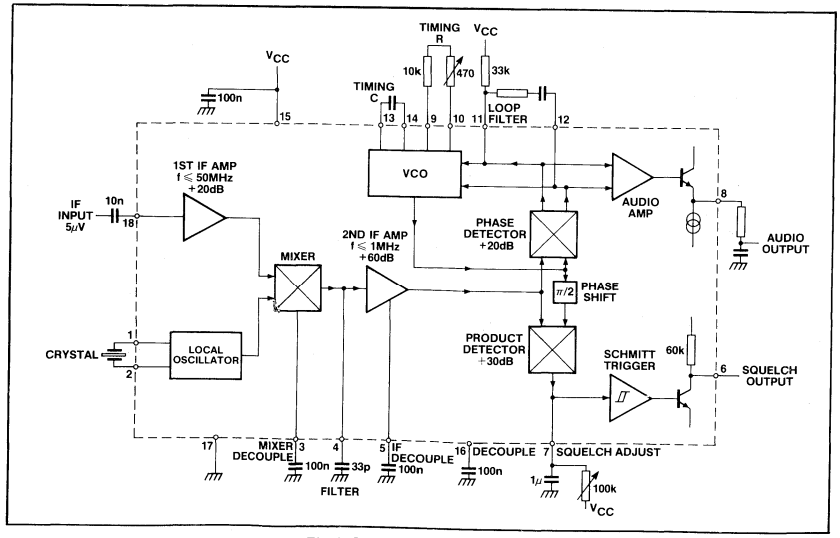


Fig.2 SL6601 block diagram

Example

A frequency modulated signal has a deviation of 10kHz and a maximum modulating frequency of 5kHz. The VCO frequency is 200kHz.

Let f_n = 6kHz and D = 0.5

Then from the graph

$$\frac{\Phi_{efn}}{\Delta f} = 0.85$$

$$\Phi_e = \frac{0.85\Delta f}{f_n} = \frac{0.85 \times 10}{6} = 1.4 \text{ rads.}$$

This is too large, so increase f_n e.g. to 10kHz.

$$\frac{f_m}{f_n} = 0.5 \frac{\Phi_{efn}}{\Delta f} = 0.45$$

$$\Phi_e = \frac{0.45 \times 10}{10} = 0.45$$

- which is somewhat low

Therefore set f_n = 7.5kHz

$$\frac{f_m}{f_n} = 0.666$$

$$\frac{\Phi_{efn}}{\Delta f} = 0.66$$

$$\Phi_e = \frac{0.66 \times 10}{7.5} = 0.88 \text{ rads.}$$

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$K_o K_D = 0.3 f_o$ where f_o is the VCO frequency

$$t_1 + t_2 = \frac{0.3 \times 200 \times 10^3}{(2\pi \times 7.5 \times 10^3)^2} = 27\mu s$$

$$t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

$$= \frac{0.5}{\pi \times 7.5 \times 10^3} - \frac{1}{0.3 \times 200 \times 10^3}$$

$$= 4.5\mu s$$

$$t_1 = 22.5\mu s$$

$$C = \frac{t_1}{20 \times 10^3} = \frac{22.5 \times 10^{-6}}{20 \times 10^3} = 1.125\text{nF (use 1nF)}$$

$$R = \frac{t_2}{t_1} \times 20 \times 10^3$$

$$= \frac{4.5}{22.5} \times 20 \times 10^3$$

$$= 4k\Omega \text{ (use 3.9k)}$$

Actual loop parameters can now be recalculated

$t_1 = 20\mu s$ $t_2 = 3.9\mu s$

$$2\pi f_n = \frac{(K_o K_D)}{(t_1 \times t_2} = \frac{(2 \times 10^5 \times 0.3)}{(23.9 \times 10^{-6})} = 50.1\text{k rad/sec} = 7.97\text{kHz}$$

$$D = f_n(t_2 + \frac{1}{K_o K_D}) = \underline{0.515}$$

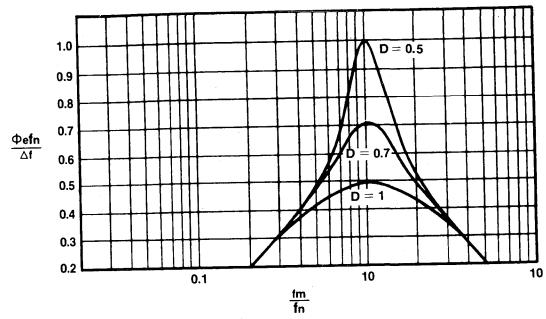


Fig.3 Damping factor

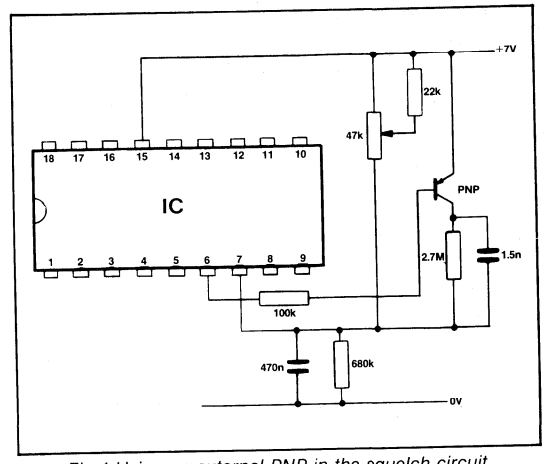


Fig.4 Using an external PNP in the squelch circuit

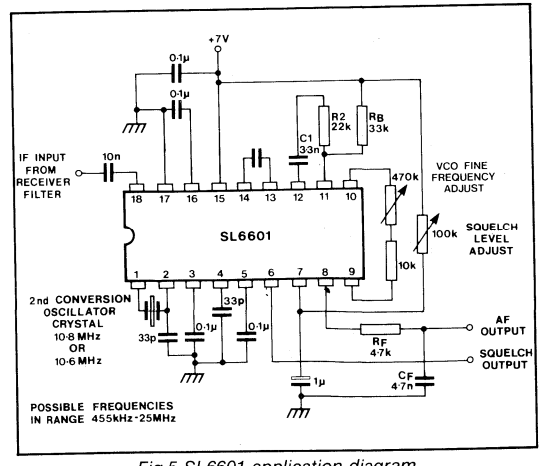


Fig.5 SL6601 application diagram
(1st IF = 10.7MHz, 2nd IF = 100kHz)

TYPICAL CHARACTERISTICS

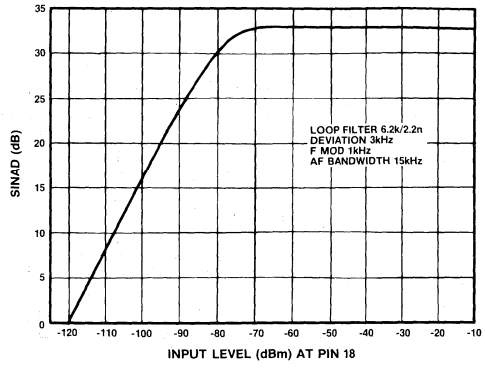


Fig.6 Typical SINAD
(signal + noise + distortion/noise + distortion)

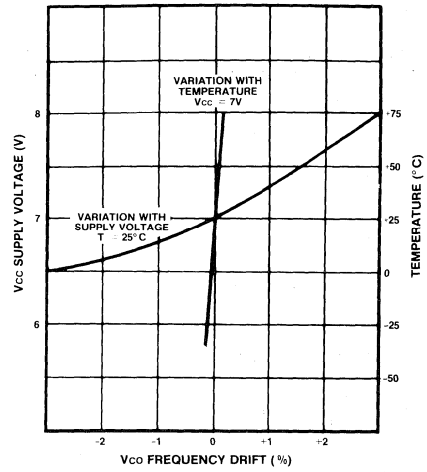


Fig.9 Typical VCO characteristics

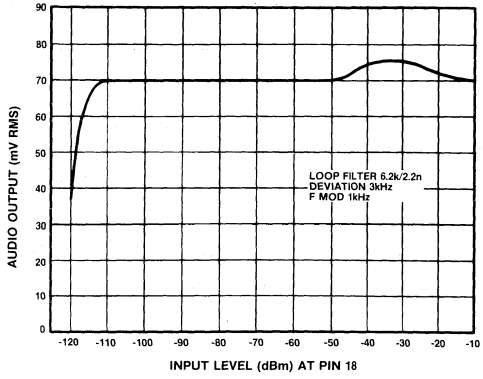


Fig.7 Typical recovered audio v. input level (3kHz deviation)

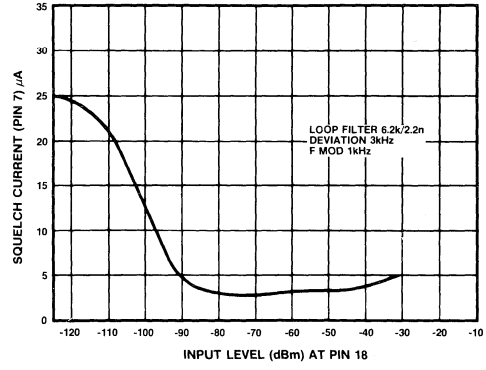


Fig.10 Typical squelch current v. input level

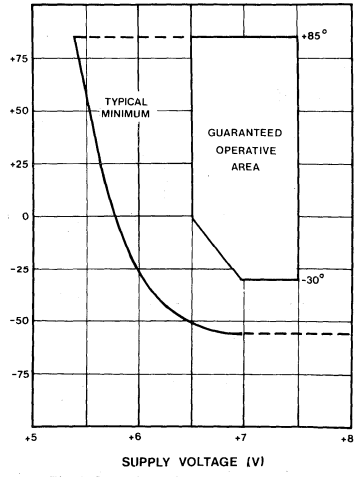


Fig.8 Supply voltage v. temperature

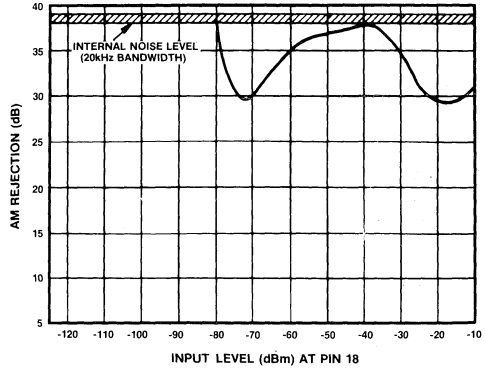


Fig.11 Typical AM rejection

(the ratio between the audio output produced by:
(a) a 3kHz deviation 1kHz modulation FM signal and
(b) a 30% modulated 1kHz modulation AM signal at the same input voltage level.)

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage Vcc : 7V

Input signal frequency: 10.7MHz, frequency modulated with a 1kHz tone with a ±2.5kHz frequency deviation

Ambient temperature: -30°C to +85°C; IF = 100kHz; AF bandwidth = 15kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		2.3	2.7	mA	
Input impedance	100		300	Ω	Source impedance = 200Ω
Input capacity	0.5	2.0	3.5	pF	
Maximum input voltage level	0.5			V rms	At pin 18
Sensitivity	5	2		μV rms	At pin 18 for S + N/N = 20dB
Audio output	35	90	140	mV rms	
Audio THD		1.3	3.0	%	1mV rms input at pin 18
S + N/N	30	50		dB	1mV rms input at pin 18
AM rejection	30	Note 1		dB	100μV rms input at pin 18, 30% AM
Squelch low level		0.2	0.5	V dc	20μV rms input at pin 18
Squelch high level	6.5	6.9		V dc	No input
Squelch hysteresis		1	6	dB	3μV input at pin 18
Noise figure		6		dB	50Ω source
Conversion gain		30		dB	Pin 18 to pin 4
Input gain compression		100		μV rms	Pin 18 to pin 4, 1dB compression
Squelch output load	250			kΩ	
Input voltage range	80	100		dB	At pin 8; above 20dB S + N/N
3rd order intercept point (input)		-38		dBm	Input pin 18, output pin 4
VCO frequency					
Grade 1	85		100	kHz	390pF timing capacitor } No input
Grade 2	95		110	kHz	390pF timing capacitor } No input
Grade 3	105		120	kHz	390pF timing capacitor } No input
Source impedance (pin 4)		25	40	kΩ	
AF output impedance		4	10	kΩ	
Lock-in dynamic range	±8			kHz	20μV to 1mV rms at pin 18
External LO drive level	50		250	mV rms	At pin 2
Crystal ESR			25	Ω	10.8MHz

APPLICATION NOTES

IF Amplifiers and Mixer

The SL6601 can be operated either in a 'straight through' mode with a maximum recommended input frequency of 800kHz or in a single conversion mode with an input frequency of 50MHz maximum and an IF of 100kHz or ten times the peak deviation, whichever is the larger. The crystal oscillator frequency can be equal to either the sum or difference of the two IF's; the exact frequency is not critical.

The circuit is designed to use series resonant fundamental crystals between 1 and 17MHz.

When a suitable crystal frequency is not available a fundamental crystal of one third of that frequency may be used, with some degradation in performance.

E.G. If an external oscillator is used the recommended level is 70mV rms and the unused pin should be left O/C. The input is AC coupled via a 0.01μF capacitor.

A capacitor connected between pin 4 and ground will shunt the mixer output and limit the frequency response of the mixer output and limit the frequency response of the input signal to the second IF amplifier. A value of 33pF is advised when the second IF frequency is 100kHz; 6.8pF is advised for 455kHz.

Phase Locked Loop

The Phase Locked Loop detector features a voltage controlled oscillator with nominal frequency set by an external capacitor equal to (40 ± 7)/f pF, where f is the VCO frequency in MHz. The nominal frequency may differ from the theoretical but there is provision for a fine frequency adjustment by means of a variable resistor between the VCO output pins; a value of 470k has negligible effect while 6.8k (recommended minimum value) increases the frequency by approximately 20%.

Care should be taken to ensure that the free running VCO frequency is correct; because the VCO and limiting IF amplifier output produce square waves, it is possible to obtain lock with the VCO frequency fractionally related to the IF, e.g. IF = 100kHz, VCO = 150kHz. This condition can produce good SINAD ratios but poor squelch performance.

The loop filter is connected between pins 11 and 12; a 33k resistor is also required between pin 11 and Vcc.

The values of the filter resistor R2 and capacitor C1 must be chosen so that the natural loop frequency and damping factor are suitable for the FM deviation and modulation bandwidth required. The recommended values for various conditions are tabulated below:

Centre frequency kHz	Deviation kHz	Resistor kΩ	Capacitor pF
100	5	6.2	2200
100	10	5.6	1800
455	5	4.7	1500
455	10	3.9	1200

Note that the values of loop filter are not critical and in many cases may be omitted.

The AF output voltage depends upon the % deviation and so, for a given deviation, output is inversely proportional to centre frequency. As the noise is constant, the signal to noise ratio is also inversely proportional to centre frequency.

VCO Frequency Grading

The SL6601 is supplied in 3 selections of VCO centre frequency. This frequency is measured with a 390pF timing capacitor and no input signal.

Devices are coded 'SL6601C' and a '/1', '/2', '/3' to indicate the selection.

Frequency tolerances are:

/1 85 - 100kHz (or uncoded)
/2 95 - 110kHz
/3 105 - 120kHz

Note that orders cannot be accepted for any particular selection, but all devices in a tube will be the same selection.

Squelch Facility

When inputs to the product detector differ in phase a series of current pulses will flow out of pin 7. The feature can be used to adjust the VCO; when a 1mV unmodulated input signal is applied to pin 18 the VCO frequency should be trimmed to maximise the voltage on pin 7.

The squelch level is adjusted by means of a preset variable resistor between pin 7 and V_{CC} to set the output signal to noise ratio at which it is required to mute the output. The capacitor between pin 7 and ground determines the squelch attack time. A value between 10nF and 10μF can be chosen to give the required characteristics.

Operation at signal to noise ratios outside the range 5-18dB is not recommended. Where the 'front end' noise is high (because of very high front end gain) the squelch may well never operate. This effect can be obviated by sensible receiver gain distribution.

The load on the squelch output (pin 6) should not be less than 250kΩ. Reduction of the load below this level leads to hysteresis problems in the squelch circuit.

The use of an external PNP transistor allows hysteresis to be increased. See Fig.4. The use of capacitors greater than 1000pF from pin 6 to ground is not recommended.

Outputs

High speed data outputs can be taken direct from pins 11 and 12 but normally for audio applications pin 8 is used. A filter network will be needed to restrict the audio bandwidth and an RC network consisting of 4.7kΩ and 4.7nF may be used.

Layout Techniques and Alignment

The SL6601 is not critical in PCB layout requirements except in the 'straight through' mode. In this mode, the input components and circuits should be isolated from the VCO components, as otherwise the VCO will attempt to 'lock' to itself, and the ultimate signal to noise ratio will suffer.

The recommended method of VCO adjustment is with a frequency measurement system on pin 9. The impedance must be high, and the VCO frequency is adjusted with no input signal.

LOOP FILTER DESIGN

The design of loop filters in PLL detectors is a straight forward process. In the case of the SL6601 this part of the circuit is non-critical, and in any case will be affected by variations in internal device parameters. The major area of importance is in ensuring that the loop bandwidth is not so low as to allow unlocking of the loop with modulation.

Damping Factor can be chosen for maximum flatness of frequency response or for minimum noise bandwidth, and values between 0.5 and 0.8 are satisfactory, 0.5 giving minimum noise bandwidth.

Design starts with an arbitrary choise of f_n, the natural loop frequency. By setting this at slightly higher than the maximum modulation frequency, the noise rejection can be slightly improved. The ratio f_m/f_n highest modulating frequency to loop frequency can then be evaluated.

From the graph, Fig.3 the value of the function

$$\frac{\Phi_e f_n}{\Delta f}$$

can be established for the desired damping factor.

Φ_e - peak phase error
f_n - loop natural frequency
Δf - maximum deviation of the input signal

and as f_n and Δf are known, Φ_e is easily calculated. Values for Φ_e should be chosen such that the error in phase is between 0.5 and 1 radian. This is because the phase detector limits at $\pm\pi/2$ radians and is non linear approaching these points. Using a very small peak phase error means that the output from the phase detector is low, and thus impairs the signal to noise ratio. Thus the choice of a compromise value, and 0.5 to 1 radian is used. If the value of Φ_e achieved is far removed from this value, a new value of f_n should be chosen and the process repeated.

With f_n and D established, the time constants are derived from

$$t_1 + t_2 = \frac{K_o K_D}{(2\pi f_n)^2}$$

$$\text{and } t_2 = \frac{D}{\pi f_n} - \frac{1}{K_o K_D}$$

K_oK_D is $0.3f_o$, where f_o is the operating frequency of the VCO. t_1 is fixed by the capacitor and an internal 20kΩ resistor: t_2 is fixed by the capacitor and external resistor.

$$\text{so } C = \frac{t_1}{2C \times 10^3}$$

$$\text{and } R_{ext} = \frac{t_2 \times 20 \times 10^3}{t_1}$$

In order that standard values may be used, it is better to establish a value of C and use the next lowest standard value e.g. $C_{calc} = 238pF$, use 220pF, as it is better to widen the loop bandwidth rather than narrow it.

The value of R_{ext} is then 'rounded up' by a similar process. It is, however, better to increase R_{ext} to the nearest preferred value as loop bandwidth is proportional (R_{ext}) – ½ while damping factor is proportional to R: thus damping factor is increasing more quickly which gives a more level response.

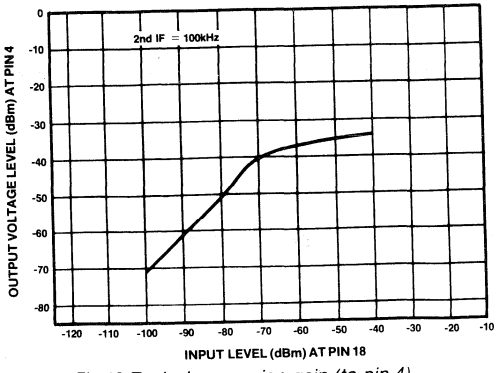


Fig.12 Typical conversion gain (to pin 4)

ABSOLUTE MAXIMUM RATINGS

Supply voltage	9V
Storage temperature	-55° C to +125° C (DP package)
	-55° C to +150° C (DG)
Operating temperature	-55° C to +125° C
(see Electrical Characteristics)	
Input voltage	1V RMS at pin 18

PLESSEY
Semiconductors

SL6638

200MHz DIRECT CONVERSION FSK DATA RECEIVER

The SL6638 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

FEATURES

- Very Low Power Operation - Typ. 4mW
- Single Cell Operation
- Complete Radio Receiver in One Package
- Operation Optimised at 200MHz
- 200nV Typical Sensitivity
- Operates at 1200 BPS

APPLICATIONS

- Low Power Radio Data Receiver
- Radio Paging
- Ultrasonic Direction Indication
- Security Systems

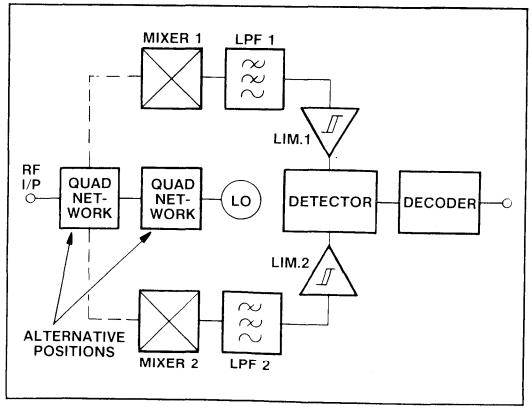
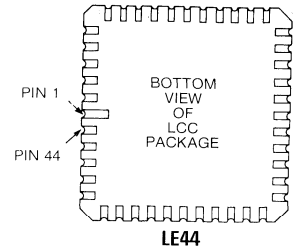


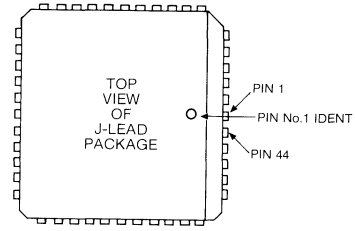
Fig.2 Block diagram (see Fig.5 for detailed schematic)

If waveform at limiter '1' input leads waveform on limiter '2' input by 90°, output at detector output will be a high level and low at decoder output.

If waveform at limiter '1' input lags waveform on limiter '2' input by 90°, output at detector output will be a low level and high at decoder output.



LE44



HP44

PIN	FUNCTION	PIN	FUNCTION
1	Detector O/P	23	Mixer 1 O/P
2	Decoder I/P	24	Power Down
3	Data Ground	25	Vcc2
4	LF Bias Decouple	26	Ground
5	Limiter '1' FB Decouple	27	Ground (Beep)
6	Limiter '1' I/P	28	Low Battery Control
7	Follower Filter O/P	29	Beep O/P
8	Follower Filter I/P	30	Beep Vcc1
9	Amplifier Filter O/P	31	Beep I/P
10	Amplifier Filter I/P	32	Mixer '2' RF I/P
11	Current Source Control (2)	33	Mixer '1' RF I/P
		34	Amplifier Filter I/P
12	Current Source O/P (2)	35	Amplifier Filter O/P
13	Battery Flag	36	Follower Filter I/P
14	Osc.Current Source O/P(1)	37	Follower Filter O/P
15	Mixer '1' LO I/P	38	RF Bias Decouple
16	Mixer '2' LO I/P	39	RF Amplifier O/P
17	Mixer Bias	40	RF Ground
18	Inverter Control O/P	41	RF I/P
19	Reference O/P	42	Limiter '2' I/P
20	Vcc1	43	Limiter '2' FB Decouple
21	Inverter Control Threshold Adjust	44	Decoder O/P
22	Mixer 2 O/P		

Fig.1 Pin connections

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.2) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.3. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.3 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

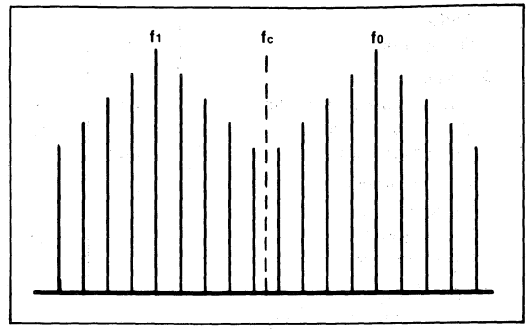


Fig.3 Spectrum diagram

ELECTRICAL CHARACTERISTICS (Use with test circuit Fig.4)

Test conditions: V_{CC1} = 1.3V V_{CC2} = 2.3V T_{amb} = -20°C to +60°C

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply voltage V_{CC1}	20	0.9		3.5	V	
Supply voltage V_{CC2}	25	1.8		3.5	V	
Supply current I_{CC1}	12,14,15, 16,17,20, 39	0.6	0.8	1.0	mA	Beep off Pin 11 unconnected
Supply current I_{CC2}	25	0.82	1.23	1.64	mA	
Powered-down I_{CC2}	25	60	115	150	μA	
RF amplifier						
Supply current (I_{RF})	39	400	500	650	μA	Pin 40 at 0V
Noise figure			5.5		dB	R_S = 50Ω
Oscillator						
Current source value (I_{OSC1})	14	200	250	350	μA	
Current source value (I_{OSC2})	12	200	250	350	μA	Pin 11 at 0V
Mixers						
Conversion gain		17	21	25	dB	10mV rms signal 10mV rms local oscillator
Input impedance	32,33		500		Ω	
Active filter	10,9					
Inverting amplifiers	34,35					
Input noise			20		nV/√Hz	
Open loop gain			40		dB	Tested as active filters
Input impedance			1		MΩ	using applications CCT
Output impedance			800		Ω	
Active filter	8,7					
Buffer amplifiers	36,37					
Gain			1		v/v	
Input impedance			20		kΩ	
Output impedance			1		kΩ	
Limiting amplifier						
Input impedance	6,42		50		kΩ	
Sensitivity	6,42		20	40	μV	Bit error of 1 in 30 5kHz deviation 500 bps

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Detector						
Output current	1		±5		μA	
Decoder						
Output mark-space ratio	44	7:9		9:7		40μV at limiter input
Output logic high	44	85			% V_{CC2}	
Output logic low	44			15	% V_{CC2}	
Battery economy	24					
Input current				1	μA	
Input logic high		1.5			V	Powered down
Input logic low				0.7	V	Powered up
Beeper driver						
Output saturation voltage	29			300	mV	I load = 50mA
Input current	31			1	μA	
Input logic high	31	1.5			V	Beep on
Input logic low	31			0.7	V	Beep off
Band-gap reference						
Output voltage	19	1.00	1.10	1.25	V	
Battery flag	13					
Output high level		85			% V_{CC2}	Battery high
Output low level				15	% V_{CC2}	Battery low
Flag trigger level		0.9		1.1	V	
Inverter control	18					
V_{CC2} voltage control level		2		2.4	V	Pin 21 unadjusted
Inverter output current			200		μA	Sourced from pin 18
Low battery control	28					
Input logic high		1.5			V	Removes beep drive if battery low
Input logic low				0.7	V	Connects beep drive
Input current				1	μA	

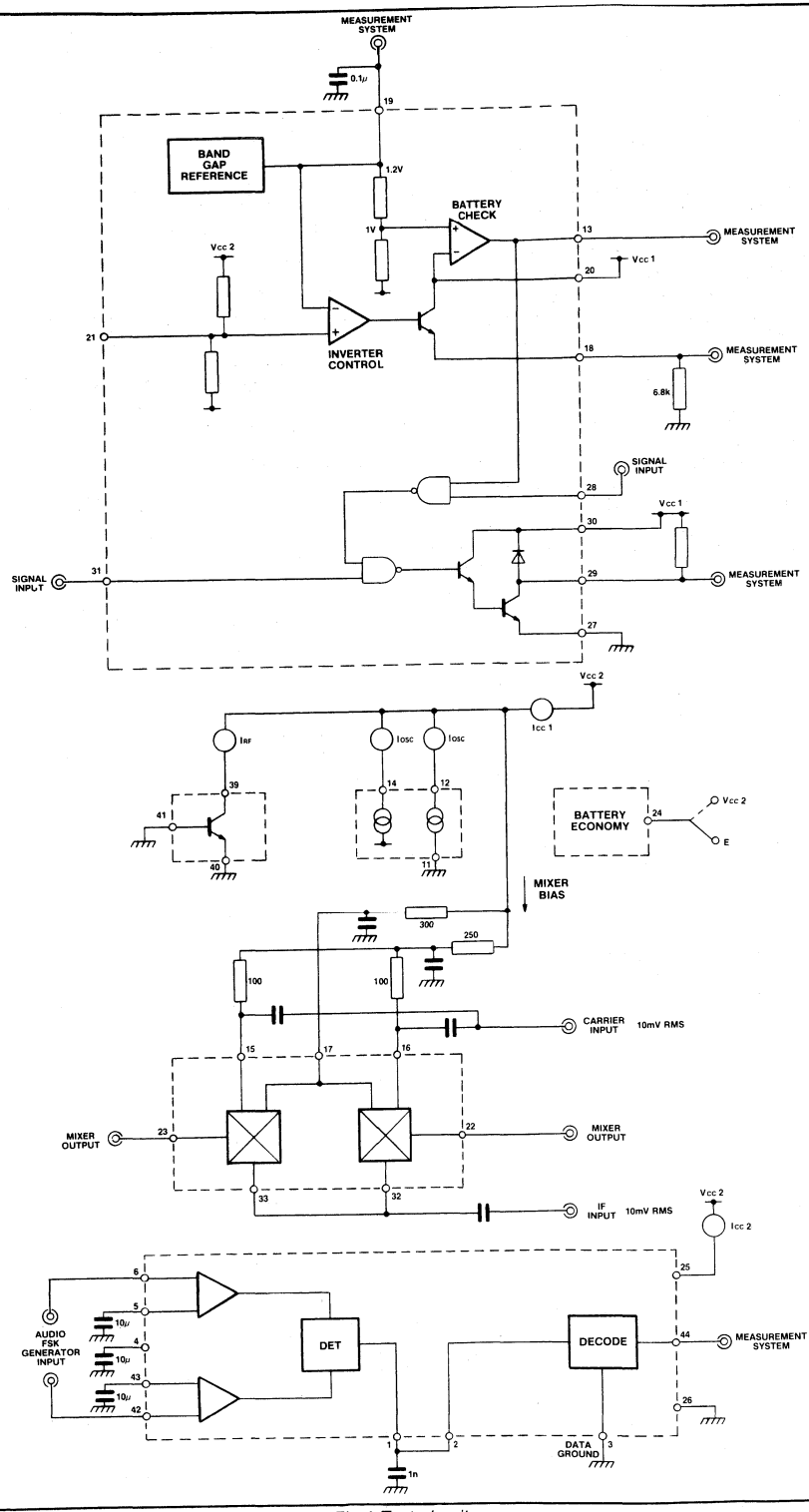


Fig.4 Test circuits

DETAILED DESCRIPTION

The schematic diagram of the SL6638 is shown in Fig.5. The various sub-sections will be described in more detail.

RF amplifier

The RF amplifier consists of a low noise transistor with a high f_t operating at a current of 500μA. It is arranged with a separate emitter connection to ensure stability, and to minimise noise introduction through common return impedances. The collector of this stage is uncommitted for maximum flexibility (transistor c, b, e on pins 39, 41 and 40 respectively) and is biased from a current mirror. The power-down circuitry removes bias from this stage in the standby condition. Typical parameters for this transistor are $\beta \simeq 100$, $rbb' \simeq 100\Omega$ and $f_t \simeq 1.2$GHz.

Mixers

The mixers are single balanced active mixers using a PNP current mirror as an active load. Inputs to the mixer are on pins 33 and 32 for the signal, and pins 15 and 16 for the LO. Pin 17 is the LO injection common point and may either be a common but 'live' point when the phase quadrature is used in the RF path or bypassed when quadrature LO drive to the mixers is employed. Emitter follower outputs on pins 23 and 22 ensure that mixer gain is unaffected by the load impedance. The mixers are also powered down on standby.

Local oscillator

A current source on pin 14 and a switchable current source on pin 12 are available for use in a local oscillator.

Inverting amplifiers

The inverting amplifiers have high gain (40dB open loop) and are for use in active low pass filters. The open loop gain is high and is not defined with any accuracy, as closed loop gain is defined by the external filter components.

Buffers

The buffer stages are x1 amplifiers for use in the active low pass filters.

Limiting amplifiers and detectors

These amplifiers provide the main gain block of the receiver system. An input of about 6μV provides limiting, and the inputs are to pins 6 and 42. Pins 4, 5 and 43 are bypass points for the amplifier bias points, while pin 1 is the digital output from the phase detector.

Decoder

The decoders function is to act as a low pass filter to the modulation frequency, and may be configured as an active LPF if desired. It should however, be designed as a very high impedance active LPF as the drive from the detectors is at a high impedance. Alternatively, the connection of a small capacitor to ground from the input is generally adequate for most applications.

Beeper drive

The beeper drive stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA, and the arrangement is such that the output waveform may be modified when the battery is near end of life. This modified waveform is generated externally (and applied to pin 28). The internal band gap reference is 1.2V and this is divided down to a suitable voltage.

Inverter control

This output is available (on pin 18) to control an external inverter. It is derived from the ratio of the internal reference to the V_{CC2} line, and moves in phase with changes in the V_{CC2} line.

Pin 21 allows the value of the inverted voltage supply to be adjusted.

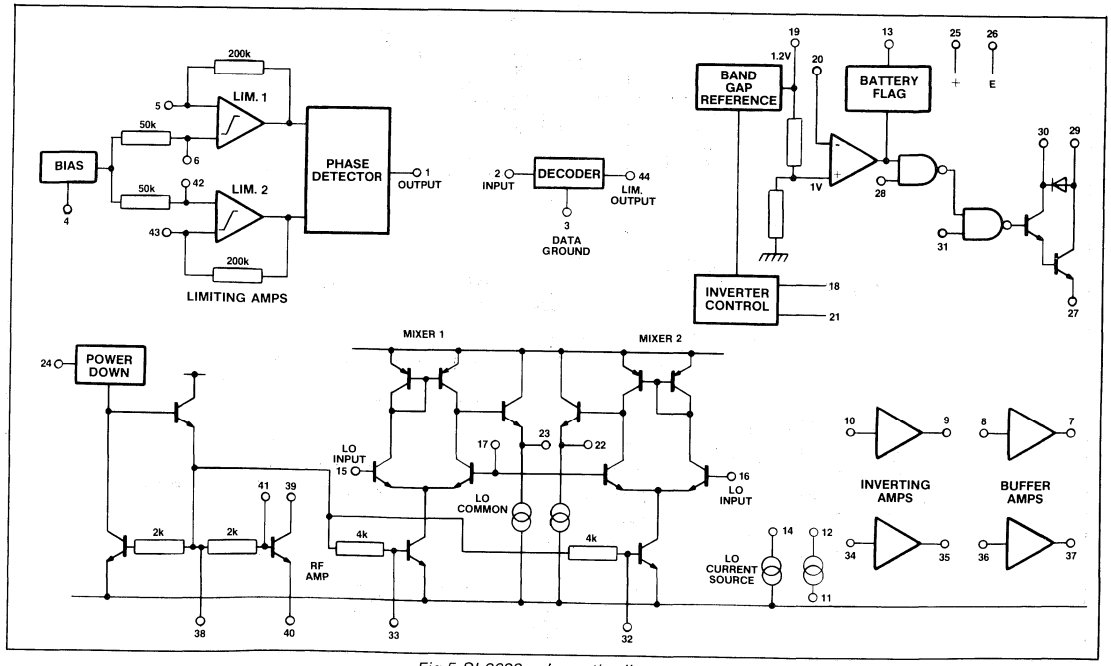


Fig.5 SL6638 schematic diagram

APPLICATIONS

The SL6638 is intended for applications at low data rates and high deviation (e.g. 512 and 1200 B.P.S. and ±4.5kHz deviation). Operation at a ratio of deviation to data rate of less than 6 is not recommended.

The choice of circuitry is dependent upon the system requirements. For example, operation from a single Leclanche or alkaline cell at a nominal 1.4V requires the use of an external inverter, while operation from a single 3 volt Lithium cell does not.

In the radio receiver application, a major decision is the positioning of the quadrature phase shift network. This network may be in the RF or the local oscillator paths, and each method has its advantages and disadvantages. Briefly, these are as follows:

1. **Local oscillator path.** This enables minimum RF loss to be attained. It requires a higher LO drive power to overcome the inevitable losses in the phasing network.
2. **RF signal path.** This method has the advantage that greater isolation may be achieved from the signal to the local oscillator - see Fig.6.

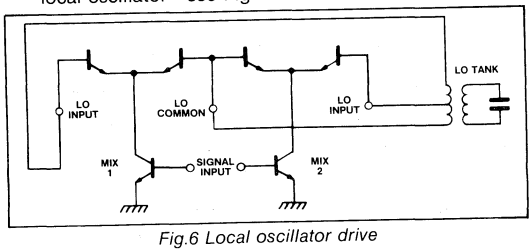


Fig.6 Local oscillator drive

The common mode rejection of the differential stages is used to its maximum advantage in this arrangement.

The form of the quadrature network is not critical. However, the use of an RC network as in Fig.7 has the disadvantage at VHF of being more subject to stray capacities than other methods.

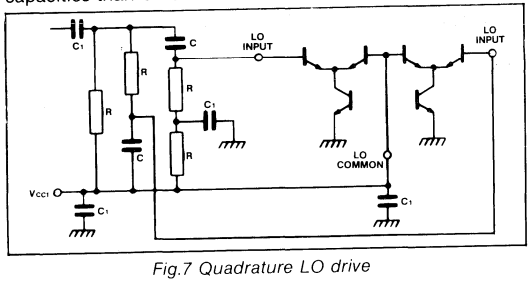


Fig.7 Quadrature LO drive

In the circuit of Fig.7, C_1 is a bypass capacitor, while $X_C = R$ at the operating frequency. Note that the resistances between the local oscillator inputs are equal to minimise DC offsets. The quadrature network can be achieved by coupled circuits (Fig.8) or a hybrid network (Fig.10).

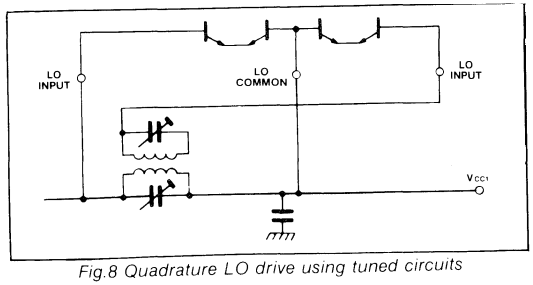


Fig.8 Quadrature LO drive using tuned circuits

In the method shown in Fig.8, the tuned circuits are adjusted to resonance, and are then detuned, one HF and the other LF, to achieve a 3dB drop in output from each one. This gives a +45° and -45° relative phase shift.

The quadrature hybrid network is well covered in the literature and is shown in Fig.9.

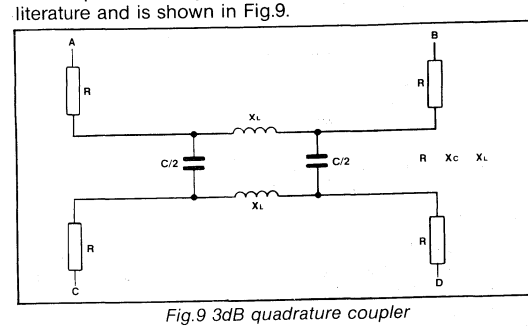


Fig.9 3dB quadrature coupler

The phase relationships are (A) input, (B) 90°, (C) 0° and (D) isolated. The circuit of Fig.10 may be used.

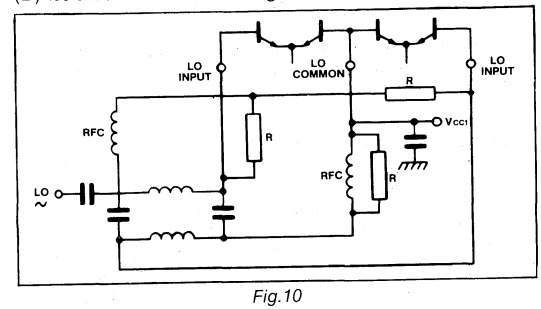


Fig.10

With a suitable local oscillator design some simplification occurs. In addition, it is possible to omit the resistors terminating the hybrid junction, although some mismatch then occurs.

Local oscillator

Because of the wide frequency range over which the SL6638 will operate, it is not possible to define which oscillator to use. Because of this, the oscillator provision is two uncommitted current sources which allows maximum flexibility. A typical overtone oscillator is shown in Fig.11.

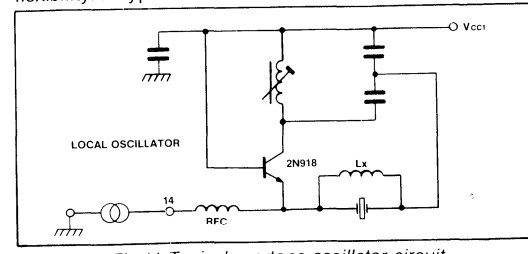


Fig.11 Typical overtone oscillator circuit

L_X is necessary with higher order overtone crystals to suppress oscillation at either the fundamental crystal frequency or as a form of Colpitts with no relation to the crystal frequency.

For lower frequencies, a simple oscillator may well be adequate as shown in Fig.12.

The choice of oscillator and quadrature network are dependent upon the application and no hard and fast rules can be formulated.

SL6638

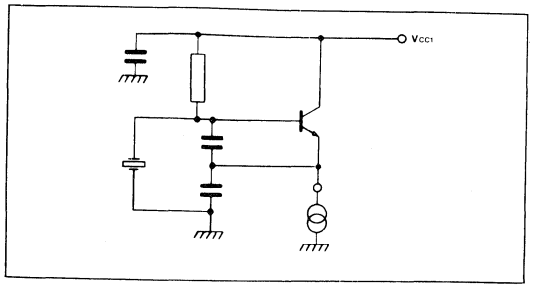


Fig.12 Fundamental LO circuit

Active filters

In any direct conversion receiver, the active filters provide the primary receiver selectively. The attenuation on the adjacent channel must be sufficient to prevent the limiting amplifiers from being driven into limiting by the unwanted signal; provided that this does not occur, then an adjacent channel signal has no effect.

The filter amplifiers consist of two stages for each channel, viz:

(a) An inverting amplifier with an open loop gain of about 40dB, and a gain-bandwidth product of 50kHz.

(b) A buffer stage with a x1 non-inverting gain.

Any of the standard variations of low pass filter can be used; however, design should ensure that differential group delay between the maximum possible error in mark and space frequencies is not excessive. The error in mark and space frequencies is caused by errors in the LO and received frequencies; an error in these frequencies leads to mark and space conditions producing different frequencies, and it is the differential group delay between these frequencies that must be minimised. This is especially important at data rates which are high in comparision with the deviation i.e. low values of modulation index m.

Decoder

The decoder may be connected as an active filter. It should however be a group delay equalised ('linear phase') filter, and the input capacitance should be minimised, as it is driven from a high impedance at the output of the detectors. It is perfectly satisfactory, however, to connect a 1000pF capacitor from the detector output to ground for bit rates up to 512 B.P.S.

Beeper drive

This output has a high current drive capability, suitable for driving beepers in pagers, or as a relay driver in other applications (Fig.13).

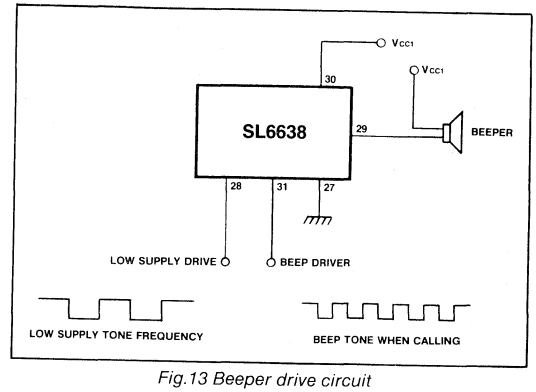


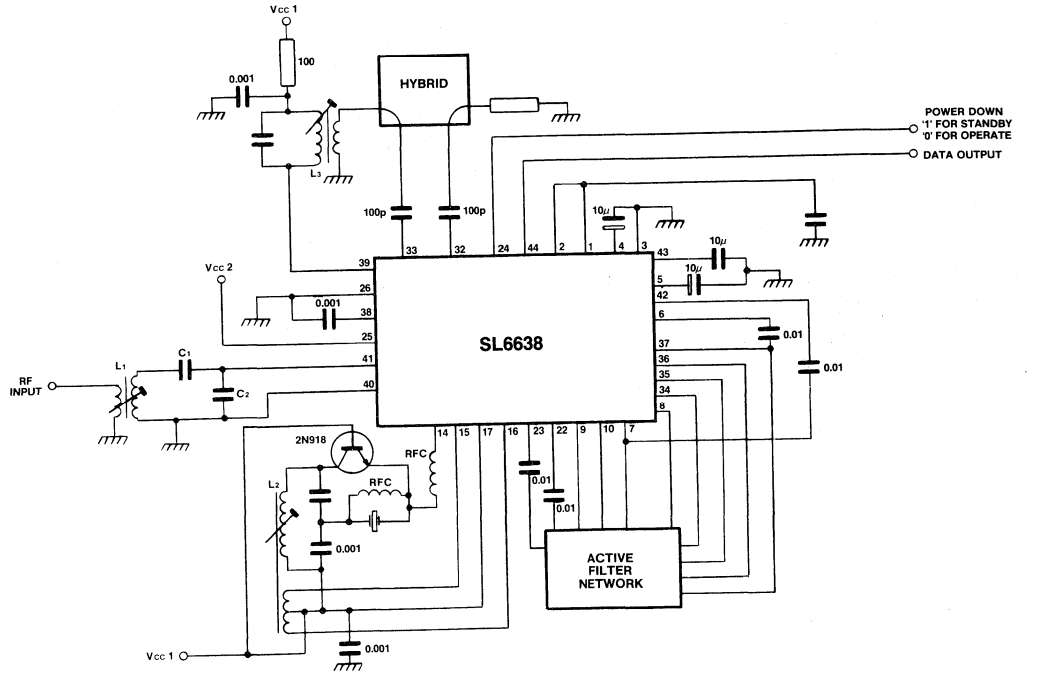
Fig.13 Beeper drive circuit

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

The circuit allows for a modification of the beep output when the battery flag has operated. The low battery control pin 28 has no effect whilst the battery is high. When the battery is low pin 28 will override the beep input, a logic high will remove beep drive and a logic low will connect beep drive. Therefore wiring pin 28 high will stop the beeper when the battery is flat, while wiring a logic low on pin 28 will cause the beeper to ignore the battery flag. Putting a low frequency on pin 28 will modulate the beep tone giving a warbling effect when the battery is flat.

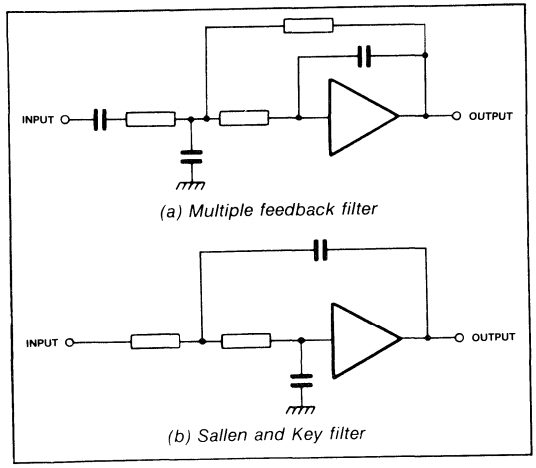
Typical application

Fig.14 shows a typical application as an FSK receiver for 512bps with a frequency deviation of ±4.5kHz. Typical sensitivity is of the order of 0.2μV for a 1 in 30 ber (bit error rate). The circuit as shown in Fig.13 uses a 9th overtone crystal and is usable to approximately 180MHz.



NOTES
Circuits L_1, C_1, C_2, L_2, L_3, resonate at the operating frequency. RFC1 suppresses oscillation at the crystal fundamental. RF level at pins 15 and 16 should be 10-20mV rms. For active filter network design, see Fig.15.

Fig.14 Typical application



(a) Multiple feedback filter

(b) Sallen and Key filter

Fig.15 Active filters. Component values may be determined from the standard books on active filter design.

The RF level at pins 15 and 16 can be increased which will increase the gain, but care must be taken with re-radiation from the input.

Operation at higher or lower frequencies is possible with appropriate external components.

USE OF SL6638 FROM ONE SUPPLY

For minimum power dissipation the SL6638 should be used with one cell (V_{CC1}) and an inverter (V_{CC2}). To operate from just one supply (V_C) certain precautions need to be taken.

Pin 25 will now be connected to Vc. Pins 12,14,39 can be returned to Vc through the same components as for two supply operation. Pins 15,16,17 are normally biased from V_{CC1} and cannot be connected directly to Vc. One diode volt drop down from the supply Vc is usually sufficient,see Fig.16.

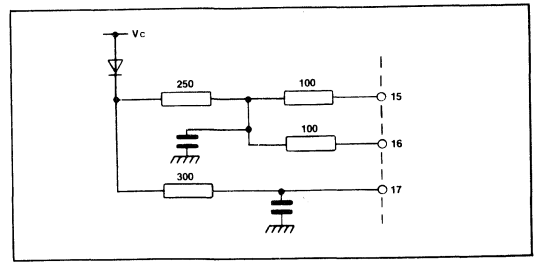


Fig.16

Pin 20 is usually connected to V_{CC1} when it is used to supply current to the inverter circuit and as an input to the battery check. For single voltage operation the inverter will not be required therefore pin 18 can be wired to Vc to disable the inverter. Pin 20 can still be used as a battery check by potting down the supply to pin 20, see Fig.17.

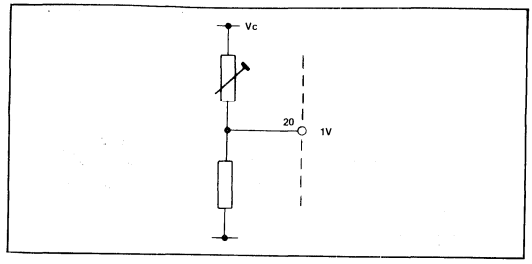


Fig.17

Pins 29,30 of the beeper driver are normally connected to V_{CC1}. These can be connected to Vc but the driver to the output transistor may then be excessive in any particular application. To reduce the drive a resistor may be included from pin 30 to Vc, see Fig.18.

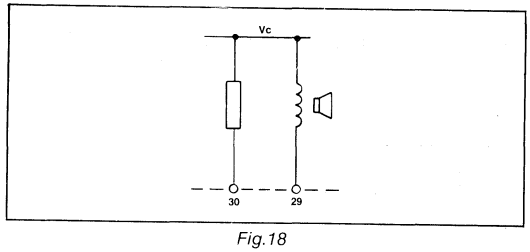


Fig.18

BATTERY ECONOMY

Function	Battery economised
RF amplifier	Yes
Osc current sources	Yes
Mixers	Yes
Active filters	Yes
Limiting amplifiers	No
Phase detector	Yes
Decoder	Yes
Band-gap reference	No
Battery check/flag	No
Inverter control	No
Low battery control	No
Beeper driver	No

Functions that are economised above will have their bias removed during power-down. Functions that are not economised will not be affected during power-down.

PLESSEY
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SL6652

LOWER POWER IF (AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6652 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

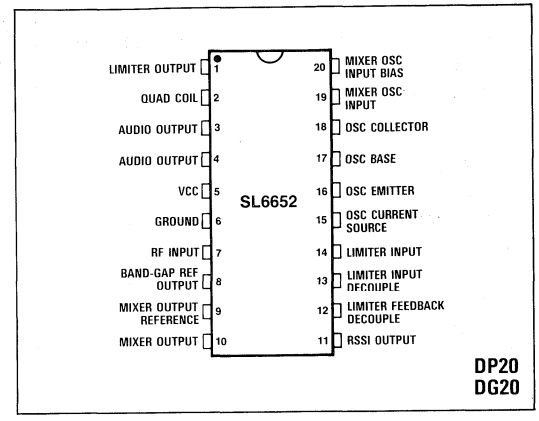

Fig.1 Pin connections (top view)

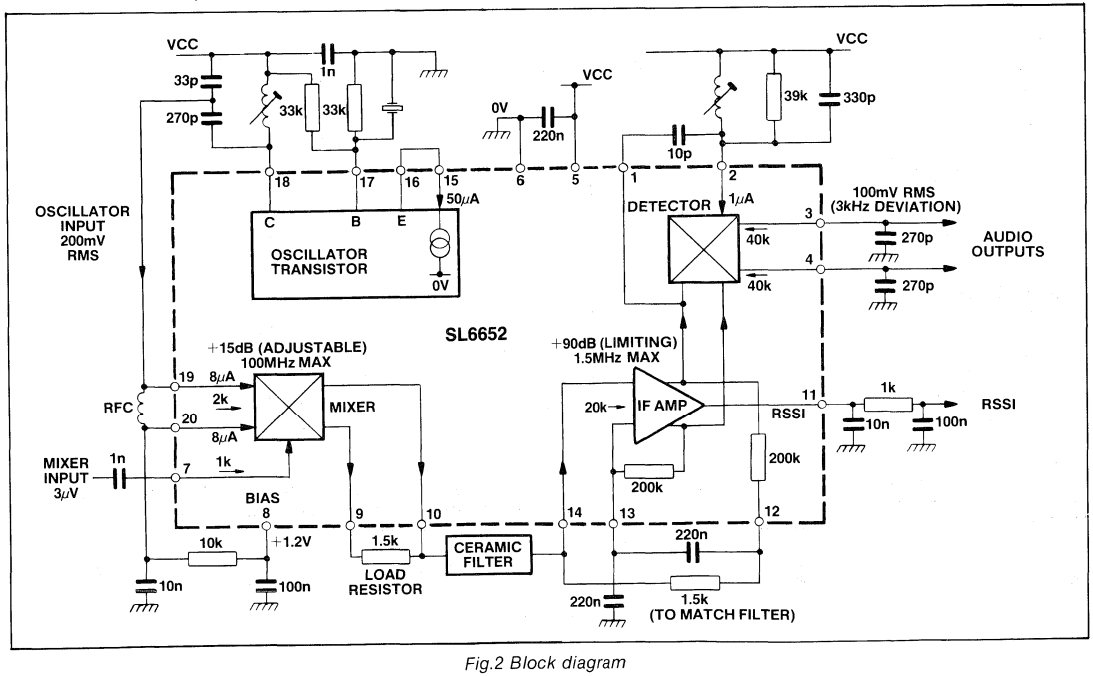

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30°C to +85°C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input <500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25°C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25°C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	5mV into pin 14
THD		0.5	5	%	5mV into pin 14
Output impedance		40		kohm	
Inter-output isolation		65		dB	1kHz
RSSI Output(T_{amb} = +25°C)					
Output current			20	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20°C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

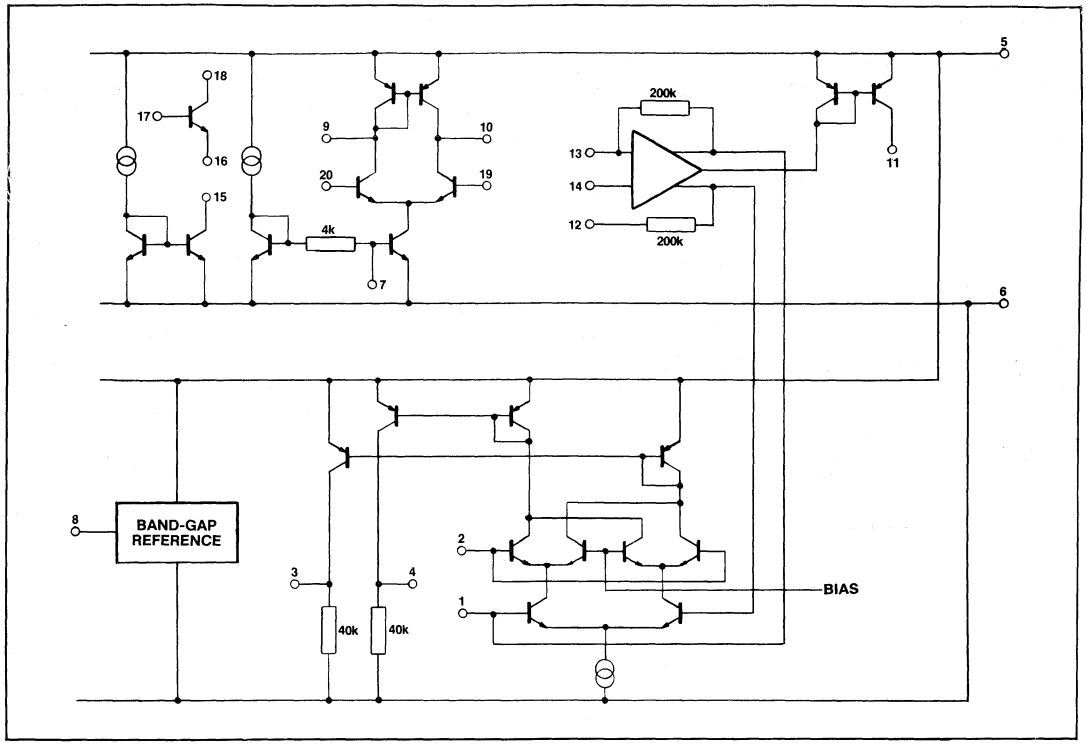

Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6652 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with differential AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor and a separate current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network. A differential output is provided to feed a comparator for digital use, although it can also be used to provide AFC.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6652 will operate reliably from 2.5V to 7.5V The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

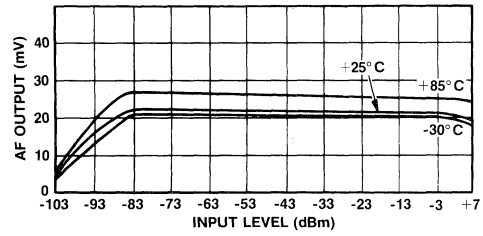

Fig.4 Audio output vs input and temperature at 2.5V

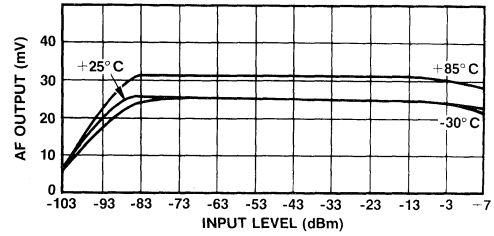

Fig.5 Audio output vs input and temperature at 5.0V

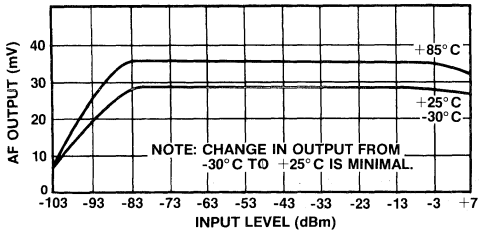

Fig.6 Audio output vs input and temperature at +7.5V

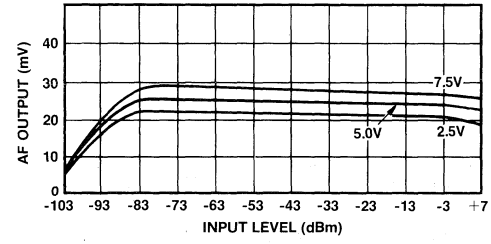

Fig.7 Audio output vs input and supply voltage at +25° C

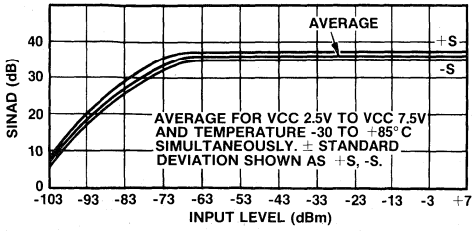

Fig.8 SINAD and input level

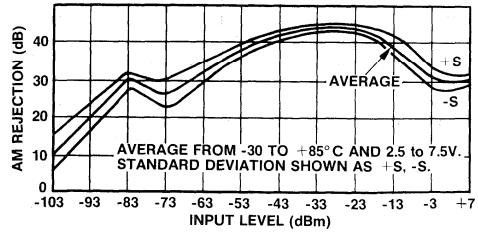

Fig.9 AM rejection and input level

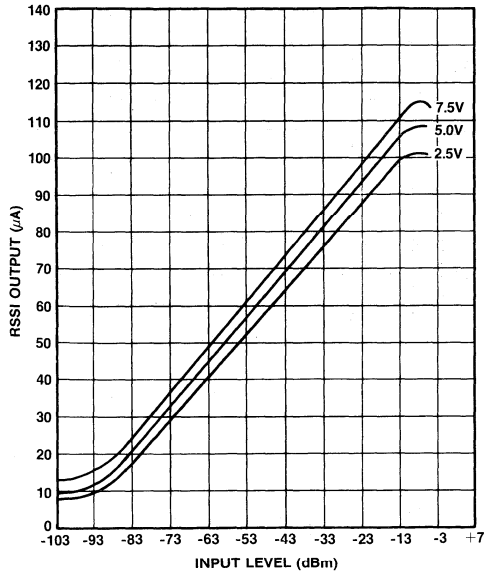

Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

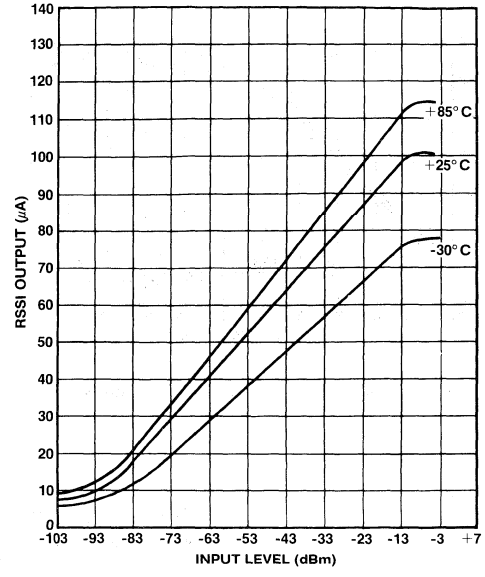

Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

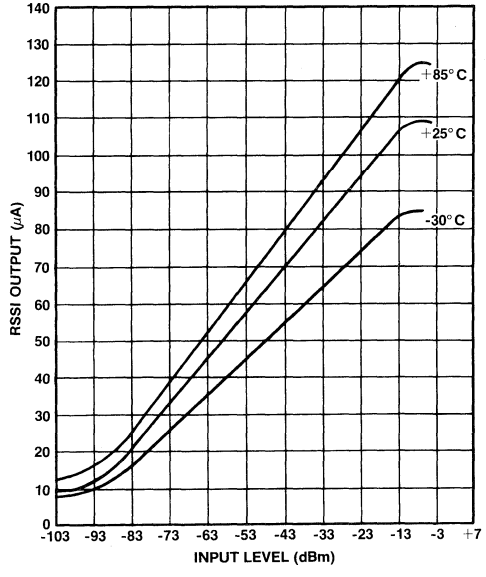

Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

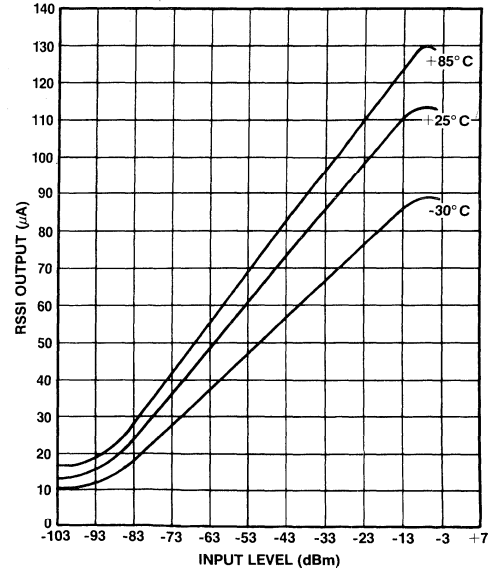

Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

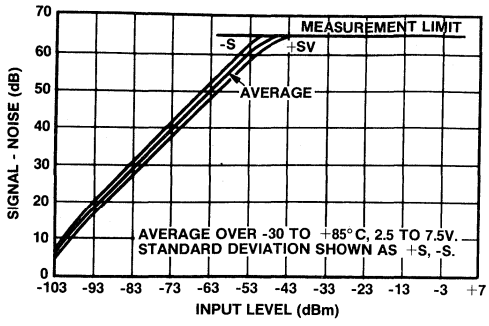

Fig.14 Signal + noise to noise ratio vs input level

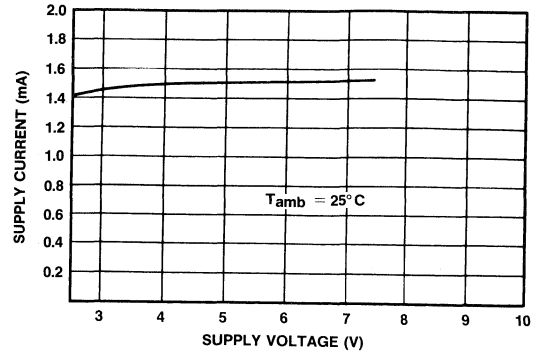

Fig.15 Supply current vs supply voltage

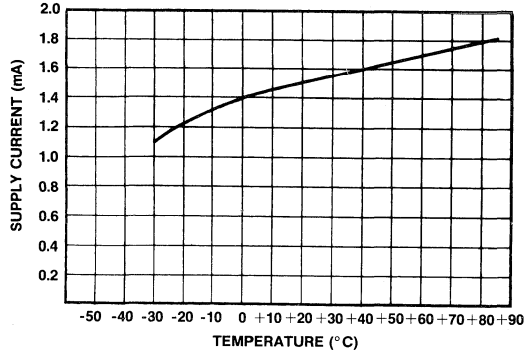

Fig.16 Supply current vs temperature (V_{CC} = 5V)

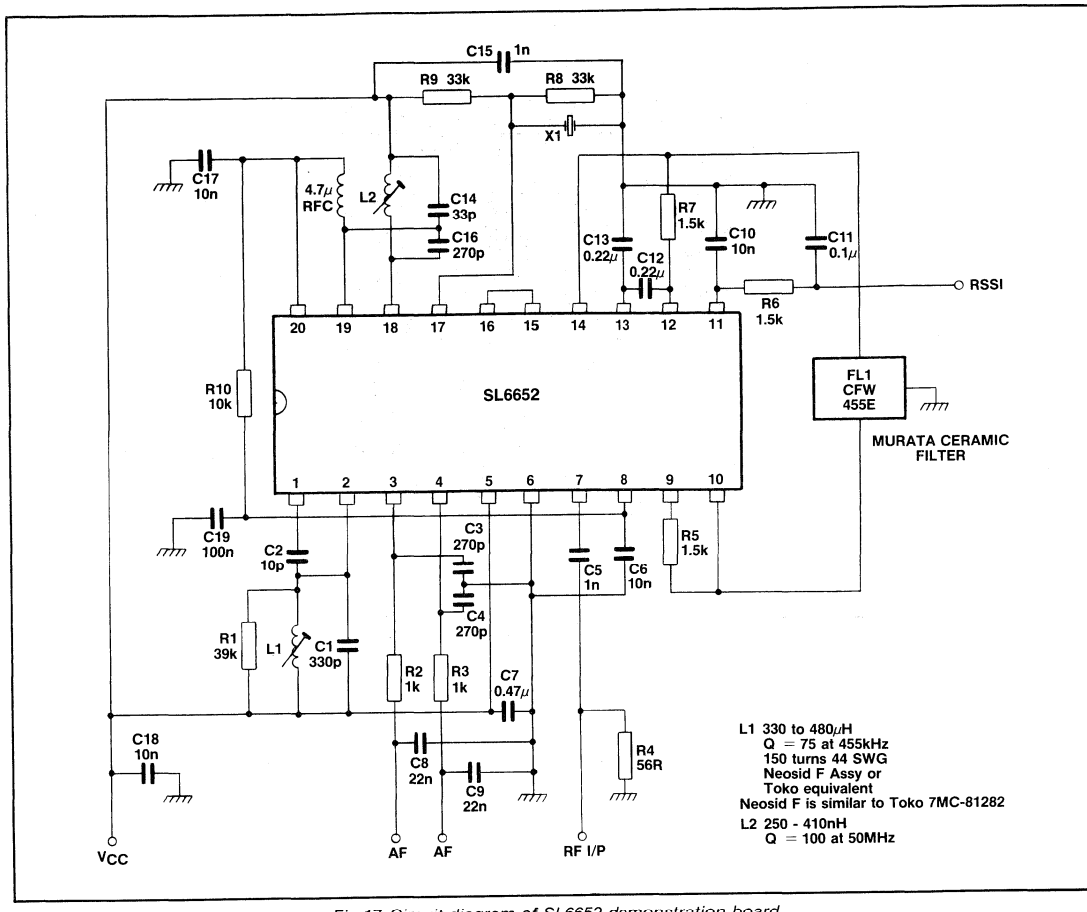

Fig.17 Circuit diagram of SL6652 demonstration board

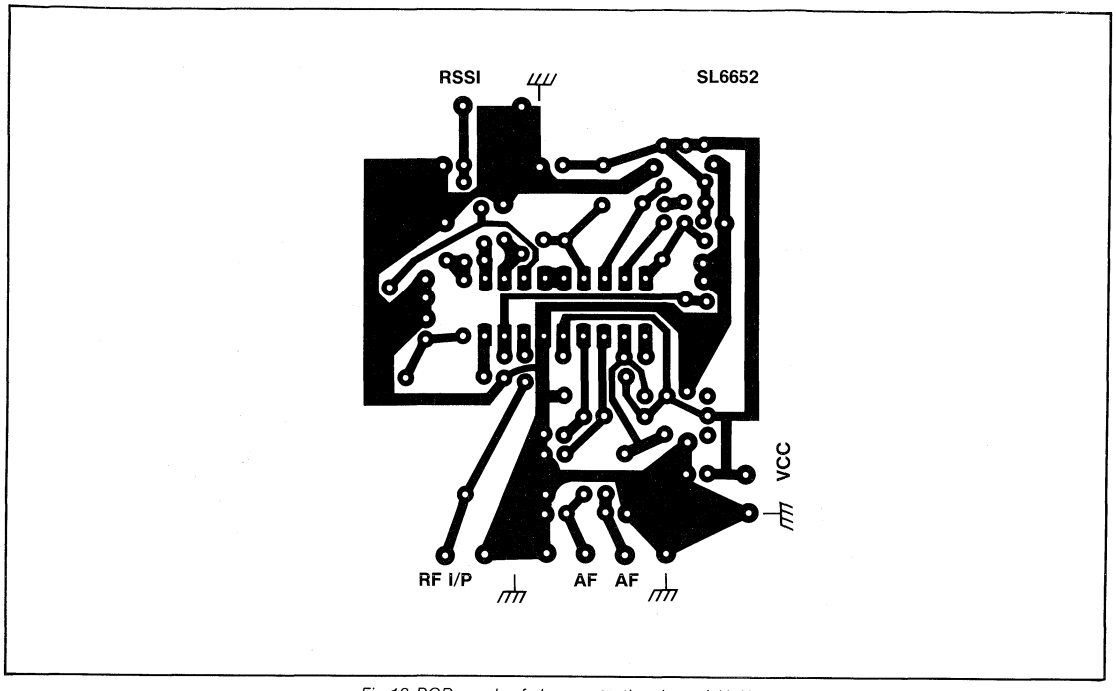

Fig.18 PCB mask of demonstration board (1:1)

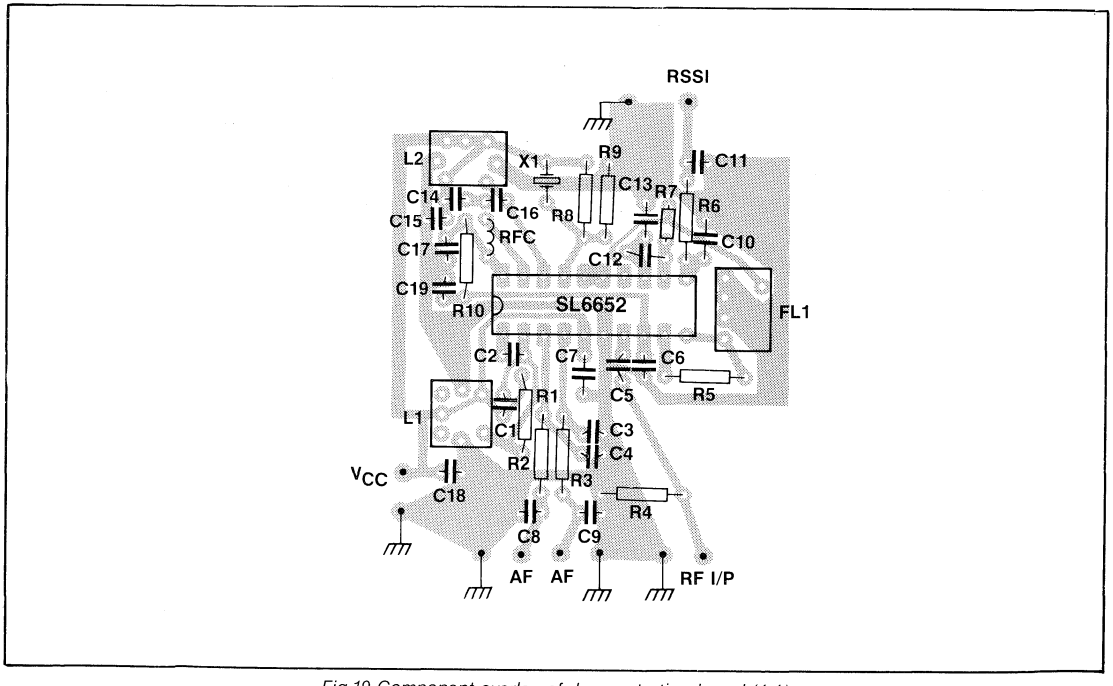

Fig.19 Component overlay of demonstration board (1:1)

PLESSEY
Semiconductors

SL6653

LOW POWER IF/AF CIRCUIT FOR FM RECEIVERS

The SL6653 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V

The SL6653 affords maximum flexibility in design and use. It is supplied in a dual-in-line plastic package.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation

APPLICATIONS

- Mobile Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply voltage 2.5V to 7.5V
- Sensitivity 3μV

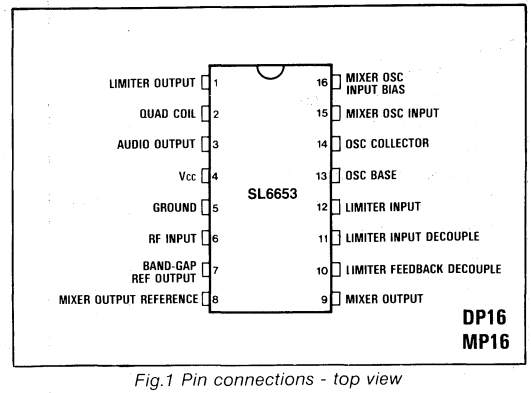

Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

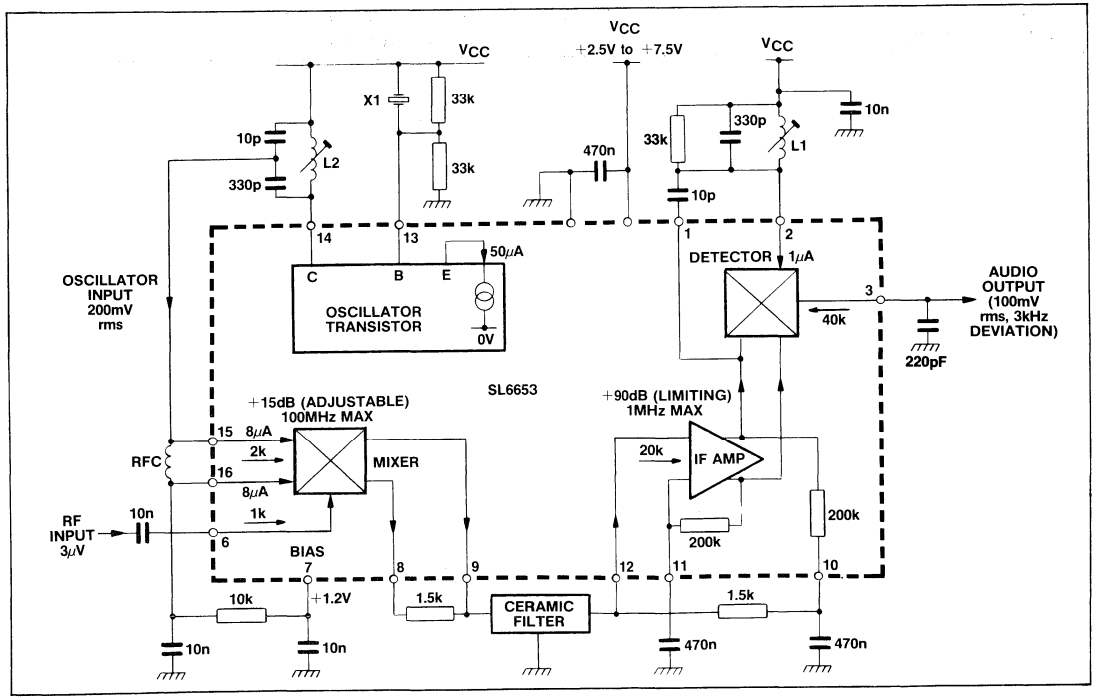

Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, Mod.Freq. = 1kHz, Deviation = 2.5kHz, Quadrature Circuit Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		30		dB	RF input < 500μV
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	
Ultimate S/N ratio		60		dB	10mV into pin 12
THD		0.5	5	%	
Output impedance		40		kohm	

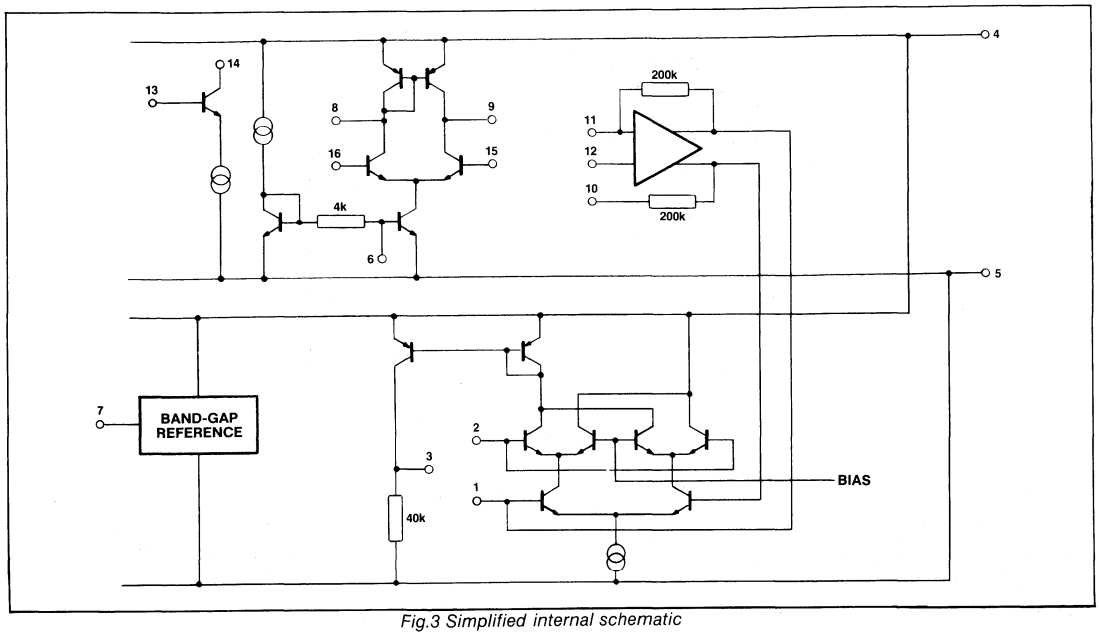

Fig.3 Simplified internal schematic

GENERAL DESCRIPTION

The SL6653 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- A transistor for use as an oscillator
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of a transistor and a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter.

Detector

A conventional quadrature detector is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

Supply voltage

The SL6653 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

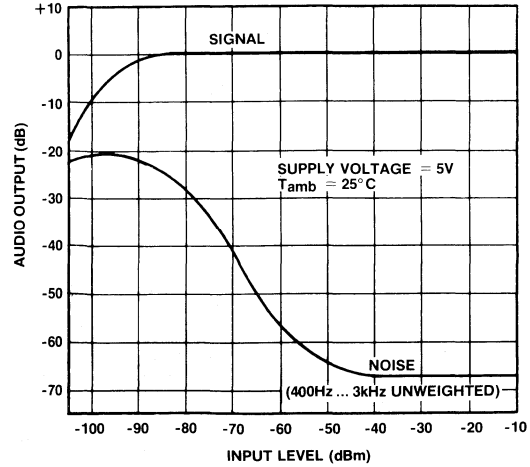

Fig.4 Audio and noise outputs vs input level

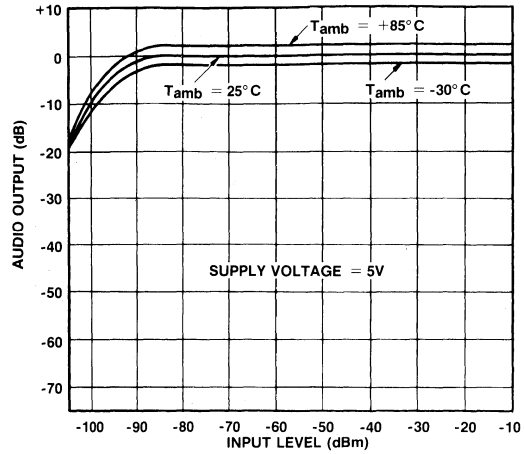

Fig.5 Audio output vs temperature

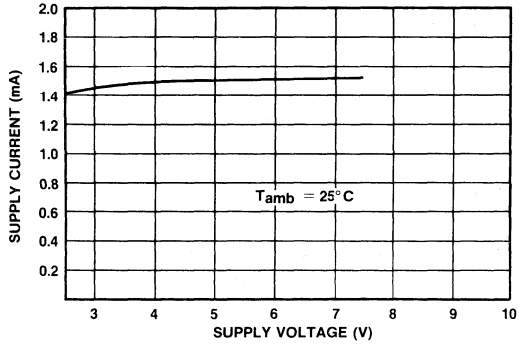

Fig.6 Supply current vs supply voltage

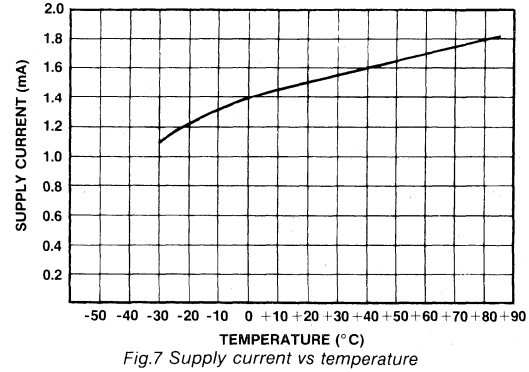

Fig.7 Supply current vs temperature

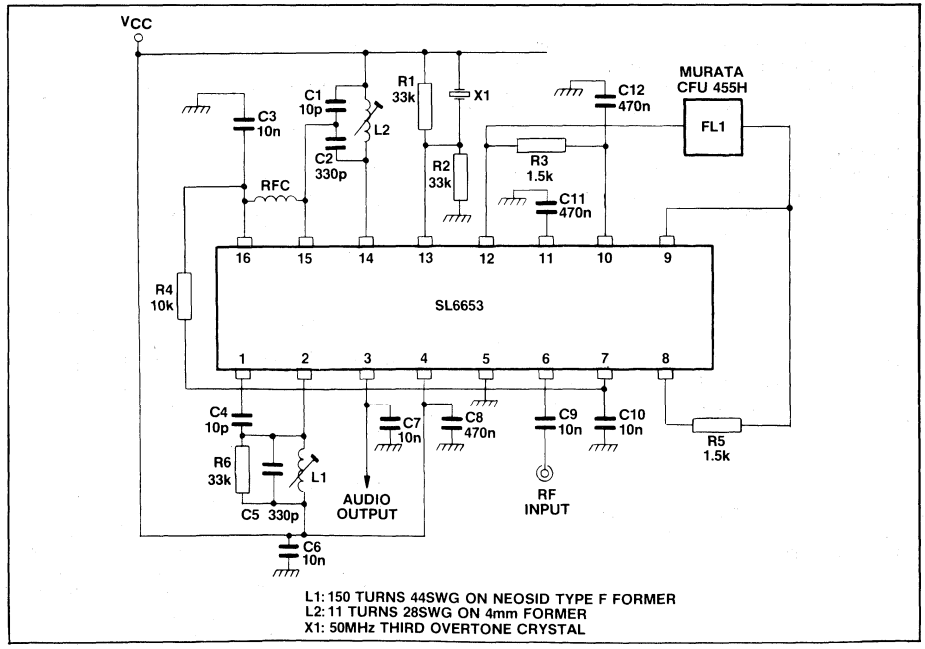

Fig.8 Circuit diagram of SL6653 demonstration board

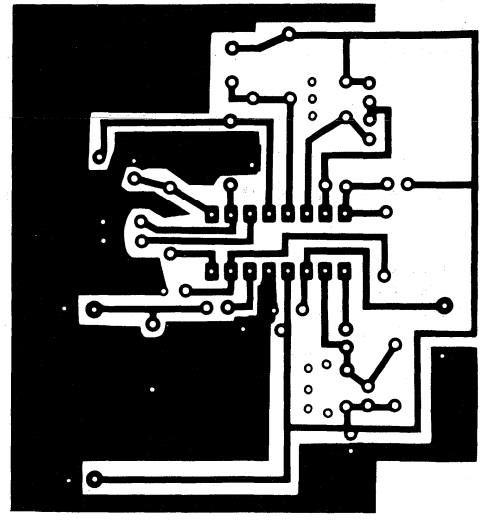

Fig.9 PCB mask of demonstration board (1:1)

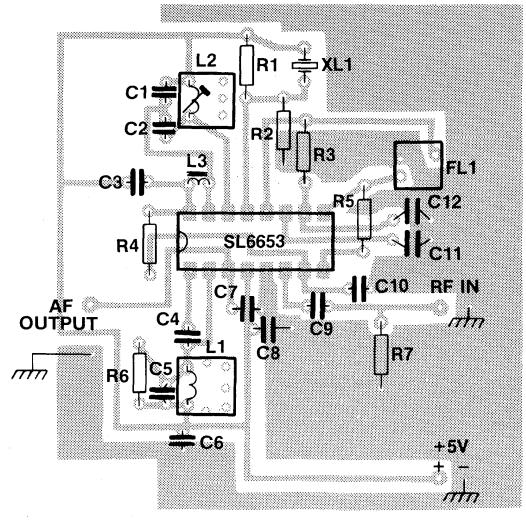

Fig.10 Component overlay of demonstration board (1:1)

PLESSEY
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SL6654

LOWER POWER IF (AF CIRCUIT (WITH RSSI) FOR FM CELLULAR RADIO

The SL6654 is a complete single chip mixer/oscillator, IF amplifier and detector for FM cellular radio, cordless telephones and low power radio applications. It features an exceptionally stable RSSI (Received Signal Strength Indicator) output using a unique system of detection. Supply current is less than 2mA from a supply voltage in the range 2.5V to 7.5V.

FEATURES

- Low Power Consumption (1.5mA)
- Single Chip Solution
- Guaranteed 100MHz Operation
- Exceptionally Stable RSSI

APPLICATIONS

- Cellular Radio Telephones
- Cordless Telephones

QUICK REFERENCE DATA

- Supply Voltage 2.5V to 7.5V
- Sensitivity 3μV
- Co-Channel Rejection 7dB

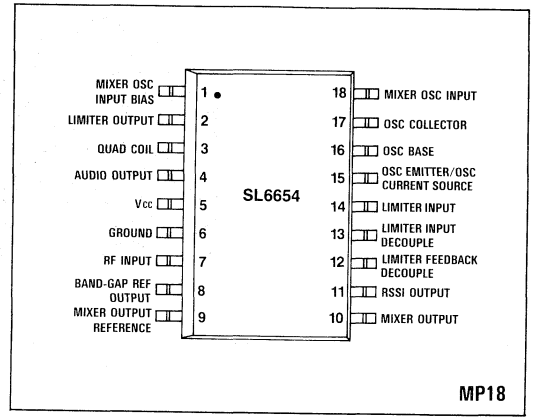

Fig.1 Pin connections (top view)

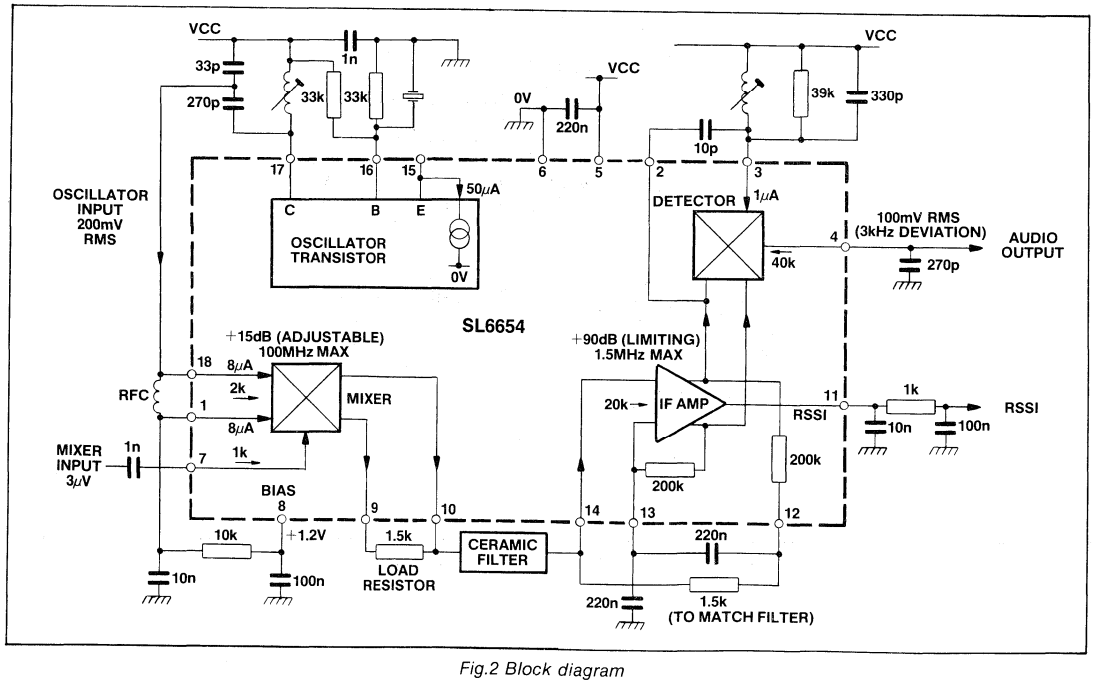

Fig.2 Block diagram

ABSOLUTE MAXIMUM RATINGS

Supply voltage	8V
Storage temperature	-55° C to +150° C
Operating temperature	-55° C to +125° C
Mixer input	1V rms

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

V_{CC} = 2.5V to 7.5V, T_{amb} = -30° C to +85° C, IF = 455kHz, RF = 50MHz, Quad Coil Working Q = 30

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Overall					
Supply current		1.5	2.0	mA	
Sensitivity		5	10	μV	20dB SINAD
		3		μV	12dB SINAD
AM rejection		40		dB	RF input $<500\mu$V
V_{bias}	1.0	1.2	1.4	V	T_{amb} = 25° C
Co-channel rejection		7		dB	See Note 2
Mixer					
RF input impedance		1		kohm	
OSC input impedance		2		kohm	
OSC input bias		5		μA	At V_{bias}
Mixer gain		15		dB	Rload = 1.5k
3rd order input intercept		-10		dBm	
OSC input level	180		300	mV	
OSC frequency	100			MHz	
Oscillator					
Current sink	40		70	μA	T_{amb} = 25° C
H_{fe}	30				40 ... 70μA
f_T		500		MHz	40 ... 70μA
IF Amplifier					
Gain		90		dB	
Frequency	455	1500		kHz	
Diff. input impedance		20		kohm	
Detector					
Audio output level	75		125	mV	5mV into pin 14
Ultimate S/N ratio		60		dB	
THD		0.5	5	%	
Output impedance		40		kohm	
RSSI Output(T_{amb} = +25° C)					
Output current			25	μA	No input pin 14
Output current	50		80	μA	Pin 14 = 2.5mV
Current change	0.9	1.22	1.5	μA/dB	See Note 1
Linear dynamic range	70			dB	See Note 1

NOTES

1. The RSSI output is 100% dynamically tested at 5V and +20° C over a 70dB range. First the input to pin 14 is set to 2.5mV and the RSSI current recorded. Then for each step of 10dB from -40 to +30dB the current is measured again. The current change in each step must meet the specified figure for current change. The RSSI output is guaranteed monotonic and free from discontinuities over this range.

2. Co-channel rejection is measured by applying a 3kHz deviation, 1kHz modulated signal at an input level to give a 20dB SINAD ratio. Then a 3kHz deviation, 400Hz modulated signal on the same frequency is also applied and its level increased to degrade the SINAD to 14dB.

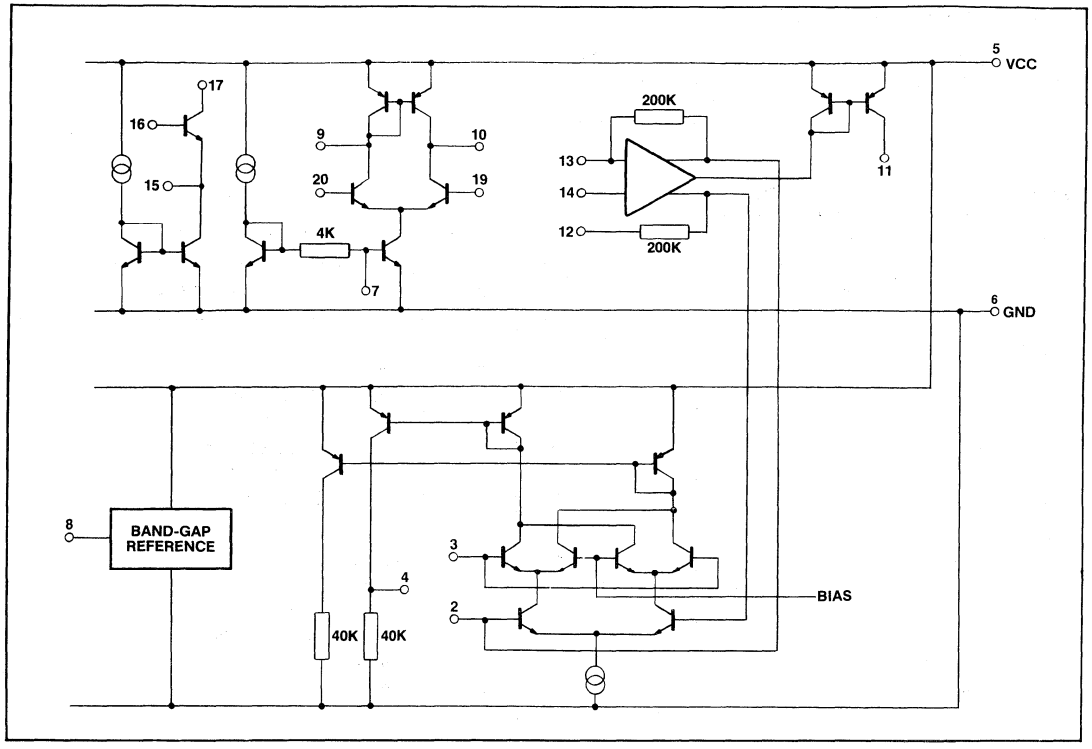

Fig.3 Internal schematic

GENERAL DESCRIPTION

The SL6654 is a very low power, high performance integrated circuit intended for IF amplification and demodulation in FM radio receivers. It comprises:

- A mixer stage for use up to 100MHz
- An uncommitted transistor for use as an oscillator
- A current sink for biasing this transistor
- A limiting amplifier operating up to 1.5MHz
- A quadrature detector with AF output
- An RSSI (Received Signal Strength Indicator) output

Mixer

The mixer is single balanced with an active load. Gain is set externally by the load resistor although the value is normally determined by that required for matching into the ceramic filter. It is possible to use a tuned circuit but an increase in mixer gain will result in a corresponding reduction of the mixer input intercept point.

The RF input is a diode-biased transistor with a bias current of typically 300μA. The oscillator input is differential but would normally be driven single-ended. Special care should be taken to avoid accidental overload of the oscillator input.

Oscillator

The oscillator consists of an uncommitted transistor with a current sink. The user should ensure that the design of oscillator is suitable for the type of crystal and frequency required; it may not always be adequate to duplicate the design shown in this data sheet.

IF amplifier

The limiting amplifier is capable of operation to at least 1MHz and the input impedance is set by an external resistor to match the ceramic filter. Because of the high gain, pins 12 and 13 must be adequately bypassed.

Detector

A conventional quadrature detector providing audio output is fed internally from the IF amplifier; the quadrature input is fed externally using an appropriate capacitor and phase shift network.

RSSI output

The RSSI output is a current source with value proportional to the logarithm of the IF input signal amplitude. There is a small residual current due to noise within the amplifier (and mixer) but beyond this point there is a measured and guaranteed 70dB dynamic range. The typical range extends to 92dB, independent of frequency, and with exceptionally good temperature and supply voltage stability.

Supply voltage

The SL6654 will operate reliably from 2.5V to 7.5V. The supply line must be decoupled with 470nF using short leads.

Internal bias voltage

The internal band gap reference must be externally decoupled. It can be used as an external reference but must not be loaded heavily; the output impedance is typically 14 ohms.

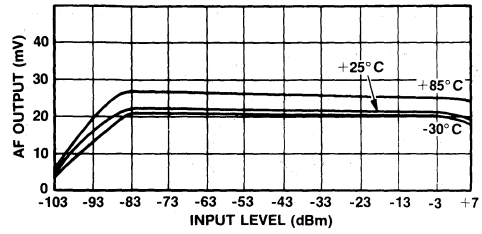

Fig.4 Audio output vs input and temperature at 2.5V

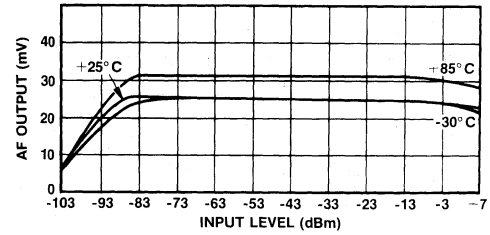

Fig.5 Audio output vs input and temperature at 5.0V

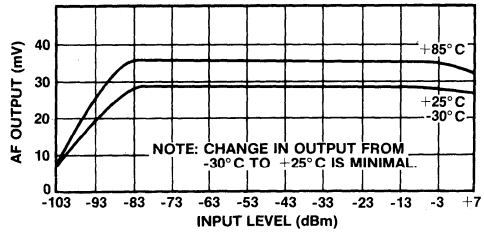

Fig.6 Audio output vs input and temperature at +7.5V

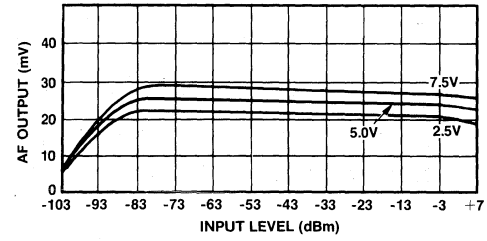

Fig.7 Audio output vs input and supply voltage at +25°C

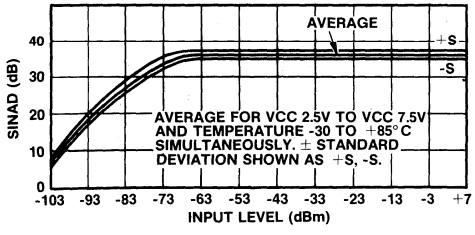

Fig.8 SINAD and input level

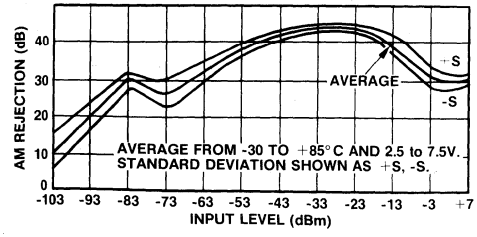

Fig.9 AM rejection and input level

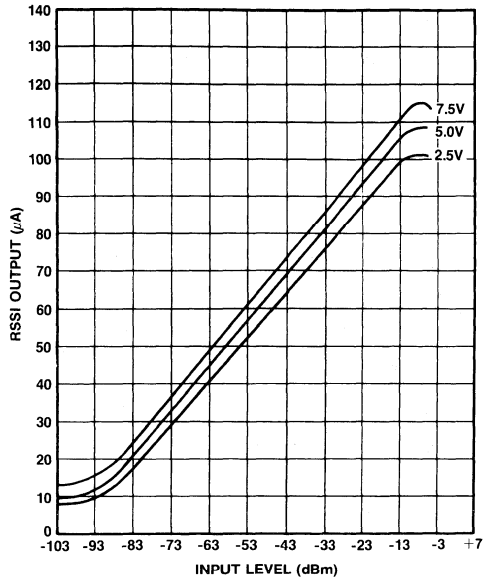

Fig.10 RSSI output vs input and supply voltage (T_{amb} = 20° C)

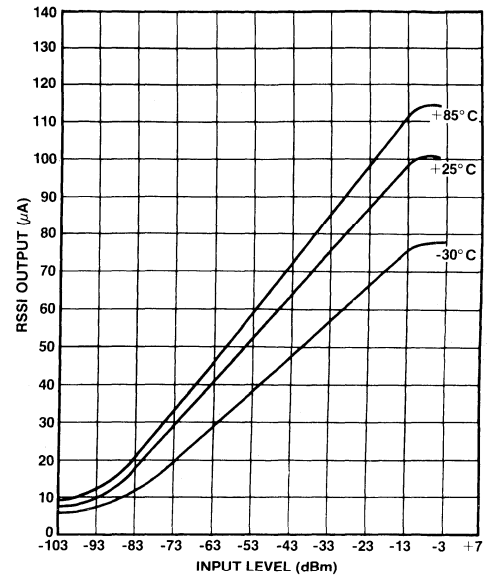

Fig.11 RSSI output vs input level and temperature (V_{CC} = 2.5V)

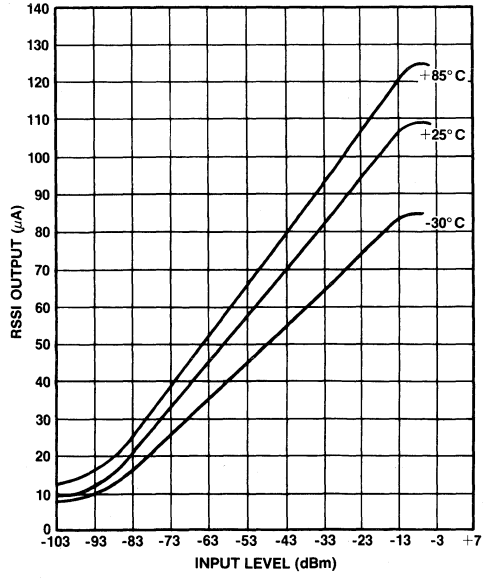

Fig.12 RSSI output vs input level and temperature (V_{CC} = 5V)

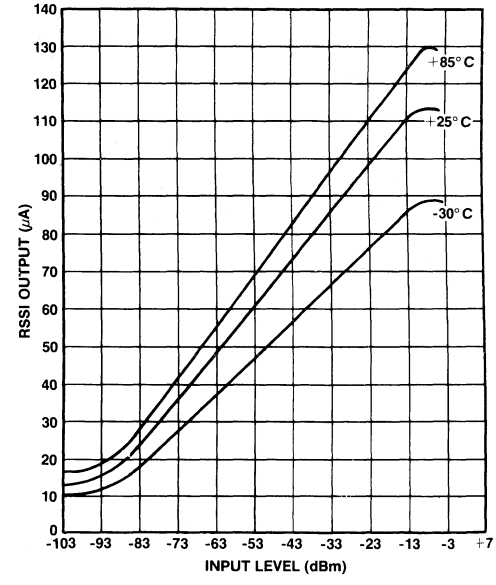

Fig.13 RSSI output vs input level and temperature (V_{CC} = 7.5V)

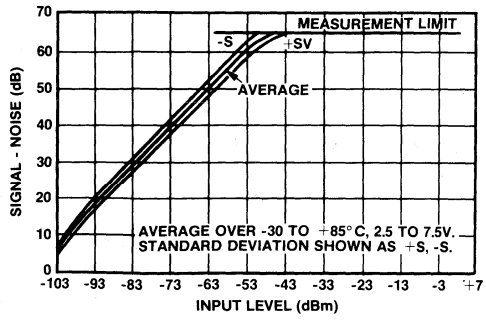

Fig.14 Signal + noise to noise ratio vs input level

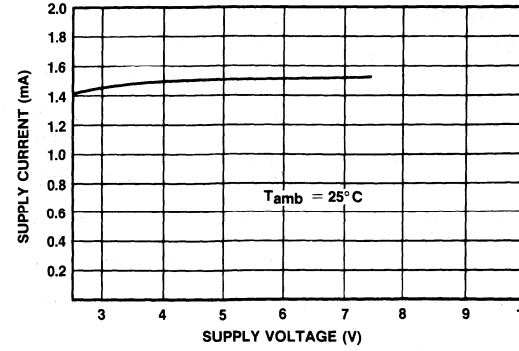

Fig.15 Supply current vs supply voltage

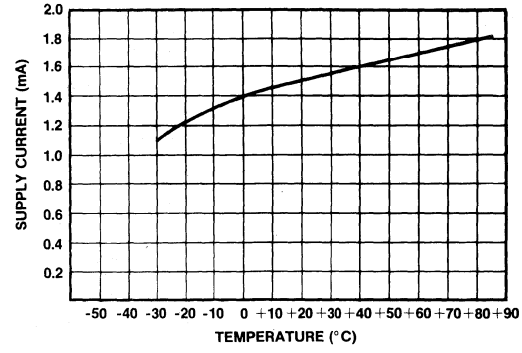

Fig.16 Supply current vs temperature (V_{CC} = 5V)

PLESSEY
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SL6655

ULTRA LOW POWER FM RADIO RECEIVER

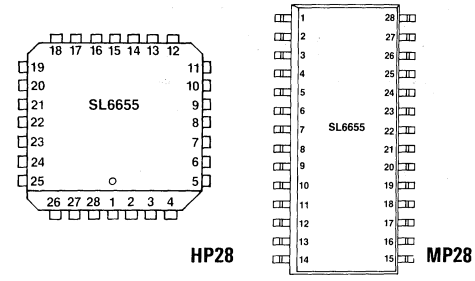
The SL6655 is a single conversion receiver complete with RF amp/mixer/oscillator/IF amplifier and detector. It features very low current consumption and operation from 0.9V to 8V supply. The device can be powered down to currents of 1μA and offers sensitivities of typically 250nV.

FEATURES

- Very Low Voltage Operation (0.9V)
- Very Low Current Consumption:
  - 1mA Powered Up (typ.)
  - 1μA Powered Down (typ.)
- Wide Supply Range 0.9V to 8V
- 250nV Sensitivity (12dB Sinad)
- Guaranteed 100MHz Operation
- Small Outline Package

APPLICATIONS

- Low Power Radio Receivers
- Radio Paging
- Cordless Telephones



Pin	Function	Pin	Function
1	N/C	15	RF Vcc +
2	Mixer output	16	LF Vcc +
3	Battery economy	17	Audio output
4	Oscillator current source & emitter	18	Audio output(Differential)
5	Oscillator base	19	Quad coil drive
6	Oscillator collector	20	Quad coil
7	Mixer osc input	21	N/C
8	Mixer osc I/P bias	22	2nd limiter F/B decouple
9	Mixer RF input	23	2nd limiter input
10	RF amp output	24	2nd limiter I/P decouple
11	Regulator output	25	1st limiter output
12	RF amp input	26	1st limiter I/P decouple
13	RF ground	27	1st limiter input
14	LF ground	28	1st limiter F/B decouple

Fig.1 Pin connections - top view

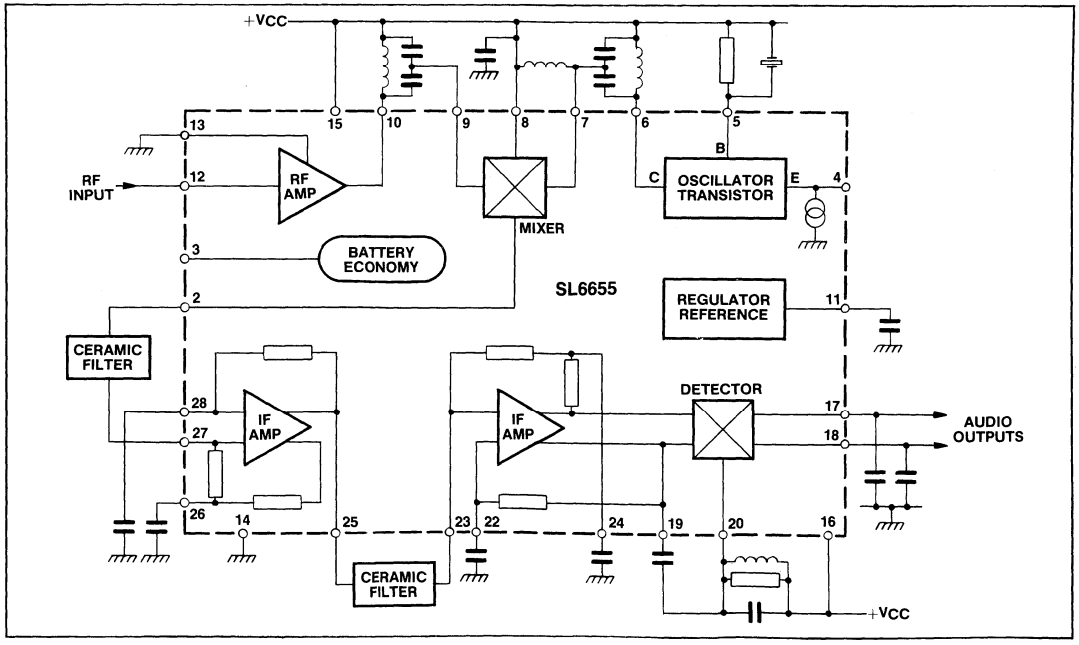


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0° C to +50° C, V_{CC} = 1.3V

Characteristic	Pin Number	Value			Units	Conditions
		Min.	Typ.	Max.		
Overall						
Supply voltage		0.9		8	V	25° C
Supply voltage		1.0		8	V	-30° C to +85° C
Supply current						
Powered up			1.0	1.3	mA	Pin 3 High
Powered down			1.0		μA	Pin 3 Low
Battery economy response			0.5		ms	
Sensitivity			250		nV	12dB Sinad
AM rejection			37		dB	
RF amplifier						
Supply current			50		μA	
Noise figure			6		dB	
H_{FE}			100			
f_T			500		MHz	
Oscillator						
Supply current			50		μA	
H_{FE}			100			
f_T			500		MHz	
IF amplifier cascade						
Sensitivity	27		3		μV	12dB Sinad
Input impedance	27, 23		1.5		kΩ	
Output impedance	25		1.5		kΩ	
Gain			100		dB	
Upper cut-off frequency			1.5		MHz	
Detector						
Audio output level			7		mV(rms)	
Inter-output isolation			65		dB	
Output impedance			50		kΩ	
Mixer						
Conversion gain			6		dB	
Input impedance			4		kΩ	
Output impedance			1.5		kΩ	
Regulator						
Output level		0.9	0.95	1	V	
Output temperature coefficient			1.3		mV/° C	
Output current		6			mA	
Battery economy						
Input current			0.5		μA	
Input logic high		80			% V_{CC}	
Input logic low				20	% V_{CC}	

GENERAL DESCRIPTION

The RF amplifier is a diode biased input with a bias current of typically 50μA. The output is left open circuit so that the gain can be selected externally.

The RF input to the Mixer is diode biased with a bias current of typically 250μA. The oscillator input is differential, but would normally be driven single ended with the remaining input biased at V_{CC}.

The Mixer has a single output with resistance of 1.5kΩ. A single transistor is used for the oscillator which has its base and collector floating, and the emitter connected to a current source of 50μA nominal value.

The IF amplifiers have input impedances of 1.5kΩ and are thus ideally suited for use with 455kHz ceramic filters.

The detector is fed internally from the IF limiting amplifier and the quadrature input is fed externally using a capacitor and appropriate phase shift networks. A differential audio output is provided to feed a comparator for digital use. The regulated output is a supply independent and partially temperature compensated capable of sourcing 6mA.

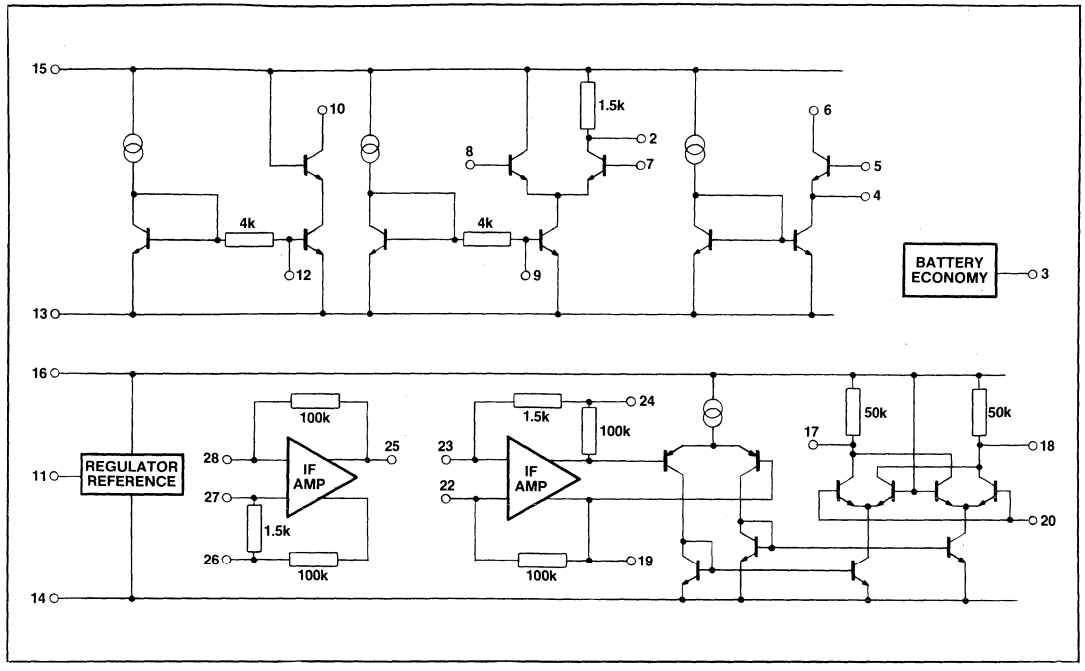


Fig.3 SL6655 internal schematic

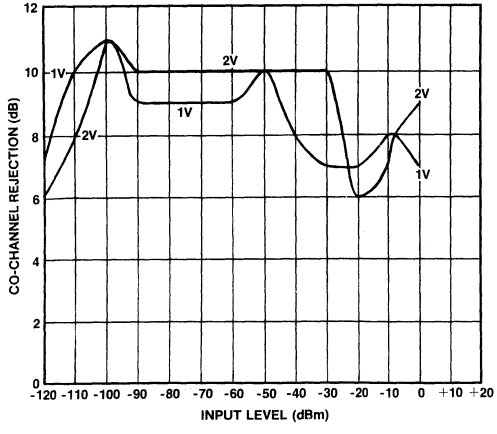


Fig.4 Input level vs co-channel rejection for V_{CC} = 1 & 2V at 25° C (unweighted measurements)

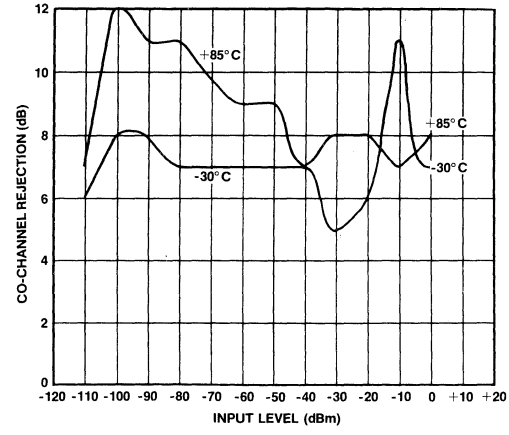


Fig.5 Co-channel rejection vs input level over temperature at V_{CC} = 1V (unweighted measurements)

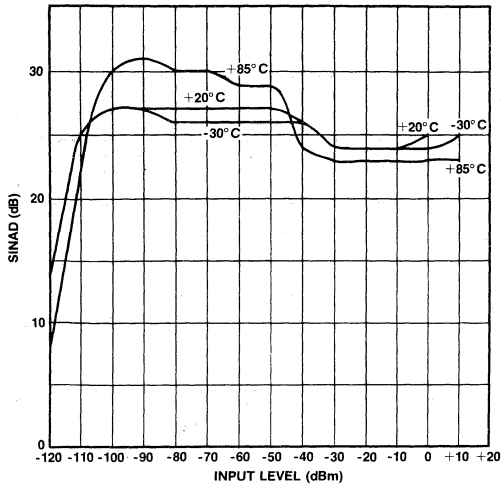


Fig.6 Sinad vs input level over temperature at Vcc = 1V (unweighted measurements)

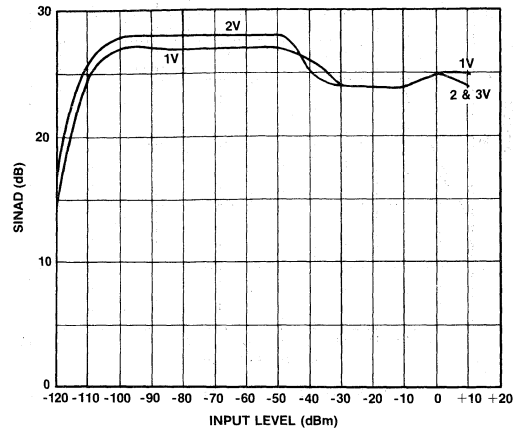


Fig.7 Sinad vs input level at Vcc = 1, 2 & 3V (unweighted measurements)

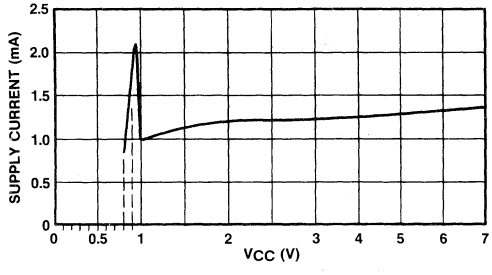


Fig.8 Supply current vs Vcc

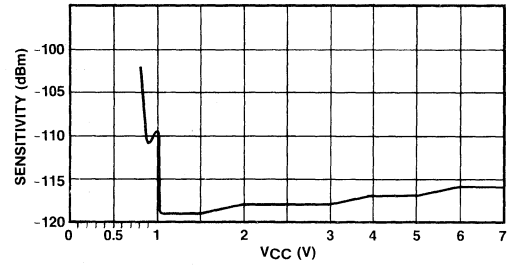


Fig.9 Sensitivity (dBm for 12dB sinad) vs Vcc

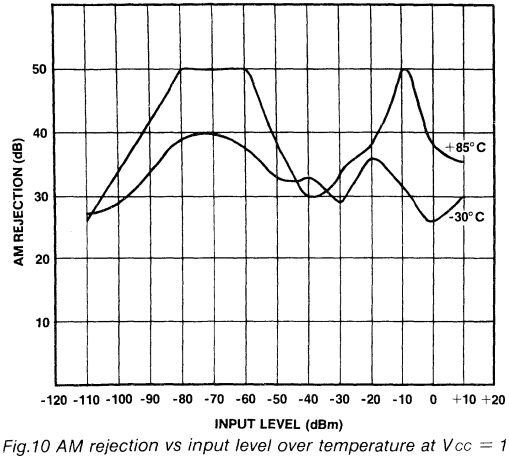


Fig.10 AM rejection vs input level over temperature at Vcc = 1V (unweighted measurements)

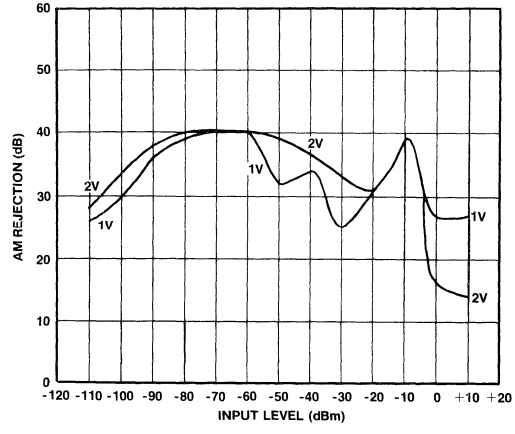


Fig.11 AM rejection vs input level at 20° C (unweighted measurements)

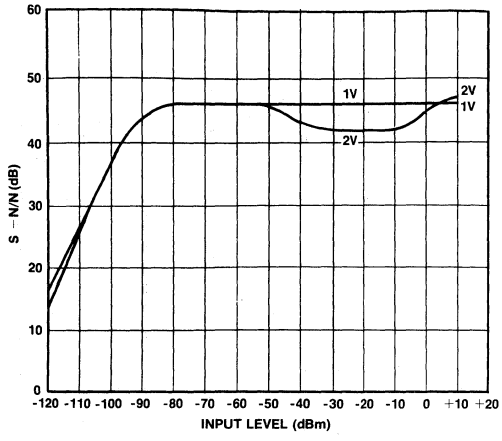


Fig.12 S + N/N vs input level (unweighted measurements)

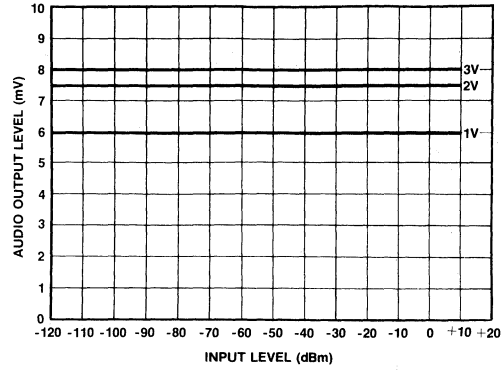


Fig.13 Audio output level vs input level (unweighted measurements)

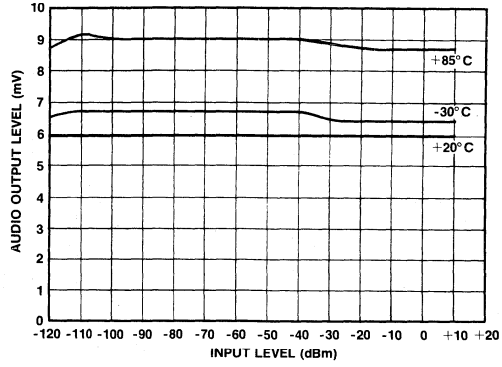


Fig.14 Audio output level vs input level over temperature at V_{CC} = 1V (unweighted measurements)

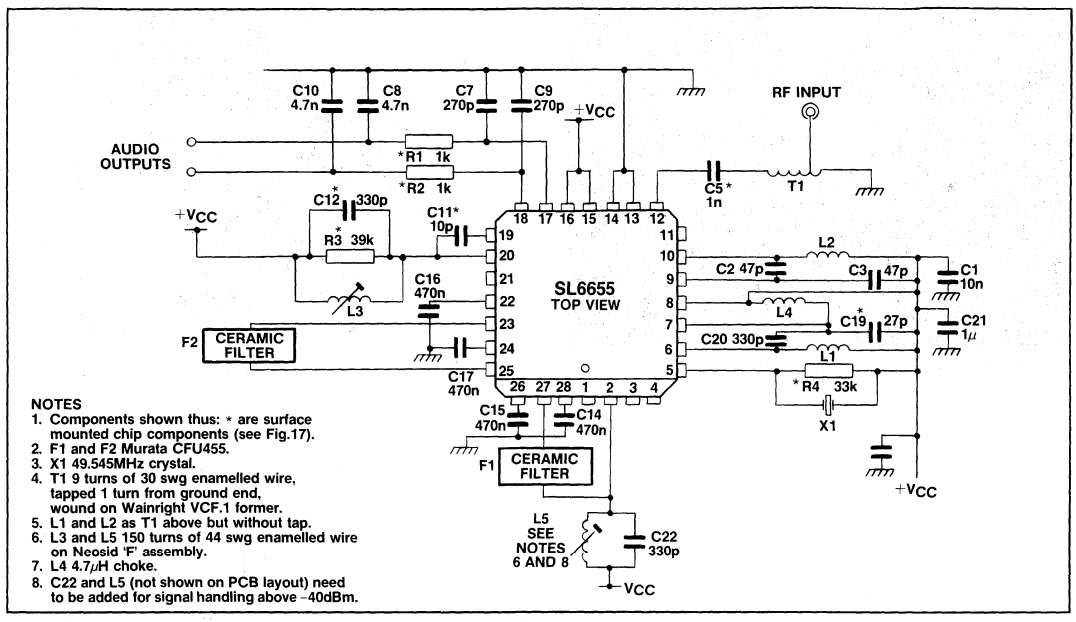


Fig.15 Circuit diagram of SL6655 demonstration board

PERFORMANCE OF SL6655 DEMONSTRATION BOARD

Input signal = 50MHz, Frequency modulated with 1kHz with ± 3kHz deviation, T_{amb} = 0° C to +50° C, V_{CC} = 1.3V

Sensitivity	-119dBm for 12dB sinad at 1.3V -113dBm for 12dB sinad at 0.9V
Adjacent channel rejection	50dB at 1.3V 68dB at 0.9V
Co-channel rejection	10dB at 1.3V 9dB at 0.9V
RF amplifier 2nd order intercept **RF amplifier 3rd order intercept**	0dB -14dBm
Noise figure of RF amplifier	6dB

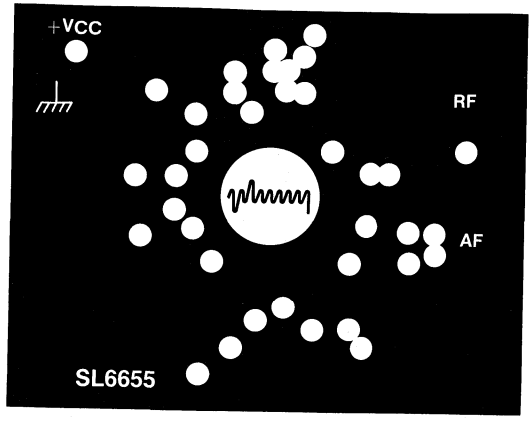


Fig.16 Ground plane of demonstration board (1:1)

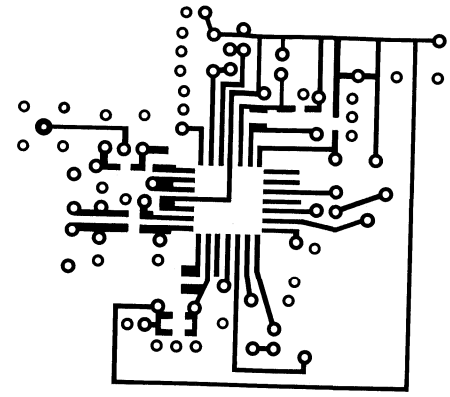


Fig.17 Track side of demonstration board (1:1)

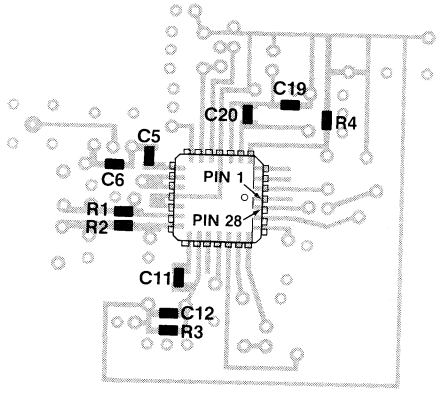


Fig.18 Surface mounted component overlay (track side) of demonstration board (1:1)

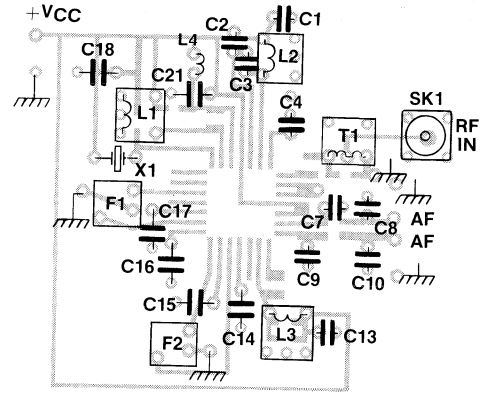


Fig.19 Component overlay (ground plane side) of demonstration board (1:1)

NOTE
A PCB layout for the SL6655 in miniature plastic DIL package (MP28) is given in the Application Note on p.268.

PLESSEY
Semiconductors

SL6670

0.9V DC/DC VOLTAGE CONVERTER

The SL6670 is a novel Bipolar monolithic voltage multiplier designed to operate from supply voltages as low as 0.9V.

Voltage tripling uses a capacitor pump technique and no external coil is required.

Full load regulation is provided and the output can be pre-set to the desired voltage.

A programmable oscillator allows for optimisation of efficiency for any particular load. This can be switched into a very high efficiency 'standby' mode when very small load currents are required. The device also comes equipped with a battery flag monitor.

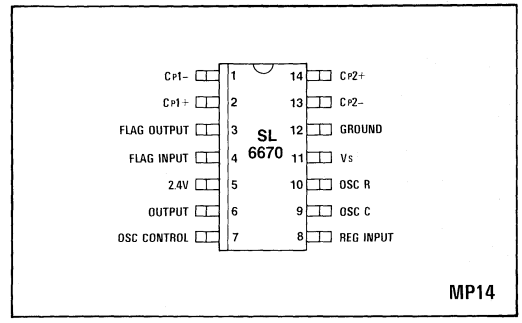


Fig.1 Pin connections - top view

FEATURES

- High Power Efficiency
- 0.9V to 8V Operation
- No Inductors Required
- Low Radiation
- Miniature Plastic Package

APPLICATIONS

- Radio Pager Power Supplies
- Memory Back-Up Supplies
- High Efficiency Battery Powered DC/DC Converters

ORDERING INFORMATION

SL6670 NA MP

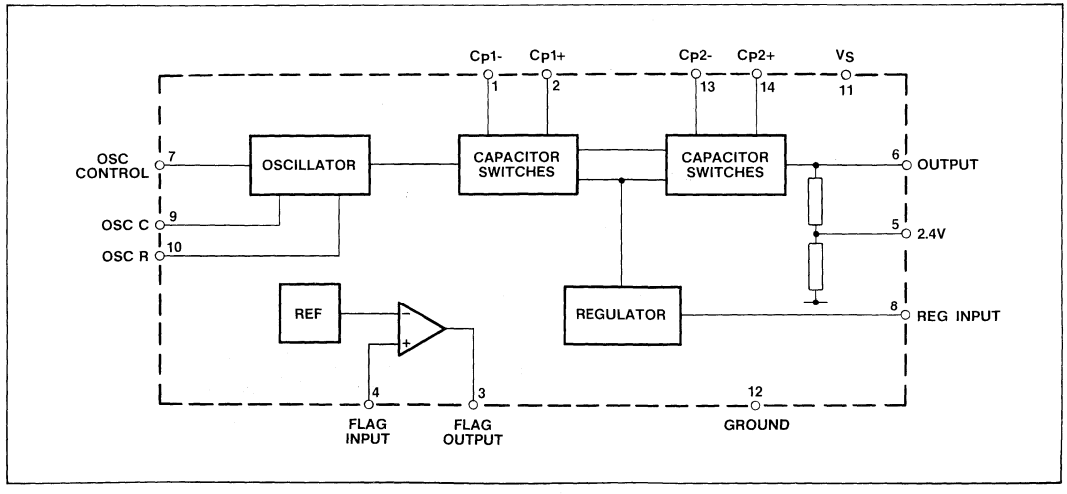


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = −30°C to +85°C, V_S = 1.05V to 8V Oscillator control high.

Characteristics	Pin No.	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage V_S	11	0.9		8	V	T_{amb} = 25°C
Supply current I_S	11		180	250	μA	I_O = 0
Output current I_O	6	1.5			mA	V_S = 2.5V, V_O = 4.5V, T_{amb} = 25°C
		1			mA	V_S = 1V, V_O = 2V, T_{amb} = 25°C
Output voltage V_O	6	0.9		8	V	
Operating frequency range f_O	9,10			50	kHz	
Output source impedance Z_O	6		67		Ω	V_S = 1.5V, V_O = 2.4V, I_O = 1mA
Power conversion efficiency (See Note 1)			85		%	I_L = 0.1mA f_O = 1kHz V_O = 3.5V, V_S = 1.3V
Voltage tripling conversion efficiency (See Note 2)			99		%	I_L = 0, f_O = 1kHz V_S = 1.05V to 3V
Oscillator control bias current	7			2	μA	V_{IN} = 0V to V_S
Oscillator control high voltage	7	70			% V_S	
Oscillator control low voltage	7			30	% V_S	
Flag input impedance	4	1.5			MΩ	
Flag output high voltage	3	70			% V_S	Sourcing 10μA
Flag output low voltage	3			30	% V_S	Sinking 1μA
Flag threshold voltage			0.7		V	
Regulator input reference voltage	8		0.7		V	
Regulator input bias current	8			0.5	μA	
Fixed output voltage option		2.25	2.4	2.55	V	T_{amb} = 25°C, I_O = 0

NOTES

1. Power conversion efficiency = $\frac{\text{Load current x Output voltage}}{\text{[Input current - Standby current] x Input voltage}}$ x 100%

2. Voltage conversion efficiency = $\frac{\text{Output voltage}}{\text{[3 x Input voltage]}}$ x 100%

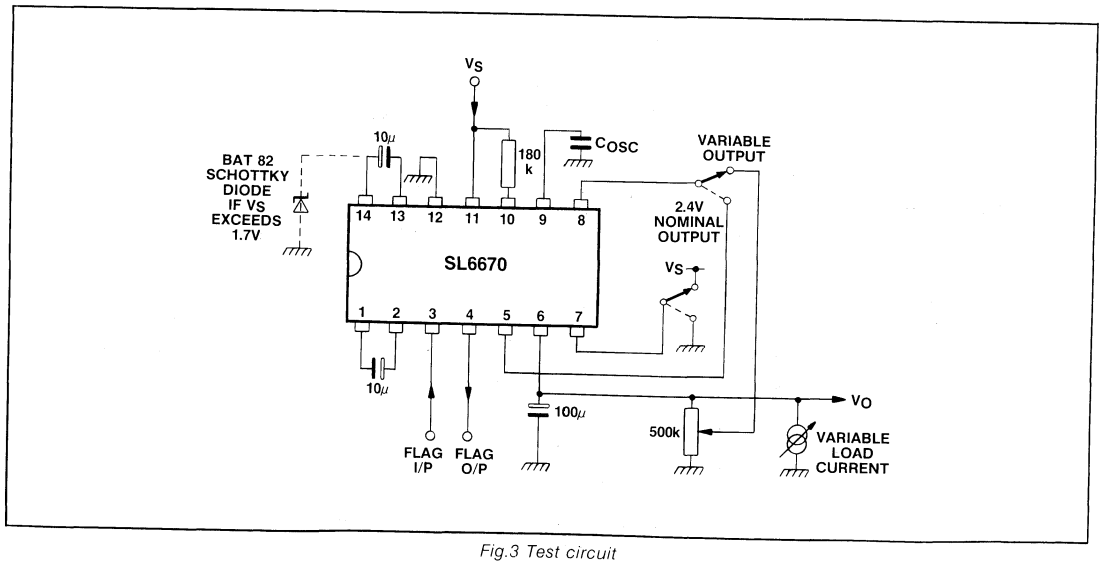


Fig.3 Test circuit

PIN DESIGNATIONS

Pin	Function
1	Capacitor between this pin and pin 2 to store pumping current.
2	Capacitor between this pin and pin 1 to store pumping current.
3	**Flag output.** This output is low when pin 4 is lower than the flag reference.
4	**Flag input.** Pin 3 output will be low when this pin is below the flag reference.
5	**2.4V nominal.** Tying this pin to pin 8, Regulator input, will set the output to nominally 2.4V.
6	**Output.** This pin drives the Tank capacitor and can be adjusted to any voltage between 0.9V and 8V.
7	**Oscillator control pin.** When this pin is taken high the oscillator runs at a frequency determined by external components on pins 9 and 10. When taken low the oscillator will run at 6% of this frequency.
8	**Regulator input.** The output voltage pin 6 is set by an external resistive divider connected from pin 6 to pin 8 and ground. The regulator will keep this pin at 0.7V. Tying this pin to pin 5 will regulate the output to 2.4V.
9	**Oscillator capacitor.** A capacitor is connected from this pin to ground and determines the oscillator frequency.
10	**Oscillator resistor.** A 180kΩ resistor connected from this pin to pin 11 is required.
11	**Battery voltage.** From 0.9V to 8V.
12	**Ground.**
13	Capacitor between this pin and pin 14 to store pumping current.
14	Capacitor between this pin and pin 13 to store pumping current. A Schottky diode is required on this pin if Vs is greater than 1.7V.

PRINCIPLE OF OPERATION

Because of the low input voltage the SL6670 uses a two stage pump circuit, using external pump capacitors, which will provide up to three times the input voltage at the output tank capacitor. A regulator is provided to enable the output to be set at any voltage below this tripled output.

The operation of the device can best be described by considering Fig.4, which shows an idealised voltage tripler. Switches S1 are closed for half the clock cycle with switches S2 open. The next half clock cycle, switches S2 are closed and switches S1 open. With switches S1 closed the capacitors charge up, towards Vs. When switches S2 close the charged capacitor are stacked one above the other on to Vs, giving a maximum output of 3Vs.

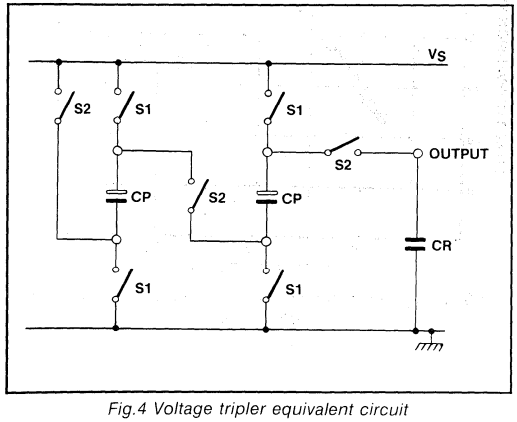


Fig.4 Voltage tripler equivalent circuit

GENERAL DESCRIPTION

Regulator

The regulator uses a charge control method to charge the pump capacitors sufficiently to keep the reservoir capacitor at a defined voltage regardless of load, thus achieving current and voltage regulation. The regulated output voltage is selected by providing a feedback voltage to the regulator input pin using an external resistive divider. Alternatively, a preset 2.4V nominal output pin is provided to minimise external components.

Oscillator

The clock is provided by the on-chip oscillator, the frequency of which can be selected by choosing appropriate R and C values. The control pin will, when taken low, reduce the oscillator frequency to approximately 6% of its nominal value. This is useful where the load is variable, e.g. radio pagers with battery economy. Linking the oscillator control input to the battery economy signal will optimise the converter efficiency for the different load requirement.

Flag Circuit

A flag circuit is included which can be used to signal that the output has dropped below a preset level. Hysteresis can be provided with a feedback resistor. The flag circuit can also be used to check the battery supply if desired. Another use of the flag circuit is to lower the oscillator frequency when either the battery voltage or output drops below a preset limit.

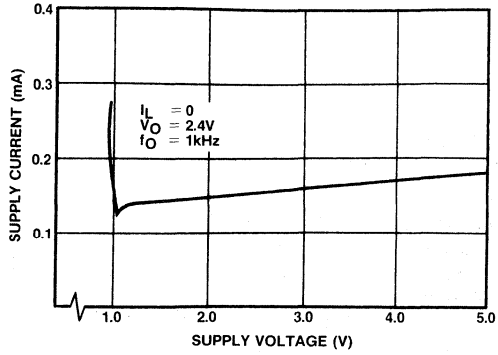


Fig.5 Supply current as a function of supply voltage

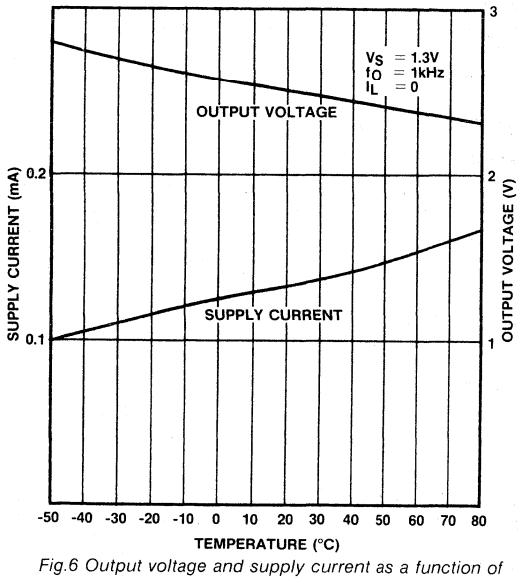


Fig.6 Output voltage and supply current as a function of temperature

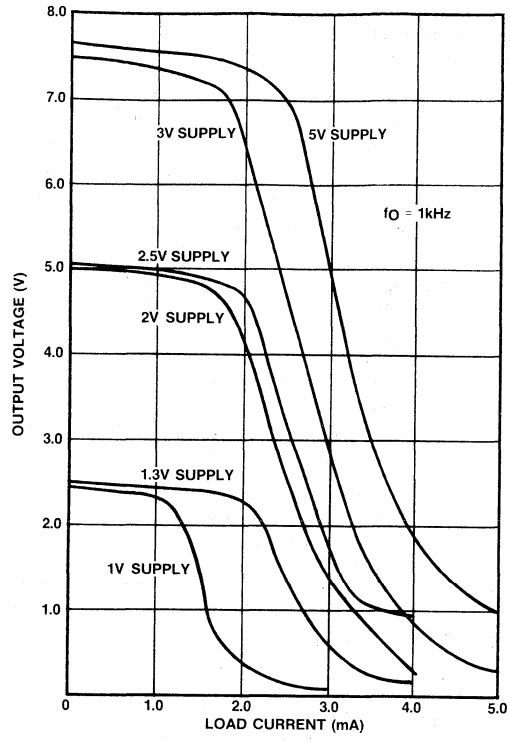


Fig.7 Output voltage as a function of load current

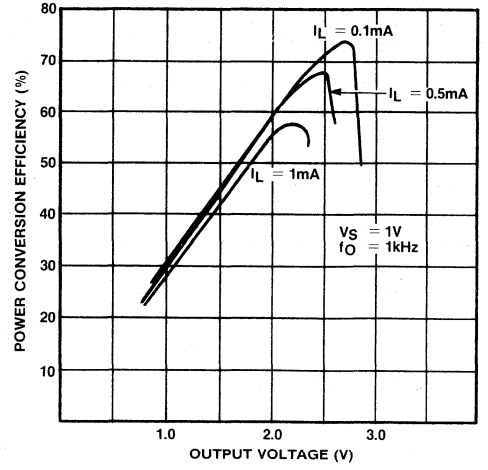


Fig.8 Power conversion efficiency as a function of regulated output voltage

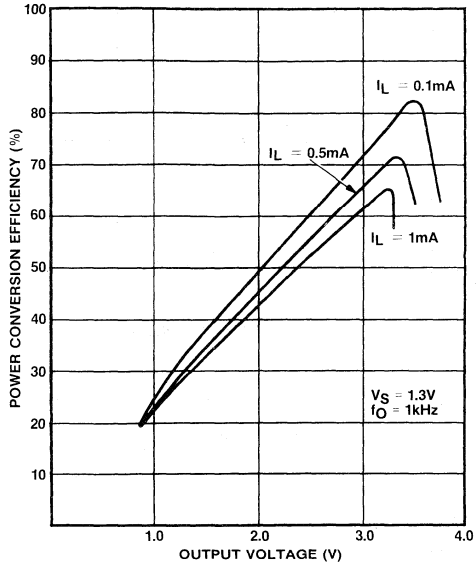


Fig.9 Power conversion efficiency as a function of regulated output voltage

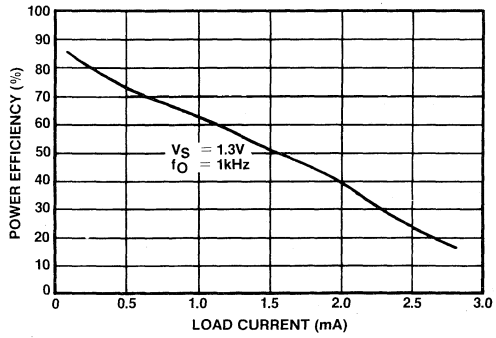


Fig.10 Optimised power conversion efficiency as a function of load current

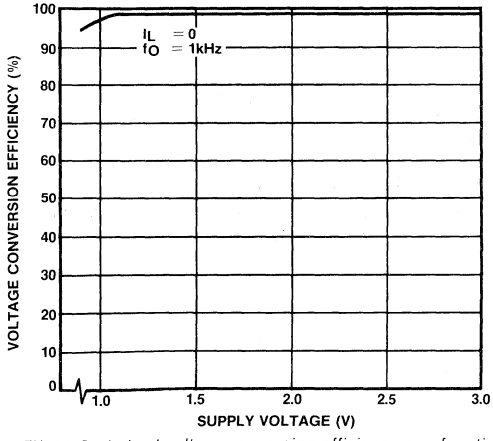


Fig.11 Optimised voltage conversion efficiency as a function of supply voltage

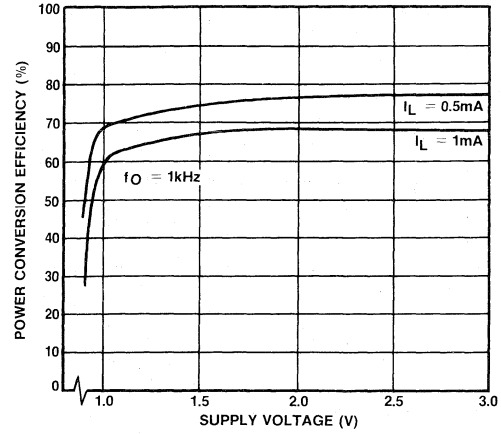


Fig.12 Optimised power conversion efficiency as a function of supply voltage

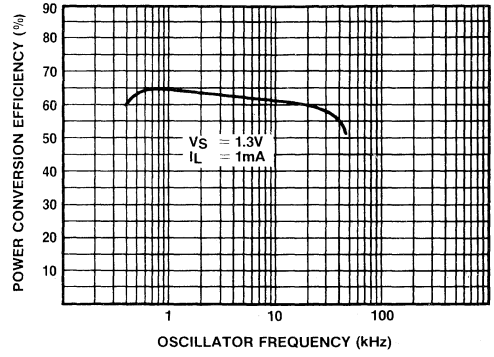


Fig.13 Power conversion efficiency as a function of oscillator frequency

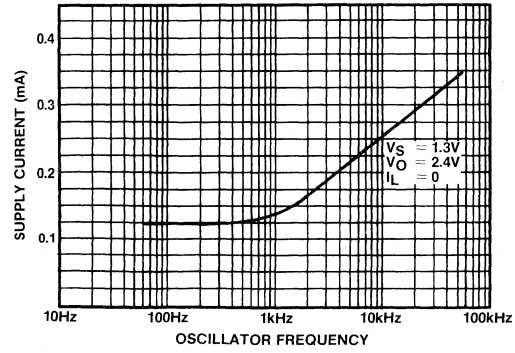


Fig.14 Supply current as a function of oscillator frequency

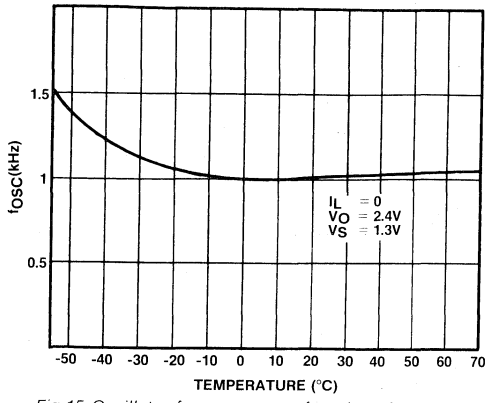


Fig.15 Oscillator frequency as a function of temperature

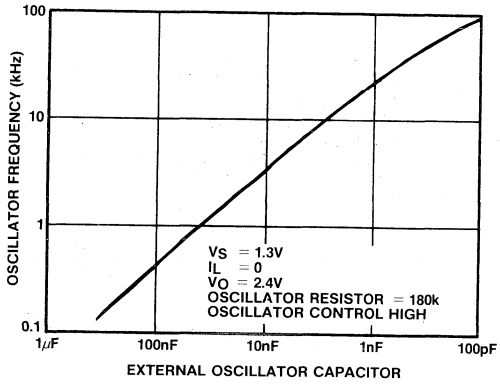


Fig.16 Oscillator frequency as a function of external oscillator capacitor

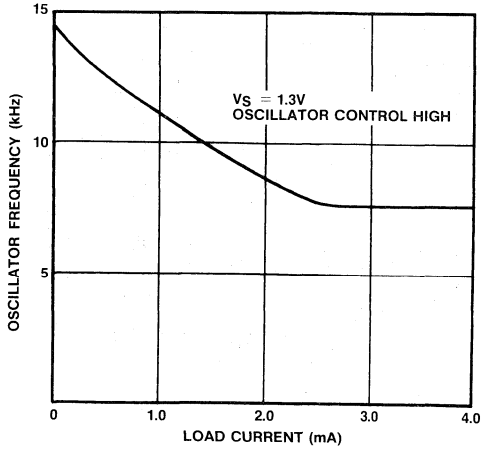


Fig.17 Variation of oscillator frequency with load current

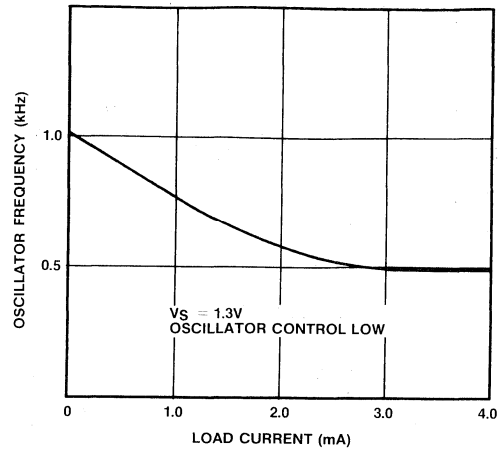


Fig.18 Variation of oscillator frequency with load current

EXTERNAL COMPONENTS

Oscillator Resistor and Capacitor

The resistor value determines the amount of hysteresis in the oscillator and should be 180kΩ for correct operation. The capacitor value, which will depend on the frequency of operation required, can be calculated as follows:

$$C_{OSC} \approx \frac{26}{f}$$

when oscillator control pin is high.
Where C is in μF and f is in Hz, or obtained from the appropriate graph.

Pump Capacitors

The pump capacitors C_P store the pumping charge before it is transferred to the tank capacitor. For the regulator to maintain optimum efficiency the pump capacitors must be equal in value. The pump capacitor value is chosen to ensure the droop voltage ΔV_P is acceptable.

$$\Delta V_P = \frac{I_{LOAD}}{fC_P}$$

The magnitude of ΔV_P is chosen considering the worst case input-output voltage expected.

$$\Delta V_P < \frac{[3V_S - V_O]}{2}$$

where ΔV_P is droop voltage on each pump capacitor.
If this consideration is not met the output will fall out of regulation.

Reservoir Capacitors

The reservoir capacitor integrates the ripple at the output. To reduce the ripple ΔV_O the reservoir capacitor C_R must be of the correct value.

$$\Delta V_O = \frac{I_{LOAD}}{2C_R f}$$

where f is clock frequency in Hz.

Schottky Diode

A Schottky diode is required from pin 14 to ground if V_S exceeds 1.7V. This protects the chip should the output be short circuited. If the diode is not present the device will remain in a non-destructive latched state; removing the supply will ensure normal operation. The inclusion of the diode will not affect the device operation and no change in device specification is required; the diode only acts as a catching diode under fault conditions and carries no current under normal operation.

CONSIDERATIONS FOR HIGH EFFICIENCY

Frequency

The efficiency of the SL6670 is dependent on the oscillator frequency. As the oscillator frequency is increased the switching losses increase, so lowering the efficiency.

Pump Capacitors

The regulator controls the amount of charge transfer assuming that both pump capacitors have the same charge characteristic. Therefore, for optimum efficiency, the pump capacitors should be the same value. To obtain optimum efficiency the value of pump capacitors must be chosen so that the regulator is always in regulation.

Reservoir Capacitor

The reservoir capacitor must be chosen to reduce the output ripple. For optimum efficiency the regulator must see a signal at its inputs which has no large ripple component.

Regulator

The regulator will control the output voltage to any level between 0.9V and 8V, depending on the value of V_S. The control range in any application is set by V_S but the device will not necessarily be efficient at all settings of output voltage. When the output voltage is set close to V_S, there is a limit to the amount of charge that can be transferred from the pump capacitors to the reservoir capacitor, and so efficiency will fall. When the output is set close to $3V_S$, the charge transfer may be insufficient, due to internal device voltage drops, to achieve the required output. The regulator will attempt to drive the output higher than is possible, by driving large currents into the switches, even with no load current. This will reduce the efficiency near the upper limit of the regulator.

DESIGN EXAMPLE

2.4V Supply from Single Alkaline Cell for use in Radio Pager

A major use of the SL6670 will be providing a high voltage supply to enable CMOS circuits to operate from battery voltages down to 0.9V. The battery can vary from 1.7V when new to 0.9V when exhausted, so the maximum output voltage is 2.7V when the battery falls to 0.9V. A good choice of output voltage would be 2.4V because this enables the on-chip potential divider to be used.

The choice of frequency is dependent on the ripple requirement and capacitor sizes. In the case of direct conversion pagers, with large amounts of gain at low frequencies, a high oscillator frequency will ease the supply decoupling required. A frequency of about 18kHz is acceptable, which gives a value of oscillator capacitor of 1.5nF.

The maximum droop voltage that can be allowed is:

$$\frac{3V_S - V_O}{2} = 150mV$$

Using a load of 1mA and a 1μF capacitor for C_P:

$$\frac{I_{LOAD}}{fC_P} = 56mV \text{ droop voltage}$$

This is well below the 150mV and is an acceptable value.

Using a 100μF capacitor for the reservoir capacitor will give:

$$\frac{I_{LOAD}}{2C_Rf} = 0.3mV \text{ output ripple}$$

If the oscillator control is used to reduce the oscillator frequency when the pager is 'battery economised', the performance at this new load level must be checked. When 'battery economised', the pager load may fall from 1mA to, say, 50μA. The droop voltage will now be:

$$\frac{50\mu}{18kHz \times \frac{6}{100} \times 1\mu F} = 46mV \text{ - an acceptable value}$$

Output ripple will be:

$$\frac{50\mu A}{2 \times 100\mu F \times 18kHz \times \frac{6}{100}} = 0.23mV$$

Since the maximum supply voltage is 1.7V the extra Schottky diode on pin 14 will not be required.

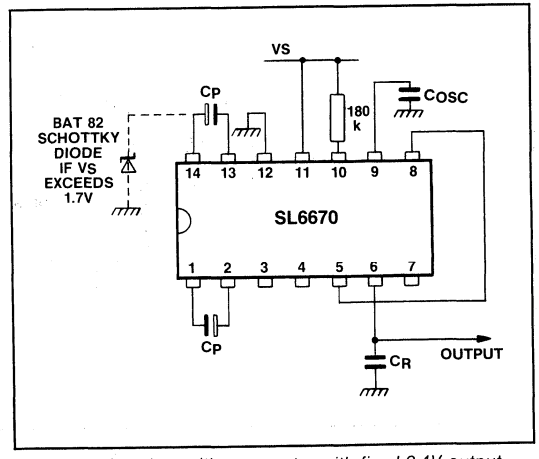


Fig.19 Simple positive converter with fixed 2.4V output

TYPICAL APPLICATIONS

Simple Positive Voltage Converter

A major application of the SL6670 is the conversion of a single cell battery to a higher voltage suitable for the supply of CMOS circuits. A typical application would be in radio pagers and Fig.19 shows a typical application. The use of 2.4V output will allow the use of the on-chip resistors and so reduce the external component count. The Schottky diode will be required if V_S exceeds 1.7V.

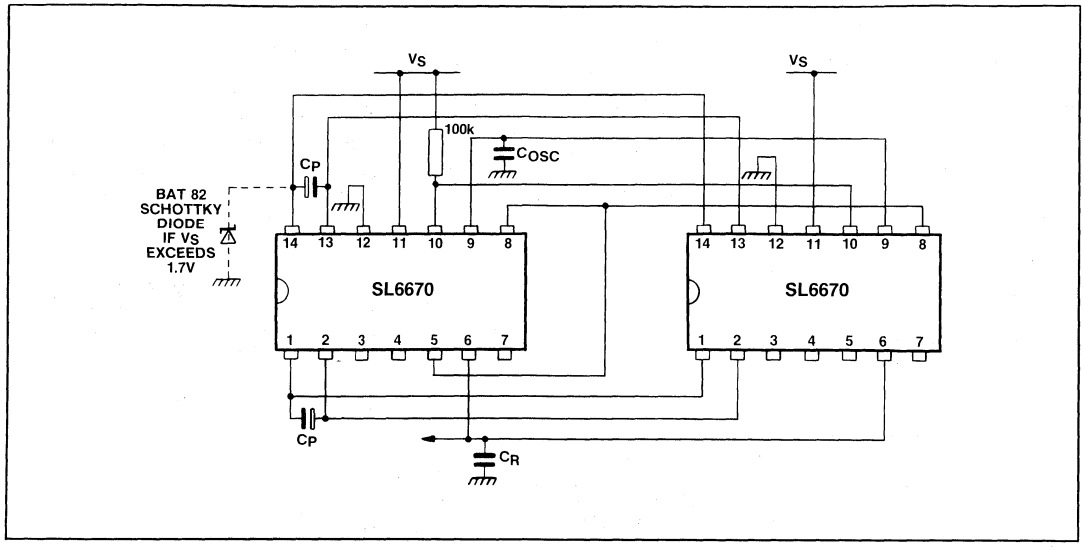


Fig.20 Paralleling devices with fixed 2.4V output

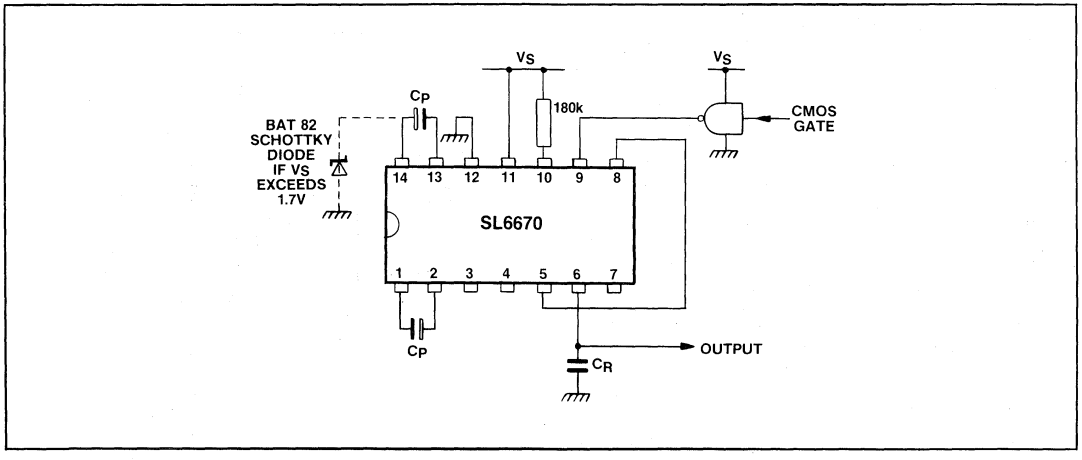


Fig.21 External clocking of SL6670

Paralleling Devices

Any number of SL6670 voltage converters may be paralleled to increase output current capability. The reservoir capacitor, pump capacitors and oscillator components serve all devices, see Fig.20. Individual components could be used for the oscillator and pump capacitors on each individual device if required.

Cosc should be doubled when paralleling devices for the same operating frequency.

External Clocking of SL6670

In some applications it may be advantageous to externally control the internal oscillator. This can be achieved as shown in Fig.21.

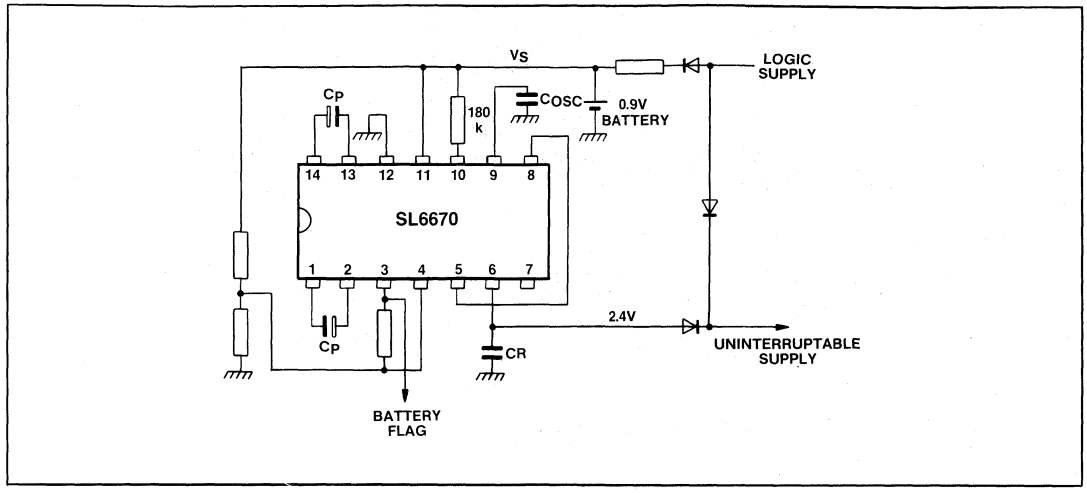


Fig.22 Uninterruptable memory supply

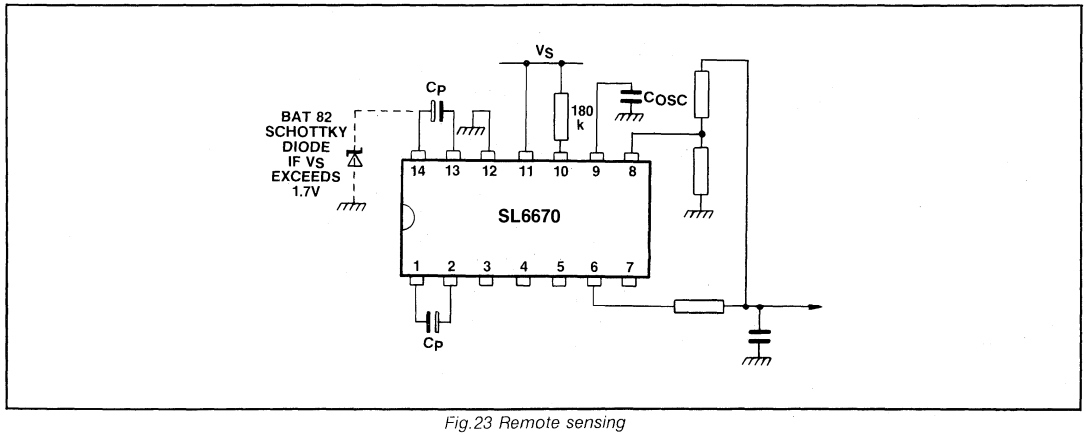


Fig.23 Remote sensing

Uninterruptable Memory Supply

Fig.22 shows the SL6670 being used as a standby memory supply. The battery flag senses when the battery supply is nearly discharged.

Remote Sensing for Regulator

The input to the regulator can be used for remote sensing applications if required. See Fig.23.

Separate Regulator Decoupling

In applications where the high output ripple can be tolerated the regulator can be separately decoupled with a small capacitor on Pin 8 as shown in Fig.24. In applications where large load glitches appear on the output a more complex smoothing network can be incorporated between the output, pin 6, and pin 8 or, for fixed 2.4V output, between pin 5 and pin 8.

3V Battery to 5V Logic Supply

Fig.25 shows the SL6670 used to provide a 5V supply from a 3V battery. The circuit continues to work even when the battery is exhausted at 1.8V. The battery flag will sense when the battery is exhausted.

R1 and R2 set the voltage where the flag is required to switch and R_F sets the value of hysteresis required.

R3 and R4 set the regulated output voltage. In normal operation 0.7V will appear across R4 and V_O-0.7V will appear across R3.

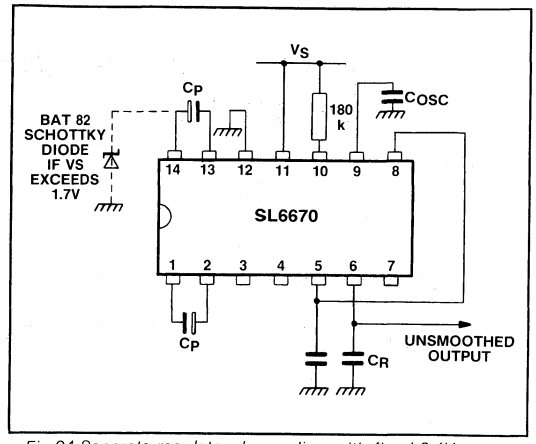


Fig.24 Separate regulator decoupling with fixed 2.4V output

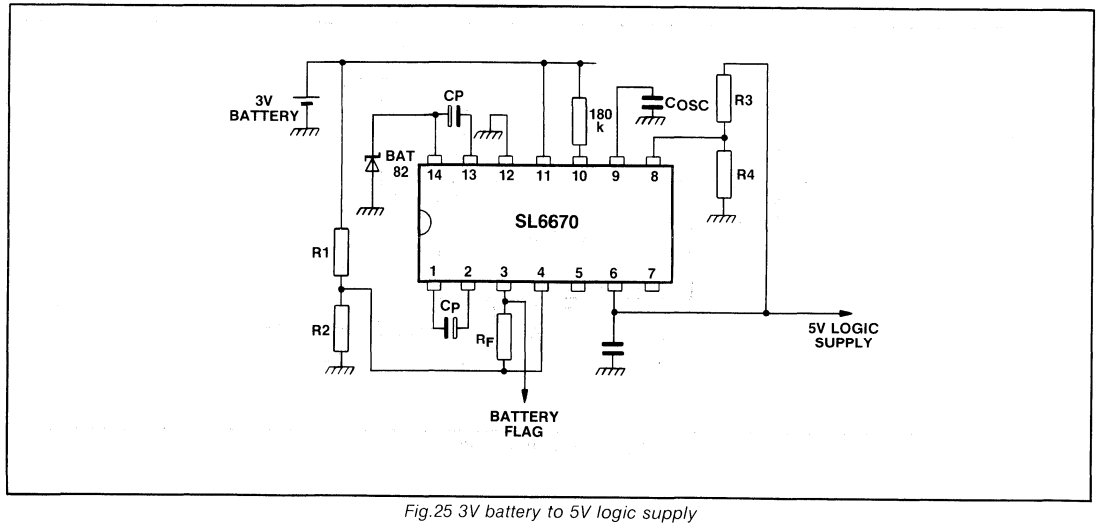


Fig.25 3V battery to 5V logic supply

PLESSEY
Semiconductors

SL6691C

IF SYSTEM FOR PAGING RECEIVERS

The SL6691C is an IF system for paging receivers, consisting of a limiting IF amplifier, quadrature demodulator, voltage regulator and audio tone amplifier with Schmitt trigger.

The voltage regulator requires an external PNP transistor as the series pass transistor. The frequency response of the tone audio amplifier is externally defined.

The SL6691C operates over the temperature range -30° C to +85° C.

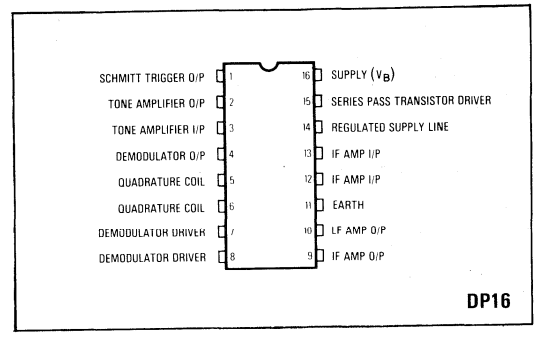


Fig.1 Pin connections (top view)

FEATURES

- Very Low Standby Current
- Fast Turn-on
- Wide Dynamic Range
- Minimum External Components

APPLICATIONS

- Pagers
- Portable FM Broadcast Receivers

ABSOLUTE MAXIMUM RATINGS

Storage temperature – 65°C to + 150°C
Supply voltage 6V

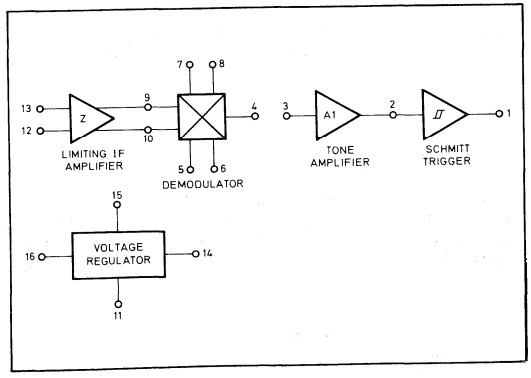


Fig.2 SL6691C block diagram

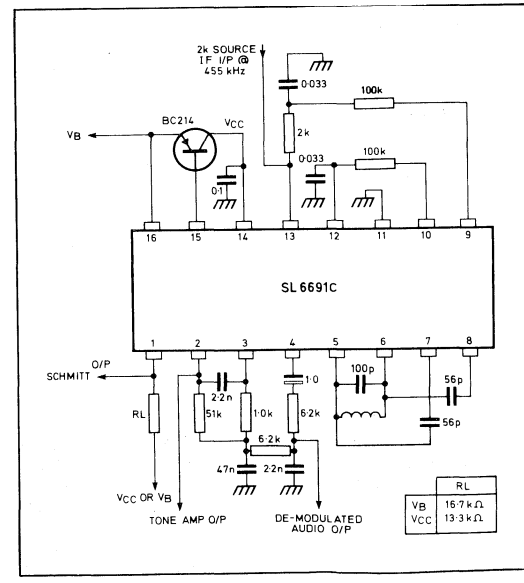


Fig.3 SL6691C test circuit

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Temperature	-30°C to +85°C
Supply voltage (V_C)	2.5V
IF frequency	455kHz (nominal)
Modulation frequency	500Hz
Deviation	±4.5kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Quiescent current		1.0	1.4	mA	V_B = 3V Pins 2 and 3 S/C Pins 1 and 4 O/C
Switch on time		12	18	ms	Note 1
Voltage regulator					
Regulated voltage	1.9		2.1	V	$V_B > 2.2V$
Supply line rejection		40		dB	$V_B > 2.2V$ 200mV p-p square wave @ 500 Hz injected
Current sink capability pin 15	100			µA	
IF amplifier					
Input impedance		20//2		kΩ//pF	
Output impedance		2		kΩ	
Dynamic range		100		dB	
Output voltage swing		600		mV p-p	
Amplifier gain		90		dB	
Sensitivity	20	16		µV rms	Audio 20dB S+N/N ratio
AM rejection		40		dB	100µV rms I/P @ 30% AM modulation
Amplifier 3dB bandwidth		1.5		MHz	
Demodulator					
Audio output	8	15		mV rms	Quadrature element L-C tuned circuit: Q = 30
Distortion, THD		1.5	3	%	
Output impedance		1	3	kΩ	
Signal-to-noise ratio		40		dB	100µV rms I/P 3kHz audio bandwidth
Tone amplifier					
Open loop gain		54		dB	
Peak output current		20		µA	
Schmitt trigger					
Mark space ratio		45/55	38/62		20µV rms I/P
Output current				µA	

NOTES

1. The 'Switch On' time is the time to the zero crossing point of the centre of the first occurrence of a 30/70 or 70/30 mark space wave on the output of the Schmitt trigger after the supply voltage has been switched on. Conditions: V_B = 2V, Tone filter connected (See Fig.3), IF input = 100µV rms, Modulation 500 Hz @ 2kHz deviation.

CIRCUIT DESCRIPTION

IF Amplifier and Detector

The IF amplifier consists of five identical differential amplifier/emitter follower stages with outputs at the fourth (pins 9 and 10) and fifth (pins 7 and 8) stages. The outputs from the fourth stage are used when the lowest turn-on time is required. Coupling to the quadrature network of the detector is via external capacitors; otherwise the design is conventional. The audio output is taken from pin 4 and filtered externally.

Tone (Audio) Amplifier

The tone amplifier is a simple inverting audio amplifier with voltage gain determined by the ratio of feedback resistor to input resistor. The frequency response can readily be controlled by suitable selection of feedback components.

Schmitt Trigger

The Schmitt trigger has an open collector output stage which saturates when the input at pin 2 is high. A 20µV rms input is sufficient.

NOMINAL DC PIN VOLTAGES(DP16)

Function	Pin	Voltage
Supply	16	Battery voltage
Series pass transistor driver	15	Battery voltage –0.7V
Regulated supply line	14	2V
Earth	11	0V
IF amp I/P	13	1V
IF amp I/P	12	1V
IF amp O/P	10	1V
IF amp O/P	9	1V
Demodulator O/P	4	1V
Quadrature coil	6	1V
Quadrature coil	5	1V
Tone amplifier I/P	3	1.4V
Schmitt trigger O/P	1	0V or pin 16 or pin 14
Tone amplifier O/P	2	1.4V
Demodulator driver	7	1V
Demodulator driver	8	1V

PLESSEY
Semiconductors

SL6700A

IF AMPLIFIER AND AM DETECTOR WITH NOISE BLANKER

The SL6700A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable. This device is characterised for operation from -55°C to +125°C.

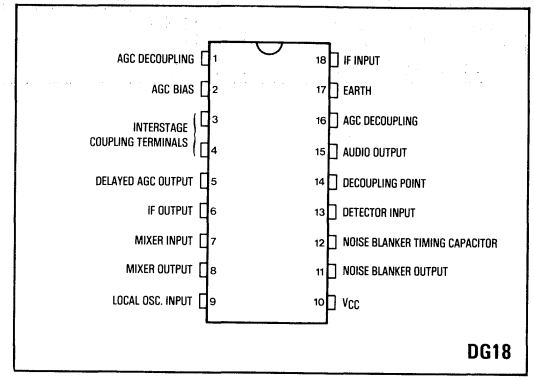


Fig.1 Pin connections (top view)

FEATURES

- High Sensitivity: 10µV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

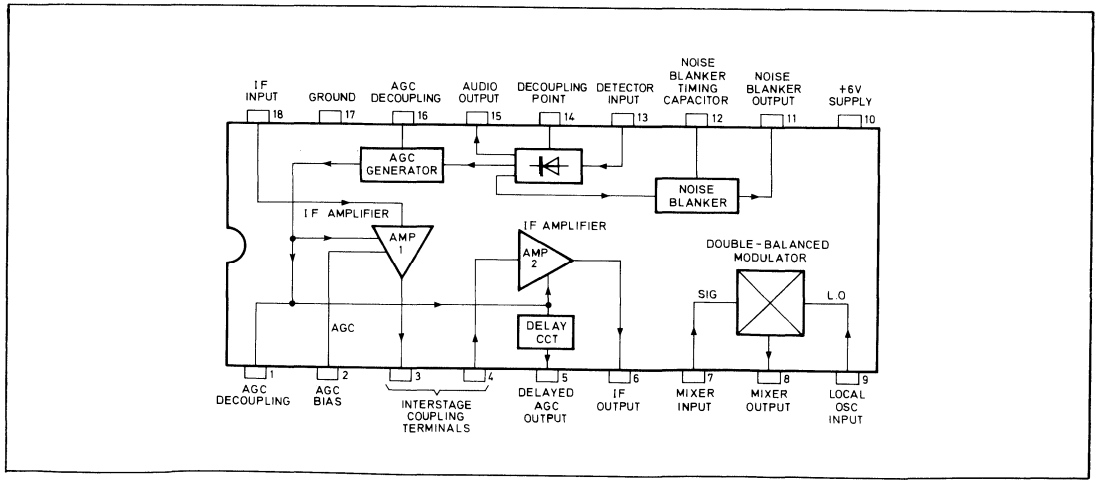


Fig.2 SL6700A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} -55°C to +125°C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	1mV input 30% modulation
Sensitivity	10	5		μV	10dB S + N/N ratio, 30%
Audio output level change		6	10	dB	10μV to 50mV input 80%
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	4.0			V	Logic 1
			0.3	V	Logic 0
Noise blank duration	300	400	500	μs	C pin 12 = 30nF,R pin 12-11 = 18k
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (L.O.)	3	5	8	kΩ	
Mixer L.O. injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 30μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

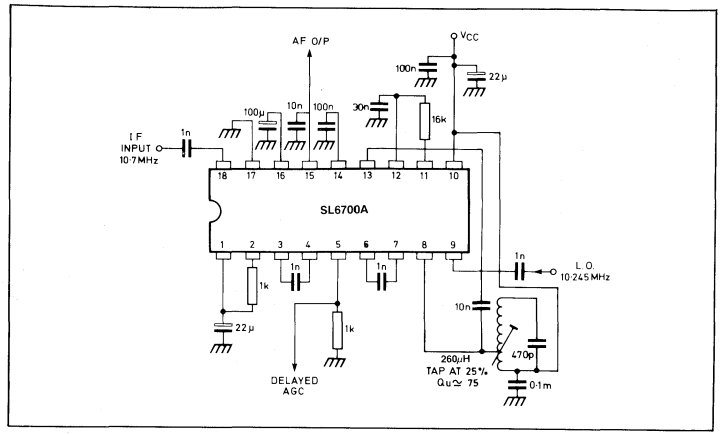


Fig.3 SL6700A AM double conversion receiver with noise blanker

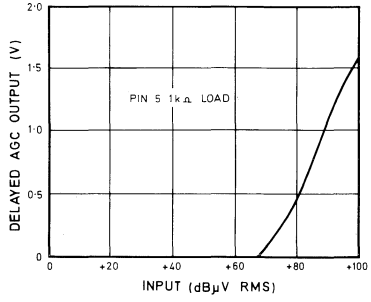


Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

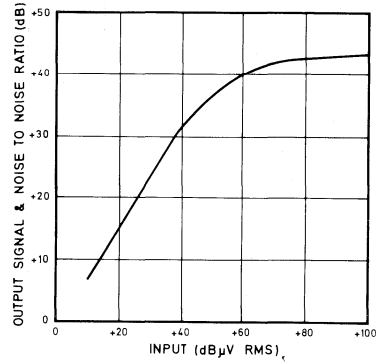


Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

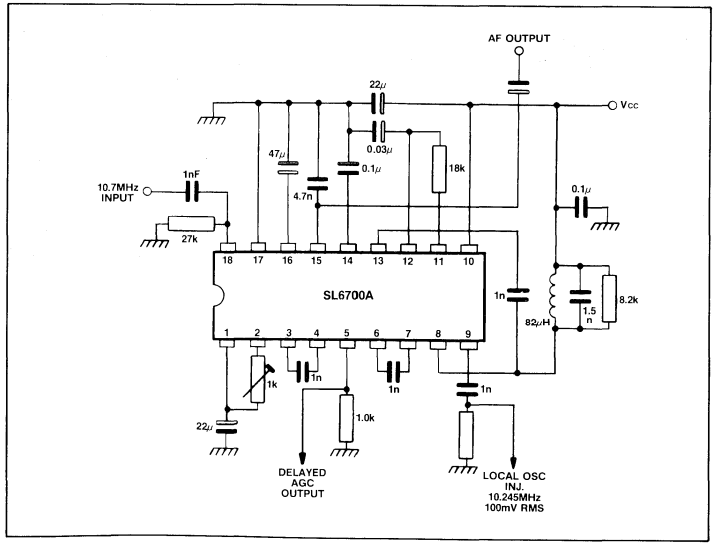


Fig.6 Test circuit

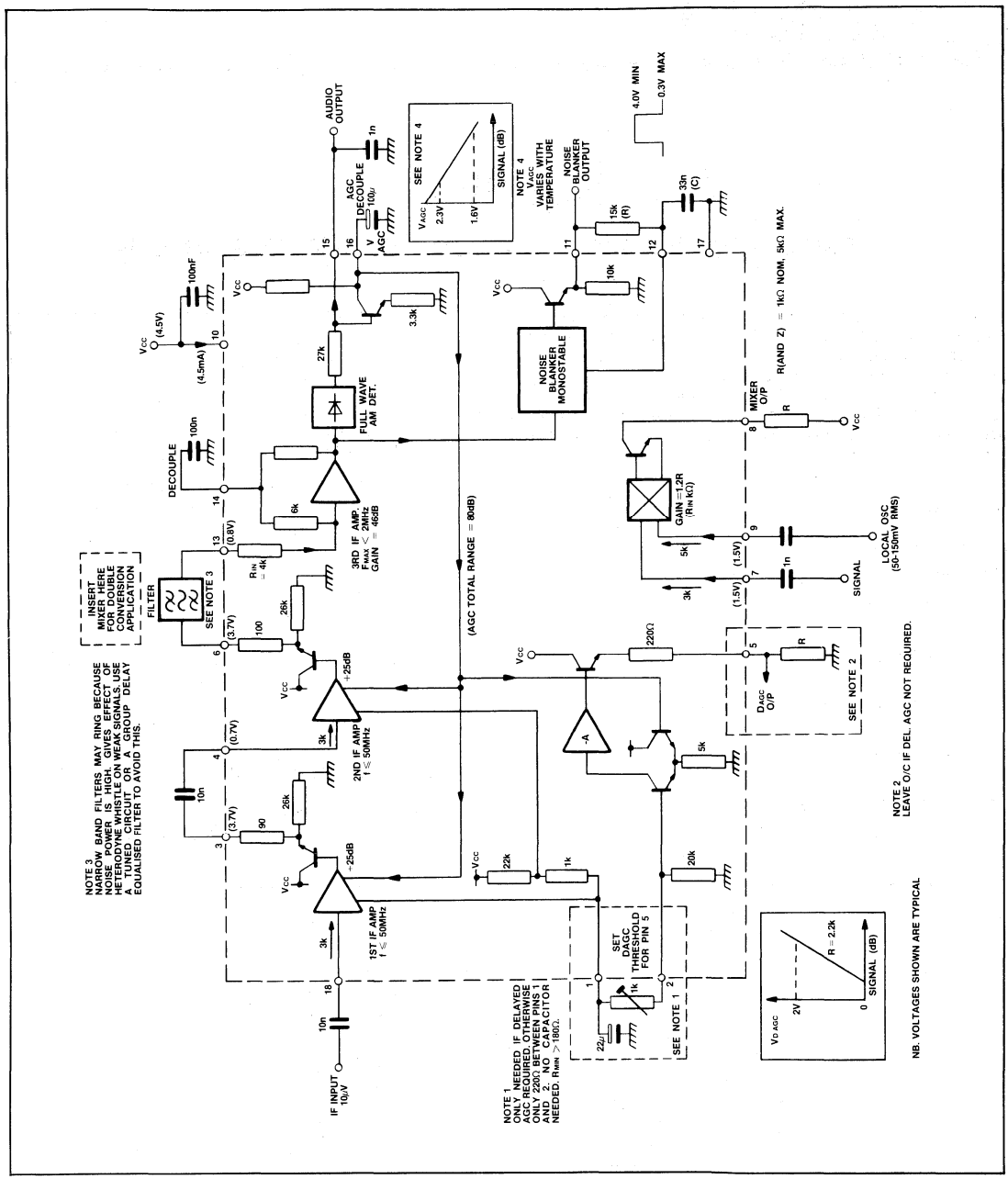


Fig.7 SL6700A Typical application circuit showing interfacing

SL6700C

IF AMPLIFIER AND AM DETECTOR WITH NOISE BLANKER

The SL6700C is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6700C will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector, an AGC generator with optional delayed output and a noise blanker monostable.

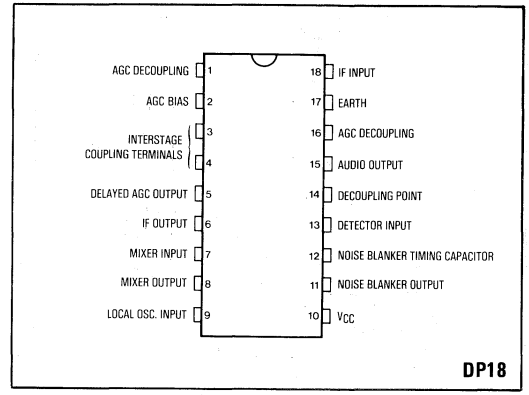


Fig. 1 Pin connections (top view)

FEATURES

- High Sensitivity: 10μV minimum
- Low Power: 8mA Typical at 6V
- Linear Detector

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

ABSOLUTE MAXIMUM RATINGS

Supply voltage: 7.5V
Storage temperature: −55°C to +125°C

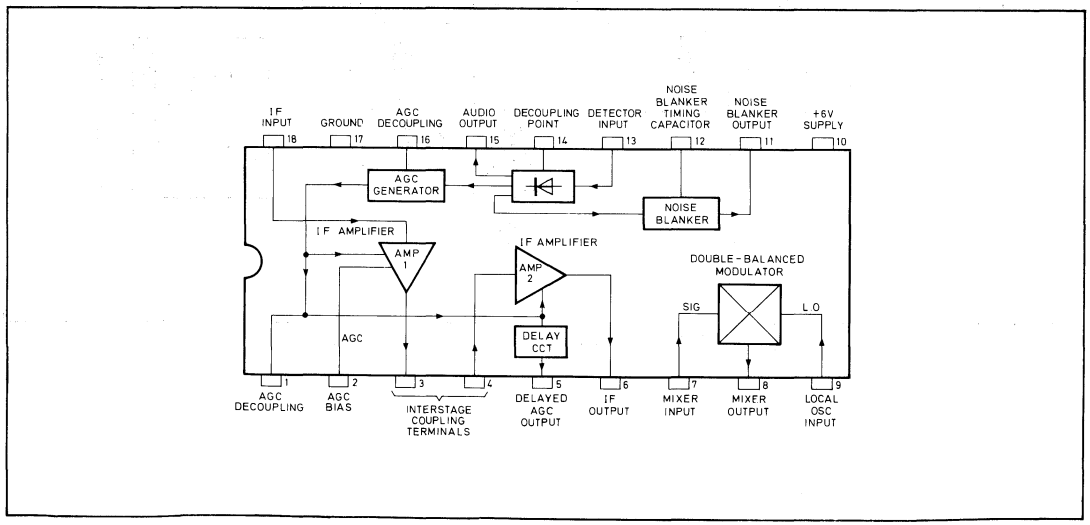


Fig. 2 SL6700C block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage 4.5V
T_{Amb} -30°C to +85°C

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		4.5	6	mA	
S/N ratio		40		dB	1mV input 80% mod @ 1kHz
TH distortion		1	5	%	1mV input 80% mod @ 1kHz
Sensitivity	10	5		μV	10dB S + n/N ratio, 30% mod 1kHz
Audio output level change		6	10	dB	10μV to 50mV input 80% mod 1kHz
AGC threshold		5		μV	
AGC range		80		dB	
AF output level		25		mV rms	30 % modulation 1kHz
Delayed AGC threshold		10		mV rms	80 % modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	40	50		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM 1kHz
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Noise blank level	2.7			V	Logic 1
			0.6	V	Logic 0
Noise blank duration		300		μs	C pin 12 = 30nF
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (signal)	2	3	5	kΩ	
Mixer Z_{in} (LO)	3	5	8	kΩ	
Mixer LO injection	20	50	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, 1kHz modulation increased from 30% to 80%

OPERATING NOTES

The noise blank duration can be varied from the suggested value of 300μs using the formula: Duration time = 0.7CR, where R is value of resistor between pins 11 and 12 and C is value of capacitor from pin 12 to ground.

There is no squelch in the SL6700C and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

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(Supply 4.5V, Input 1mV)

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2	2.09V	11	3.7V
3	3.68V	12	0V
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

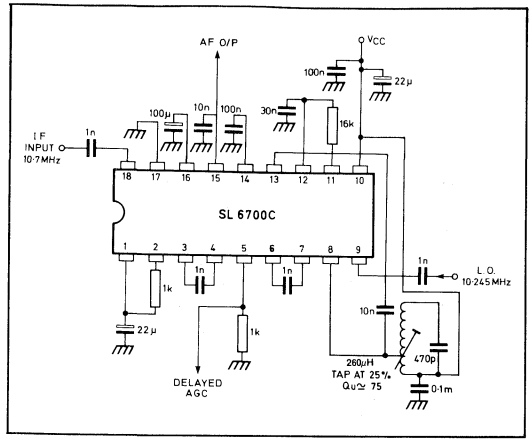


Fig. 3 SL6700C AM double conversion receiver with noise blanker

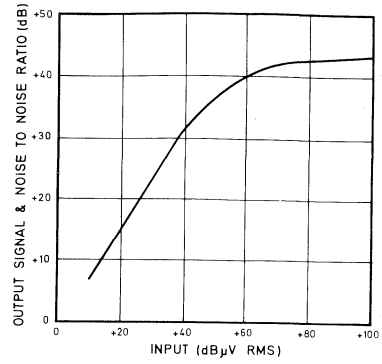


Fig. 5 Typical signal to noise ratio (S+N/N) with input signal (f=10.7MHz, 30% modulation)

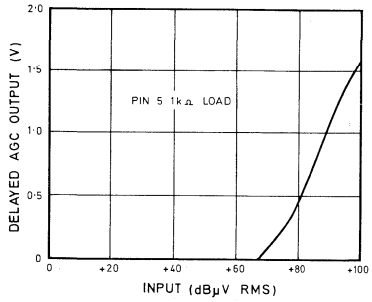


Fig. 4 Typical delayed AGC output variation with input signal (f=10.7MHz, 30% modulation)

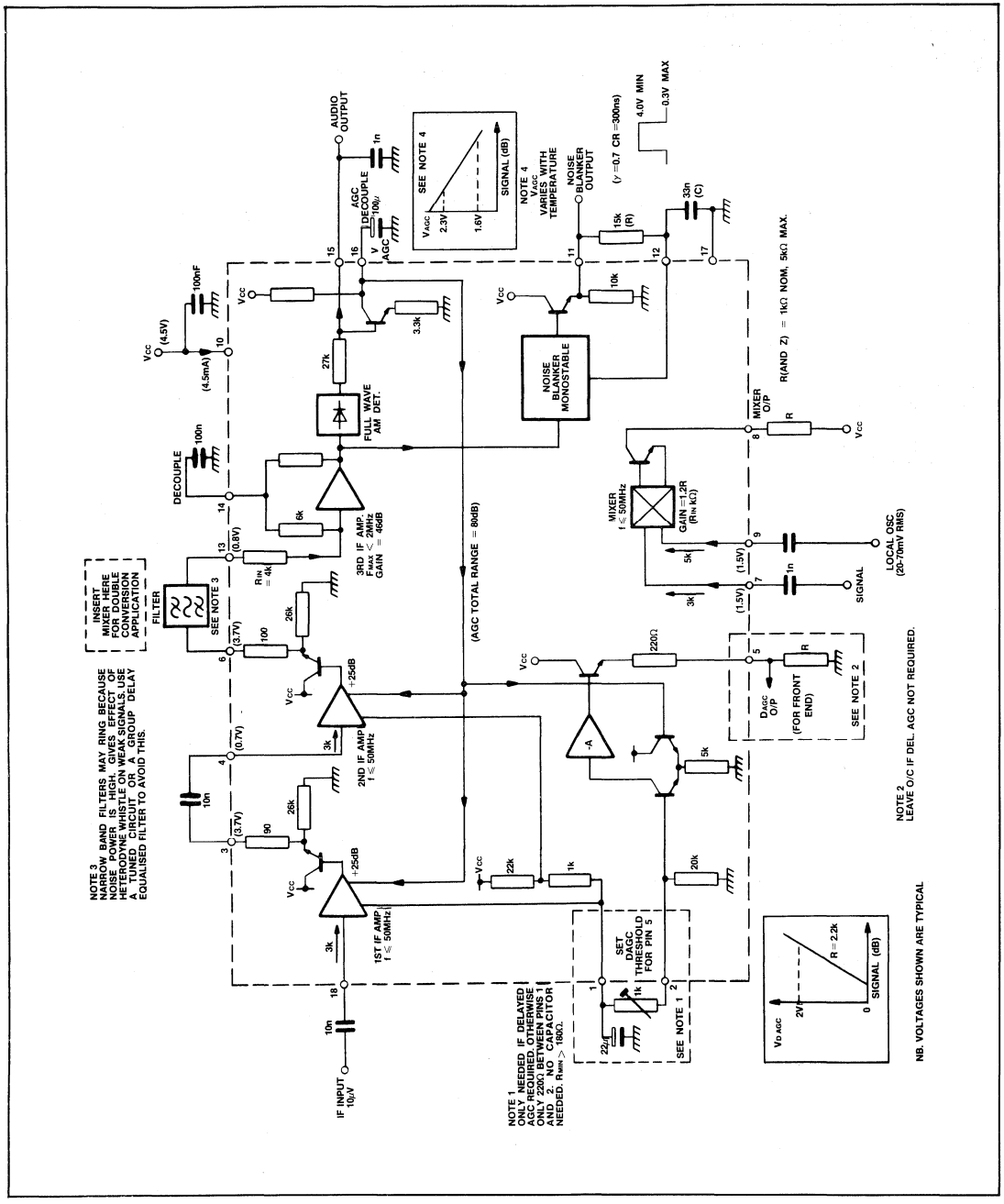


Fig.6 SL6700C Typical application circuit showing interfacing

PLESSEY
Semiconductors

SL6701A

AM IF AND DETECTOR (DOUBLE CONVERSION)

The SL6701A is a single or double conversion IF amplifier and detector for AM radio applications. Its low power consumption makes it ideal for hand held applications. Normally the SL6701A will be fed with a first IF signal of 10.7MHz or 21.4MHz; there is a mixer for conversion to the first or second IF, a detector and an AGC generator with optional delayed output. This device is characterised for operation from -55°C to +125°C.

FEATURES

- High Sensitivity: 10uV Minimum
- Low Power: 8mA Typical at 6V
- Linear Detector
- Full MIL Temperature Range

APPLICATIONS

- Low Power AM/SSB Receivers

QUICK REFERENCE DATA

- Supply Voltage: 4.5V
- Input Dynamic Range: 100dB Typical

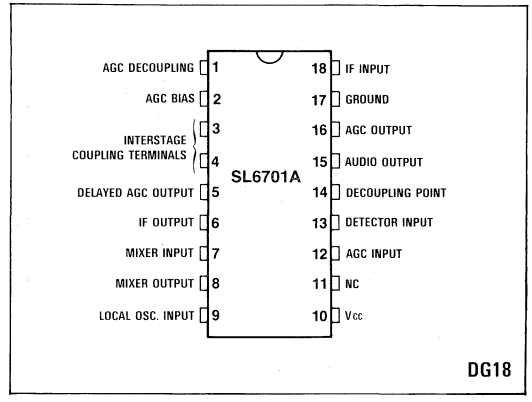


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage	7.5V
Storage temperature	-55°C to +150°C
Operating temperature	-55°C to +125°C

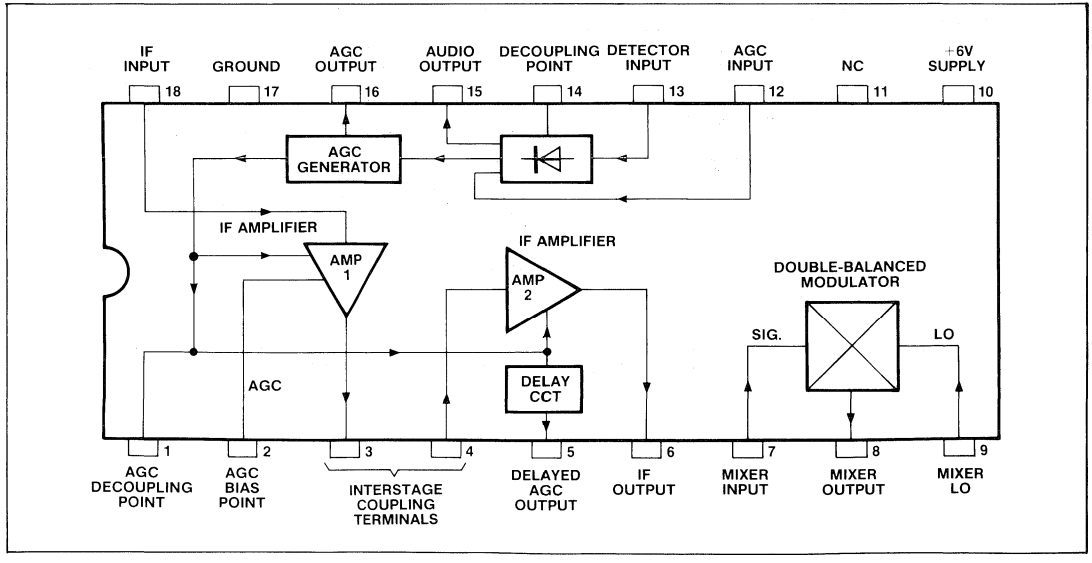


Fig.2 SL6701A block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)

T_{amb} = -55°C to +125C Test circuit Fig.6. Modulation frequency 1kHz

Characteristic	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply voltage	4		7	V	Optimum performance at 4.5V
Supply current		3.5	7	mA	
S/N ratio		40		dB	1mV input 80% modulation
TH distortion		3	5	%	1mV input 30% modulation
Sensitivity	10	5		μV	10dB S + N/N ratio, 30%
Audio output level change		6	10	dB	10μV to 50mV input 80%
AGC threshold		5		μV	
AGC range		80		dB	
AF output level	20	40		mV rms	30% modulation 1mV input
Delayed AGC threshold		10		mV rms	80% modulation
Dynamic range		100		dB	Noise floor to overload
IF frequency response	15	25		MHz	3dB gain reduction
IF amplifier gain	40	50	60	dB	10.7MHz (both amplifiers cascaded)
Detector gain	40	46	55	dB	455kHz 80% AM
Detector Z_{in} pin 13	2	4	6.8	kΩ	
IF amplifier Z_{in} pin 18	1.8	3	4.5	kΩ	
Mixer conversion gain	1.0R	1.2R	1.5R	kΩ	R is load resistor in kΩ
Mixer Z_{in} (Signal)	2	3	5	kΩ	
Mixer Z_{in} (LO)	3	5	8	kΩ	
Mixer LO injection	50	100	150	mV rms	fc = 10.245MHz
Detector output voltage change	6	8	8.2	dB	1mV rms input, modulation increased from 30% to 80%

OPERATING NOTES

There is no squelch in the SL6701A and the delay in the delayed AGC is too large to make this output suitable. Squelch is best obtained from a comparator on the AGC decoupling point, pin 16.

The IF amplifiers may be operated at 455kHz giving a single conversion system.

The mixer may also be used as a product detector. Further application information is available on request.

TYPICAL DC PIN VOLTAGES

(Supply 4.5V, Input 1mV)

Pin	Voltage	Pin	Voltage
1	2.25V	10	4.5V
2	2.09V	11	2.5V*
3	3.68V	12	
4	0.7V	13	0.77V
5	0.6V	14	1.5V
6	3.7V	15	1.0V
7	1.5V	16	0.7V
8	4.3V	17	0V
9	1.5V	18	0.7V

* Pins 11 and 12 connected together

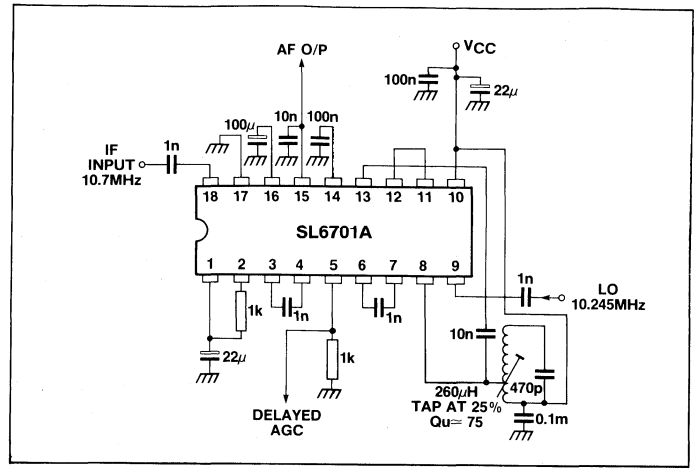


Fig.3 SL6701A AM double conversion receiver with noise blanker

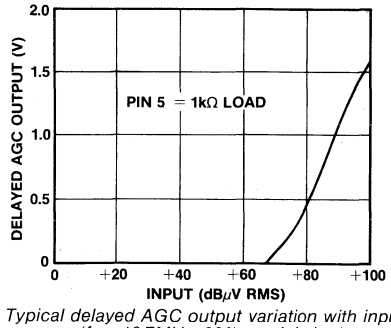


Fig.4 Typical delayed AGC output variation with input signal (f = 10.7MHz, 30% modulation)

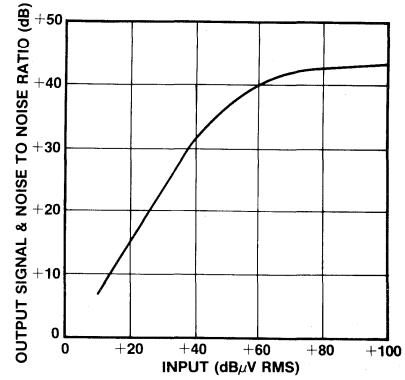


Fig.5 Typical signal to noise ratio (S + N/N) with input signal (f = 10.7MHz, 30% modulation)

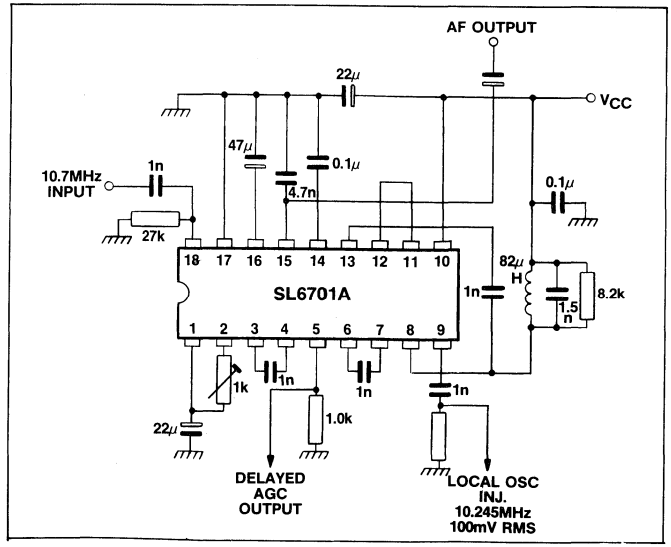


Fig.6 Test circuit

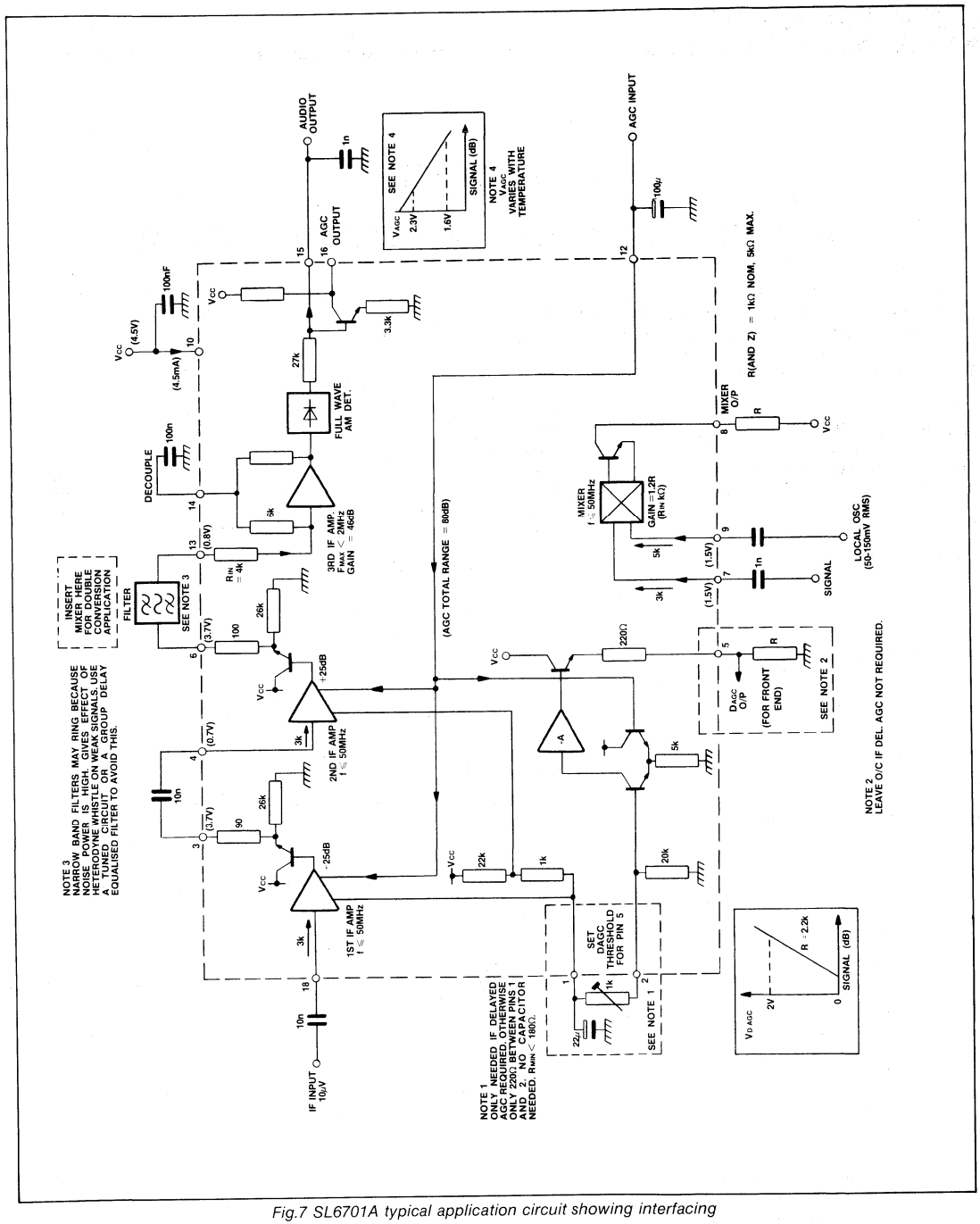


Fig.7 SL6701A typical application circuit showing interfacing

TAB1043

QUAD PROGRAMMABLE OPERATIONAL AMPLIFIER

The TAB1043 is an advanced bipolar integrated circuit containing four separate operational amplifiers. The amplifiers are programmed by current into the appropriate bias pin. Pin 8 (Bias 2) programmes amplifiers B, C and D and pin 16 (Bias 1) programmes amplifier A.

For example, with a suitable choice of bias current, the TAB1043 will perform in a manner similar to four amplifiers of the 741 type, but with improved frequency response and input characteristics.

The TAB1043 is especially suitable for use in active filter applications.

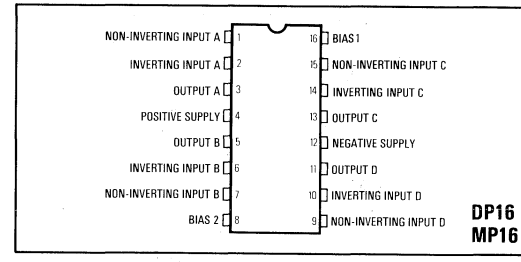


Fig. 1 Pin connections

FEATURES

- Four Independent Op. Amps. in One Package
- Internally Compensated
- Wide Range of Supply Voltages from ±1.5V to ±12V
- No Latch-Up
- Programmable Over 100 :1 Current Range
- Gain Bandwidth Product Up to 4MHz
- Built-In Short Circuit Protection
- Very Low Noise

APPLICATIONS

- Active Filters
- Oscillators
- Low Voltage Amplifiers

QUICK REFERENCE DATA

- Supply Voltages ±1.5V to ±12V
- Supply Current ±40uA to ±2mA
- Operating Frequency Range 1MHz
- Gain 95dB
- Operating Temperature Range -40°C to +85°C

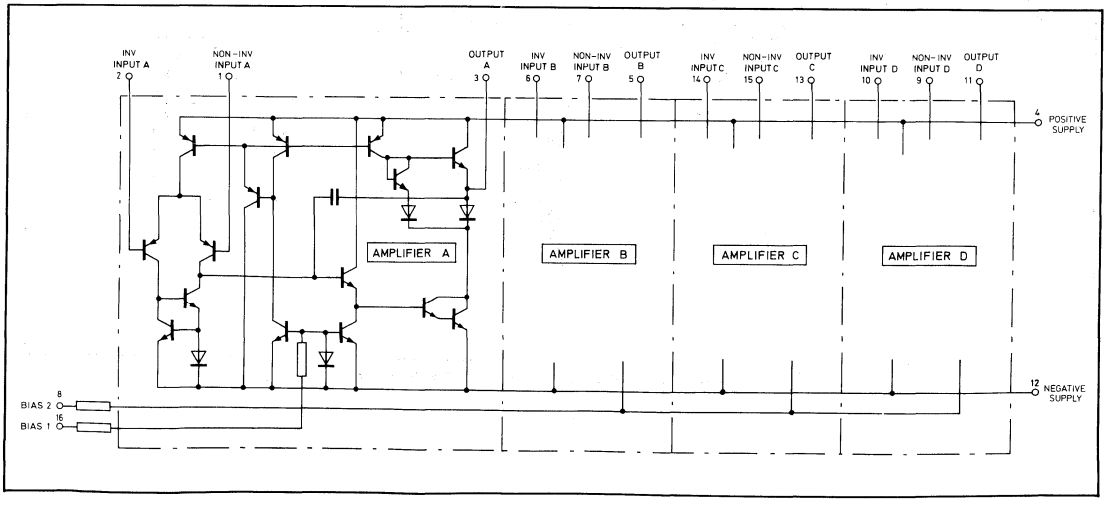


Fig. 2 Circuit diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} 25°C
Operating mode A: Supply volts ±12V Bias set current 75μA
Operating mode B: Supply volts ±12V Bias set current 1μA
Operating mode C: Supply volts ±1.5V Bias set current 1μA

Characteristics	Operating Mode									Units	Conditions
	A			B			C				
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Input offset voltage		1	5		1	5		1	5	mV	R_S 10kΩ
Input offset current		20	200		5	50		5	50	nA	
Input bias current		250	500		30	100		30	100	nA	
Input resistance	0.1	0.6		0.5	2		0.5	2		MΩ	
Supply current (each amplifier)	1000	1600	2200		42		20	40	60	μA	
Large signal volt gain	74	95		66	90		66	90		dB	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 100kΩ(C)
Input voltage range	10	10.5		10	10.5		0.2	0.4		±V	R_S 10kΩ
Common mode rejection ratio	70	110			82			82		dB	
Output voltage swing	9	10.8		9	10.8		0.2	0.3		±V	RL = 4kΩ(A)
											RL = 100kΩ(B)
											RL = 4kΩ(C)
Supply voltage rejection ratio	75	96		75	86		75	86		dB	R_S 10kΩ
Gain bandwidth product					50			50		kHz	Gain = 20dB
		3.5								MHz	
Slew rate		1.5			0.02			0.02		V/μs	Gain = 20dB
Input noise voltage		15			45			45		nV/√Hz	f_o = 1kHz
Input noise current		1.6			1.6			1.0		pA/√Hz	f_o = 1kHz

OPERATING NOTES

Bias set current

The amplifiers are programmed by the I_{SET} current into the BIAS pin to determine the frequency response, slew rate and the value of supply current. The relationship is summarised as follows:

Gain bandwidth product	I_{SET} x 50kHz
Power supply current (each amplifier)	I_{SET} x 25μA
Slew rate	I_{SET} x 0.02 V/μs (I_{SET} in μA)

The open loop voltage gain is largely unaffected by change in bias set current but tends to peak slightly at 10μA.

Since the voltage on the BIAS pin is approximately 0.65V more positive than the negative supply, a resistor may be connected between the bias pin and either 0V or the positive supply to set the current. Thus, if the resistor is connected to 0V, the I_{SET} current is determined by:

$$I_{SET} = \frac{Vs - 0.65}{R}$$

where R is value of the 'set' resistor.

The output goes high if the non-inverting input is taken lower than 1V above the negative power supply.

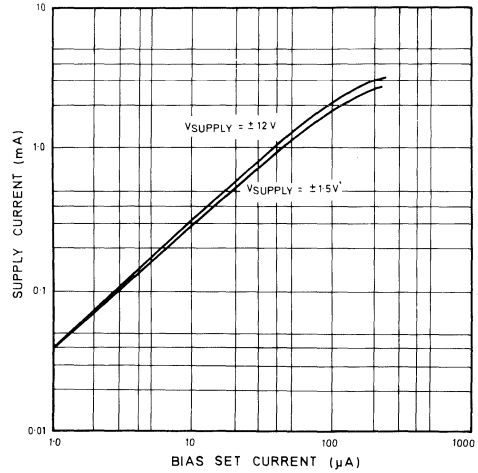


Fig.3 Supply current (each amplifier) v. bias set current

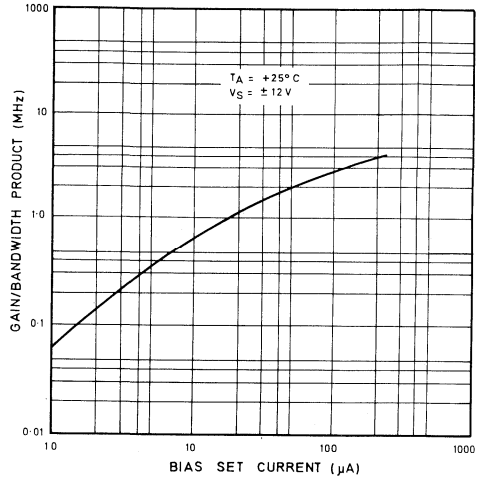


Fig. 4 Gain bandwidth product v. I_{SET}

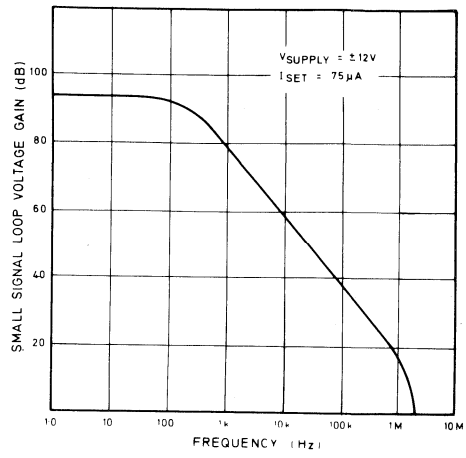


Fig. 5 Typical frequency response

ABSOLUTE MAXIMUM RATINGS

Supply voltages	±15V
Common mode input voltage	Not greater than supplies
Differential input voltage	±25V
Bias set current	10mA each pin
Storage	-55° C to +125° C
Power dissipation	800mW at 25° C
	Derate at 7mW/° C above 25° C
Operating temperature range	-40° C to +85° C

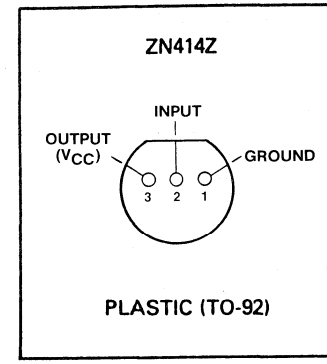
PLESSEY
Semiconductors

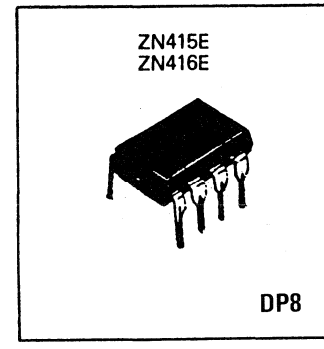
ZN414Z, ZN415E, ZN416E

AM RADIO RECEIVERS

FEATURES

- Single cell operation (1.1 to 1.6 volt operating range)
- Low current consumption
- 150kHz to 3MHz frequency range (i.e. full coverage of medium and long wavebands)
- Easy to assemble, no alignment necessary
- Simple and effective AGC action
- Will drive crystal earphone direct (ZN414Z)
- Will drive headphones direct (ZN415E and ZN416E)
- Excellent audio quality
- Typical power gain of 72dB (ZN414Z)
- Minimum of external components required





GENERAL DESCRIPTION

The ZN414Z is a 10 transistor tuned radio frequency (TRF) circuit packaged in a 3-pin TO-92 plastic package for simplicity and space economy.

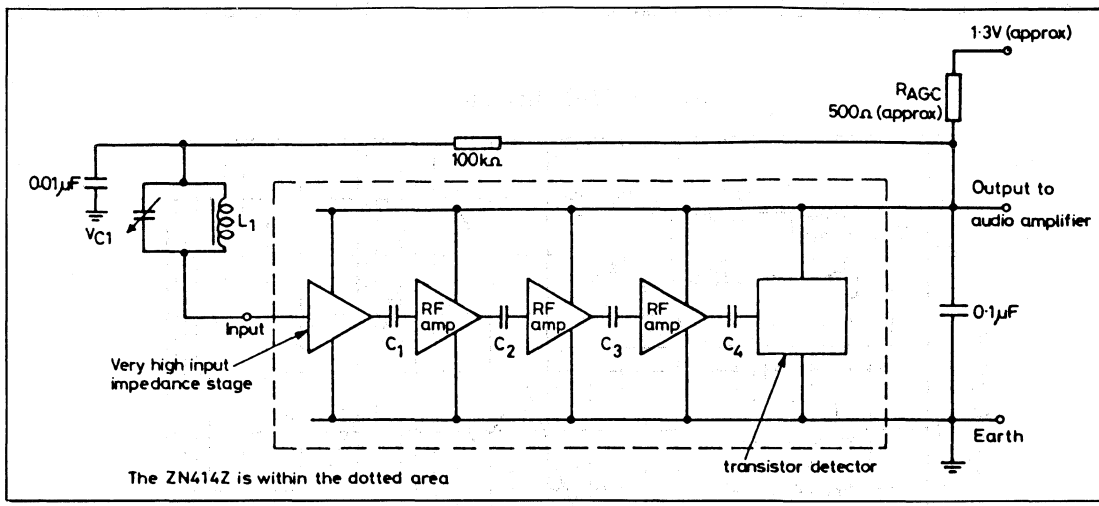
The circuit provides a complete R.F. amplifier, detector and AGC circuit which requires only six external components to give a high quality A.M. tuner. Effective AGC action is available and is simply adjusted by selecting one external resistor value. Excellent audio quality can be achieved, and current consumption is extremely low. No setting-up or alignment is required and the circuit is completely stable in use.

The ZN415E retains all the features of the ZN414Z but also incorporates a buffer stage giving sufficient output to drive headphones directly from the 8 pin DIL.

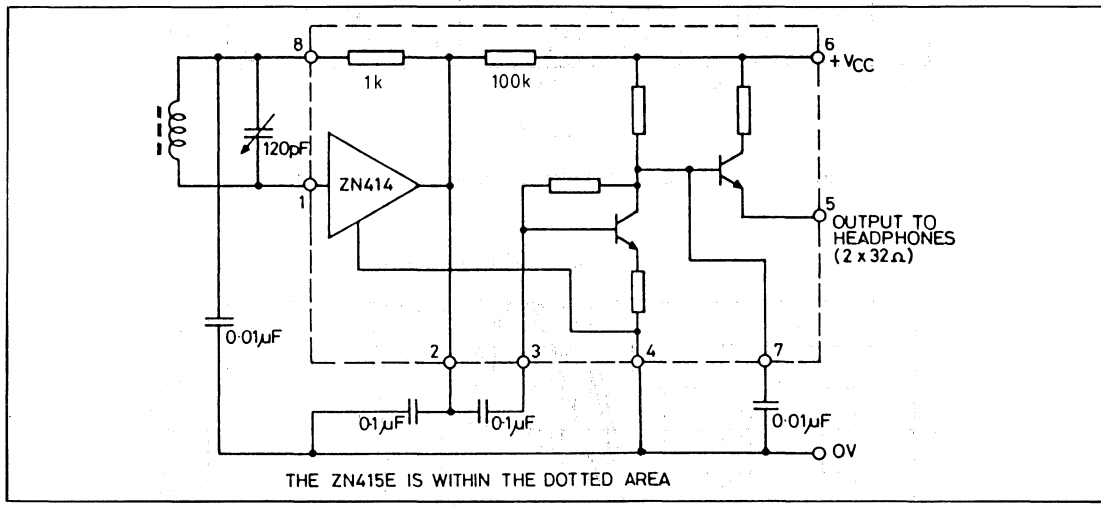
Similarly the ZN416E is a buffered output version of the ZN414Z giving typically 120mV (r.m.s.) output into a 64Ω load. The same package and pinning is used for the ZN416E as the ZN415E.

DEVICE SPECIFICATIONS $T_{amb} = 25°C$, $V_{CC} = 1.4V$. Parameters apply to all types unless otherwise stated.

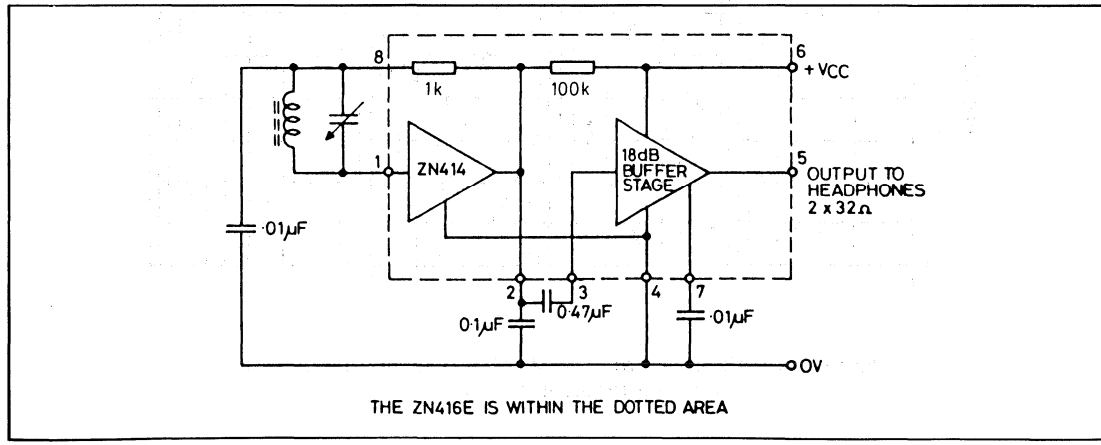
Parameter		Min.	Typ	Max.	Units
Supply voltage, V_{CC}		1.1	1.3	1.6	volts
Supply current, I_S with 64Ω headphones	ZN414Z	-	0.3	0.5	mA
	ZN415E		2.3	3	
	ZN416E		4	5	
Input frequency range		0.15	-	3.0	MHz
Input resistance		-	4.0	-	MΩ
Threshold sensitivity (Dependant on Q of coil)			50		μV
Selectivity		-	4.0	-	kHz
Total harmonic distortion		-	3.0	-	%
AGC range		-	20	-	dB
Power gain (ZN414Z)			72		dB
Voltage gain of output stage	ZN415E	-	6	-	dB
	ZN416E		18		
Output voltage into 64Ω load before clipping	ZN414Z	-	60	-	mVpp
	ZN415E		120		
	ZN416E		340		
Upper cut-off frequency of output stage, No capacitor, (ZN415E and ZN416E)		20	-	-	kHz
With 0.01μF between pin 7 and 0V (ZN415E)		-	6	-	kHz
With 0.01μF between pin 7 and 0V (ZN416E)		-	10	-	kHz
Lower cut-off frequency of output stage 0.1μF between pins 2 and 3 for ZN415E 0.47μF between pins 2 and 3 for ZN416E		-	50	-	Hz
Quiescent output voltage	ZN414Z	-	40	-	mV
	ZN415E		80		
	ZN416E		200		
Operating temperature range		0	-	70	°C
Maximum storage temperature		−65	-	125	°C



ZN414Z System Diagram



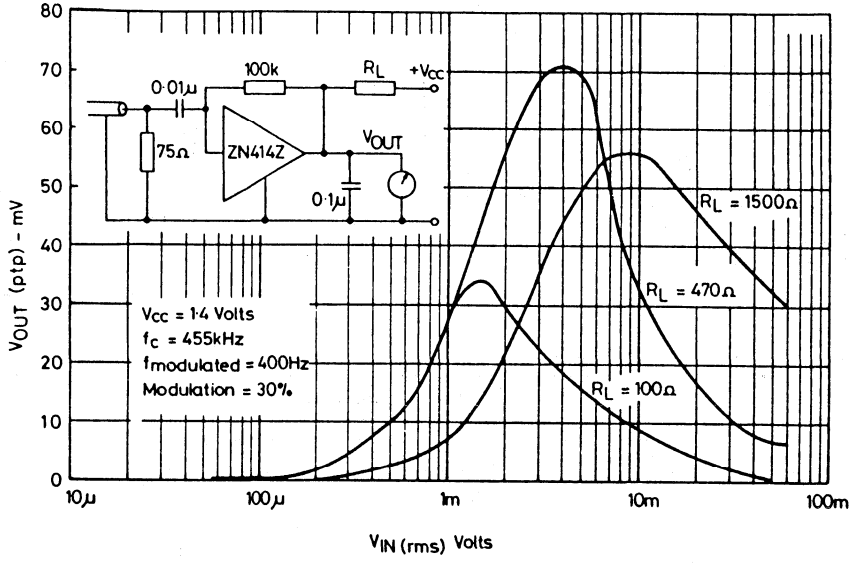
ZN415E System Diagram



ZN416E System Diagram

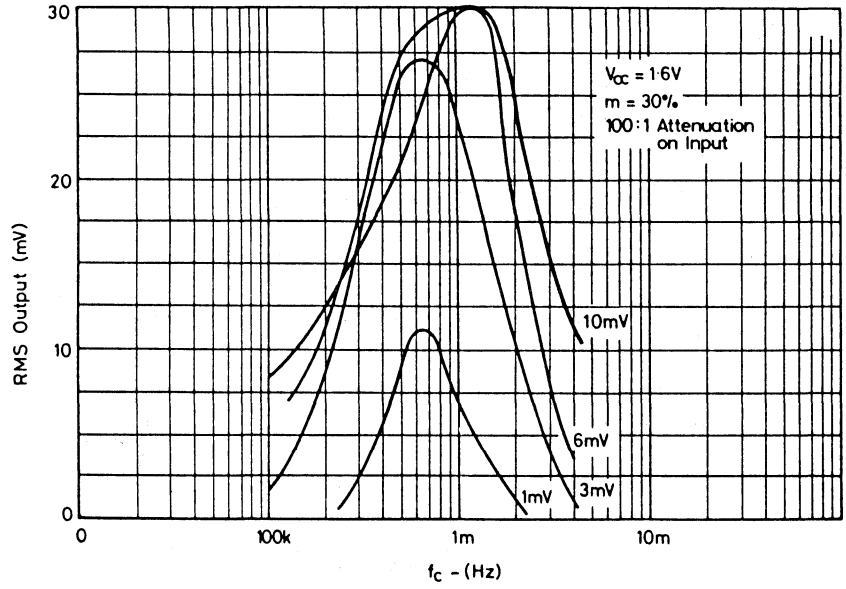
ZN414Z CHARACTERISTICS – All measurements performed with 30% modulation, $F_M = 400Hz$

Gain and AGC characteristics



See operating notes for explanation of AGC action.

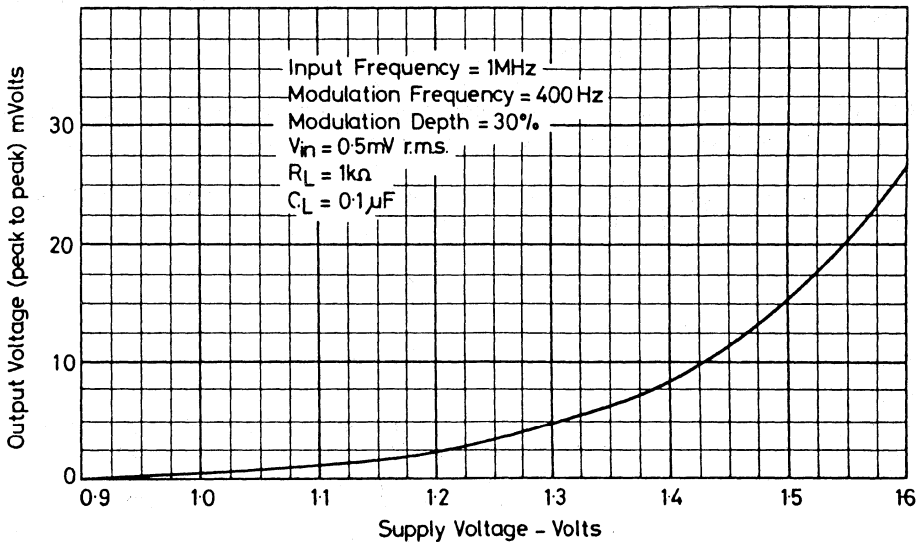
Frequency response of the ZN414Z



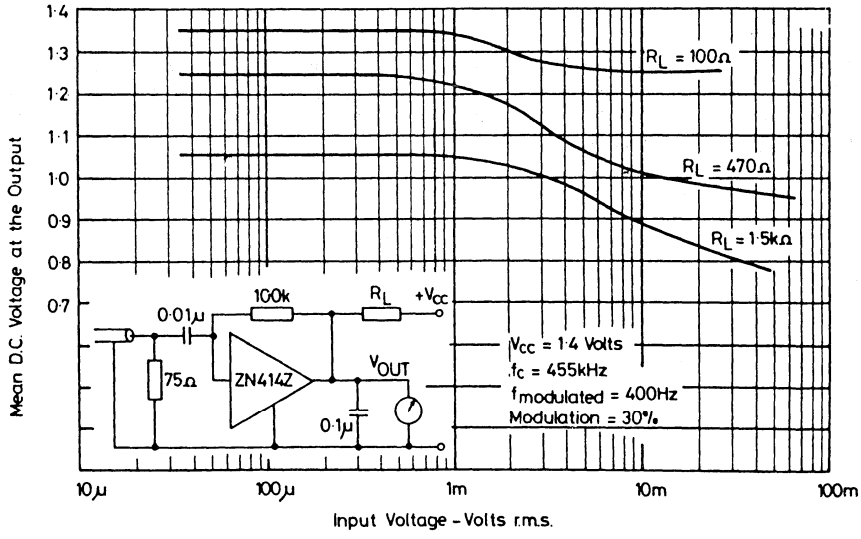
Note that this graph represents the chip response, and not the receiver bandwidth.

ZN414Z CHARACTERISTICS – *(Continued)*

Gain variation with supply volts.



D.C. level at output



LAYOUT REQUIREMENTS

As with any high gain R.F. device, certain basic layout rules must be adhered to if stable and reliable operation is to be obtained. These are listed below:

1. The output decoupling capacitor should be soldered as near as possible to the output and earth leads of the ZN414Z. Furthermore, its value together with the AGC resistor (R_{AGC}) should be calculated at $\approx$4kHz, i.e.:

$$C \text{ (farads)} = \frac{1}{2\pi \cdot R_{AGC} \cdot 4 \cdot 10^3}$$

2. All leads should be kept as short as possible, especially those in close proximity to the ZN414Z.
3. The tuning assembly should be some distance from the battery, loudspeaker and their associated leads.
4. The 'earthy' side of the tuning capacitor should be connected to the junction of the 100kΩ resistor and the 0.01μF capacitor.

OPERATING NOTES

(a) Selectivity

To obtain good selectivity, essential with any T.R.F. device, the ZN414Z must be fed from an efficient, high 'Q' coil and capacitor tuning network. With suitable components the selectivity is comparable to superhet designs, except that a very strong signal in proximity to the receiver may swamp the device unless the ferrite rod aerial is rotated to "null-out" the strong signal.

Two other factors affect the apparent selectivity of the device. Firstly, the gain of the ZN414Z is voltage sensitive (see previous page) so that, in strong signal areas, less supply voltage will be needed to obtain correct AGC action. Incorrect adjustment of the AGC causes a strong station to occupy a much wider bandwidth than necessary and in extreme cases can cause the RF stages to saturate before the AGC can limit RF gain. This gives the effect of swamping together with reduced AF output. All the above factors have to be considered if optimum performance is to be obtained.

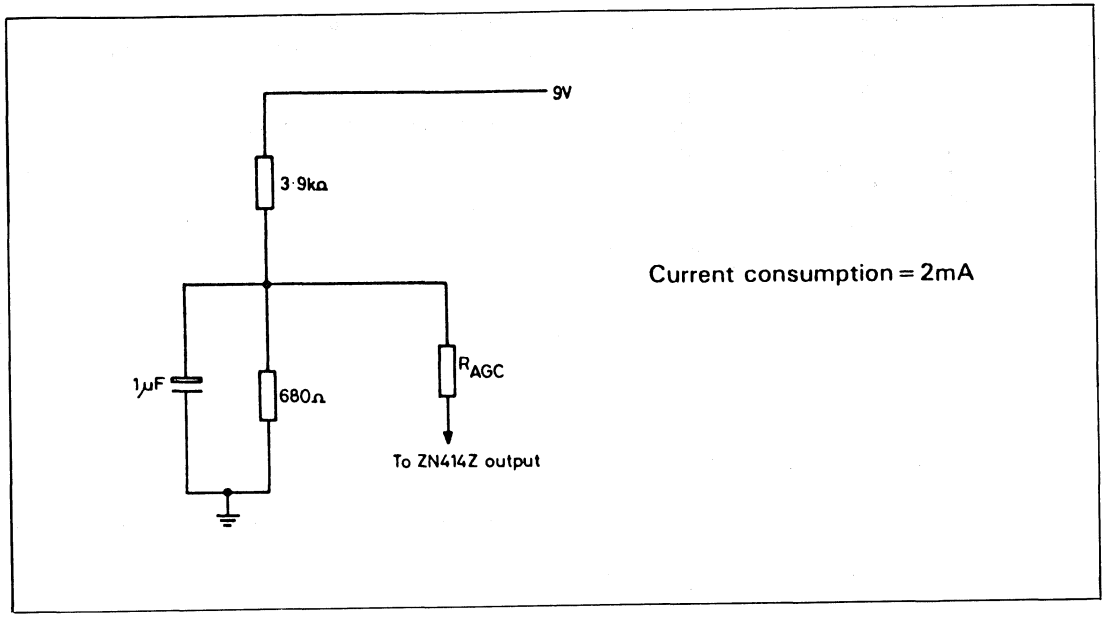
(b) Ferrite aerial size

Because of the gain variation available by altering supply voltage, the size of the ferrite rod is relatively unimportant. However, the ratio of aerial rod length to diameter should ideally be large to give the receiver better directional properties. Successful receivers have been constructed with ferrite rod aerials of 4cm (1.5") and up to 20cm (8").

DRIVE CIRCUITS

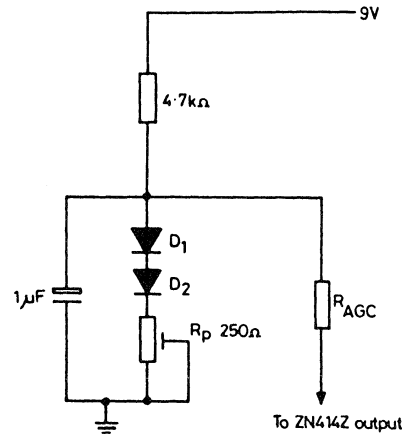
Three types of drive circuit are shown, each has been used successfully. The choice is largely an economic one, but circuit 3 is recommended wherever possible, having several advantages over the other circuits. Values for 9V supplies are shown, simple calculations will give values for other supplies.

1. Resistive Divider (ZN414Z)



Note: Replacing the 680Ω resistor with a 500Ω resistor and a 250Ω preset, sensitivity may be adjusted and will enable optimum reception to be realised under most conditions.

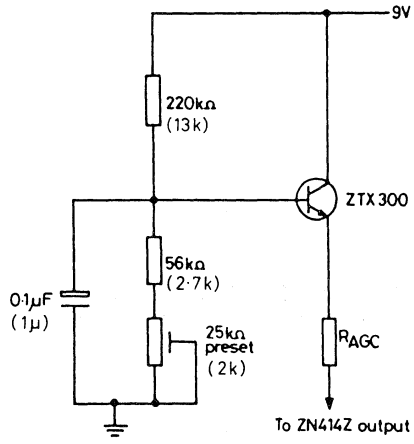
2. Diode Drive (ZN414Z)



$D_1 = D_2$ = Any general purpose silicon diode
R_p = Optional sensitivity control, a recommended value being 250Ω.

Current consumption ≈ 1.5mA

3. Transistor Drive (ZN414Z and ZN415E)

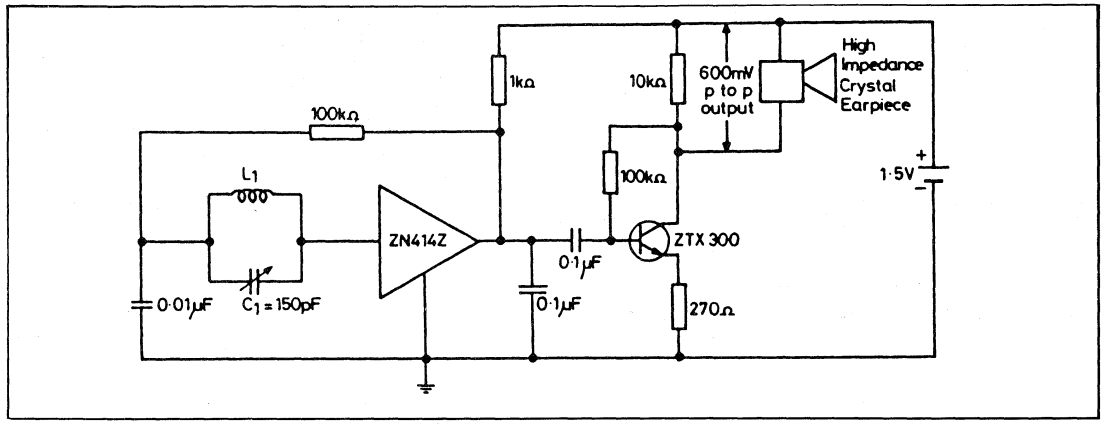


Current consumption is virtually that which is taken by the ZN414Z (0.3mA) or the ZN415E (2.3mA).
Component values shown in brackets are for the ZN415E.

RECOMMENDED CIRCUITS

(a) Earphone radio

The ZN414Z will drive a sensitive earpiece directly. In this case, an earpiece of equivalent impedance to R_{AGC} is substituted for R_{AGC} in the basic tuner circuit. Unfortunately, the cost of a sensitive earpiece is high, and unless an ultra-miniature radio is wanted, it is considerably cheaper to use a low cost crystal earpiece and add a single gain stage. One further advantage of this technique is that provision for a volume control can be made. A suitable circuit is shown below.

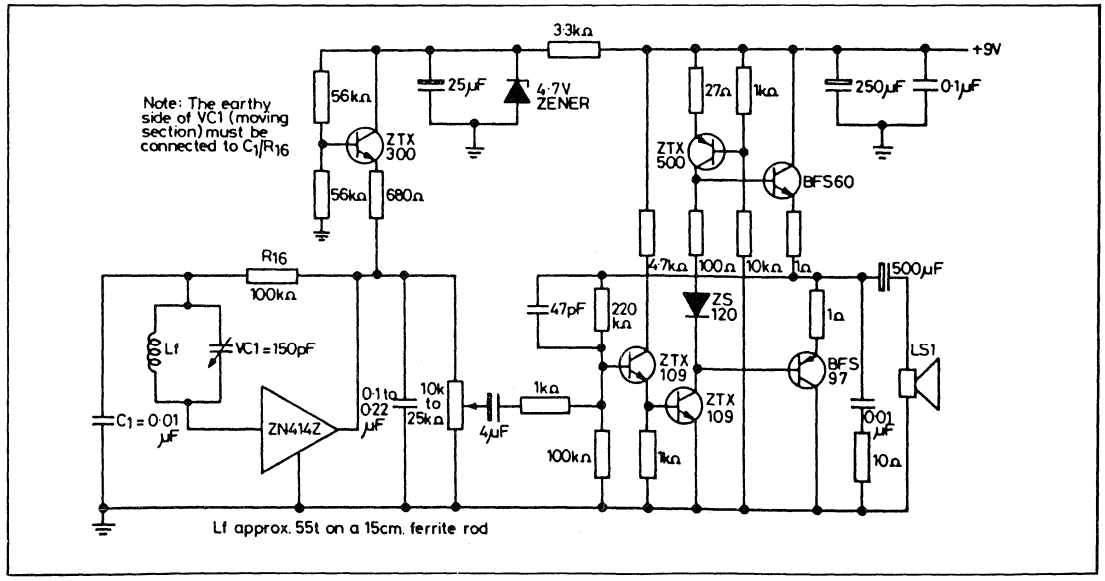


$L_1 \approx 80$ turns of 0.3mm dia. enamelled copper wire on a 5cm or 7.5cm long ferrite rod. Do not expect to adhere rigidly to the coil-capacitor details given. Any value of L_1 and C_1 which will give a high 'Q' at the desired frequency may be used.

Volume Control: a 250Ω potentiometer in series with a 100Ω fixed resistor substituted for the 270Ω emitter resistor provides an effective volume control.

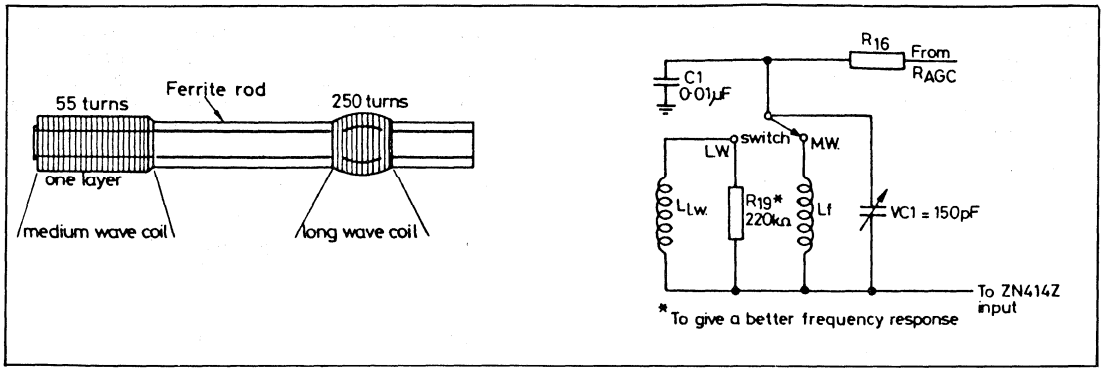
(b) Domestic portable receiver

The circuit shown is capable of excellent quality, and its cost relative to conventional designs is much lower.



The complete circuit diagram of the Triffid receiver

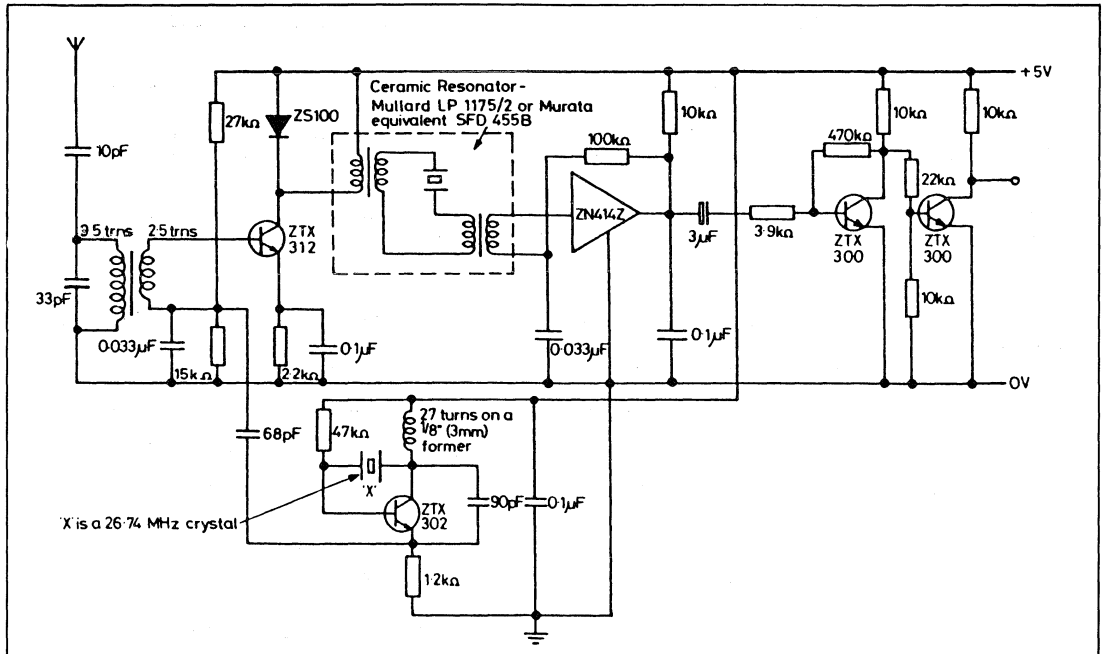
(b)i



Coil winding details and waveband selection

(c) Use in model control receiver

The circuit below shows a ZN414Z used as an I.F. amplifier for a 27MHz superhet receiver.



Performance Details:

Sensitivity = 2.5µV for a 5V p.t.p. output measured at f_C = 27.21MHz, 100% modulated with 100Hz square wave.

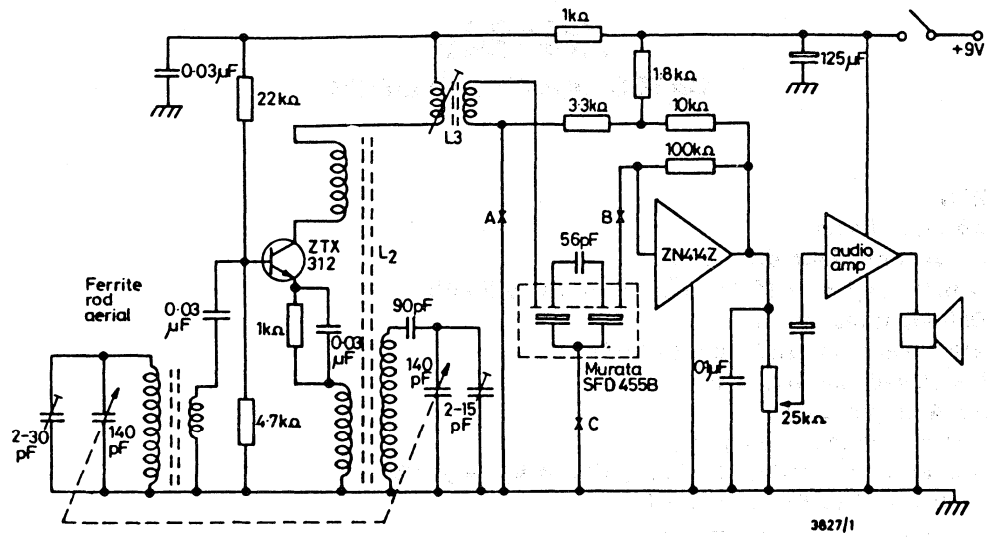
Selectivity: ±5kHz for <100mV p.t.p. output.

Input Signal Range: 2.5µV to 25mV (i.e. 80dB)

Supply Current: ≈4.5mA.

(d) Broadcast band superhet using ZN414Z

The ZN414Z coupled with the modern ceramic resonators offers a very good I.F. amplifier at modest cost, whilst maintaining simplicity and minimal alignment requirements. A typical circuit is shown below:



– 6dB Bandwidth = 6kHz
– 30dB Bandwidth = 8kHz
AGC Range ≈ 40dB
(For 10dB change in A.F. output).

FURTHER APPLICATIONS

The ZN414Z is an extremely versatile device and, in a data sheet, it is not possible to show all its varied applications. A comprehensive applications note on the device is available which gives full details of various radio receivers, I.F. amplifiers and frequency standards together with comprehensive technical information.

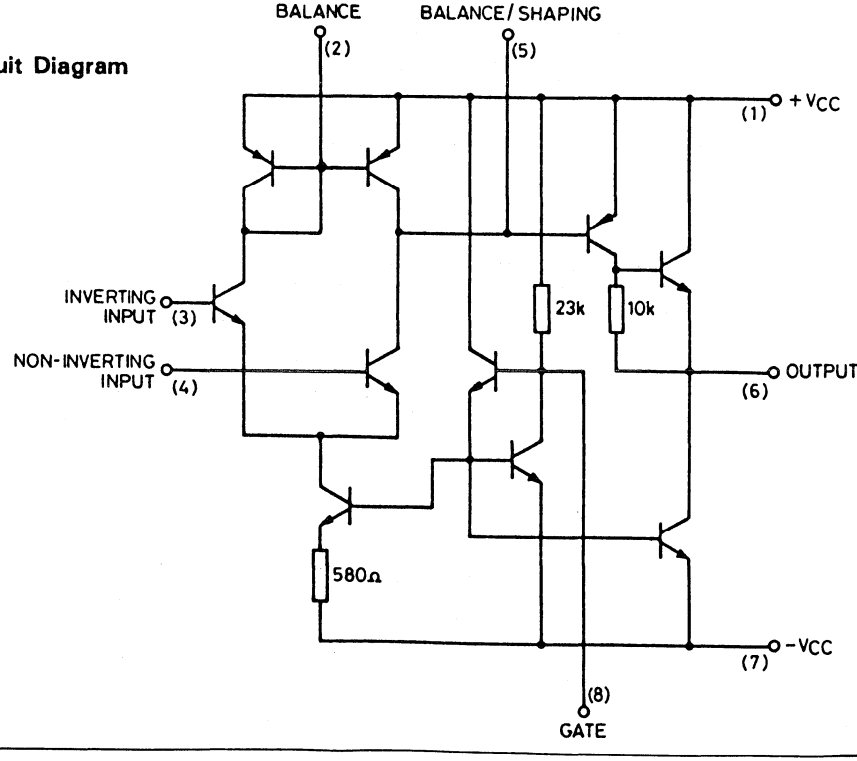
ZN424P

GATED LINEAR AMPLIFIER

FEATURES

- 86dB typical gain
- Very low open loop distortion
- Low noise ($e_n^2 = 4 \times 10^{-17}$ V²/Hz; 100Hz to 20kHz)
- 200kΩ input resistance
- 20kHz open loop bandwidth (−3dB)
- 0.1μs closed loop rise time
- Class A output stage
- 100V/μs slew rate (rising edge)
- Maximum output swing ±11V, ±17V at $V_{CC} = \pm 18$V
- Operation at 5V, TTL compatible
- Logic gate current drive capability
- Input-output isolation gating facility

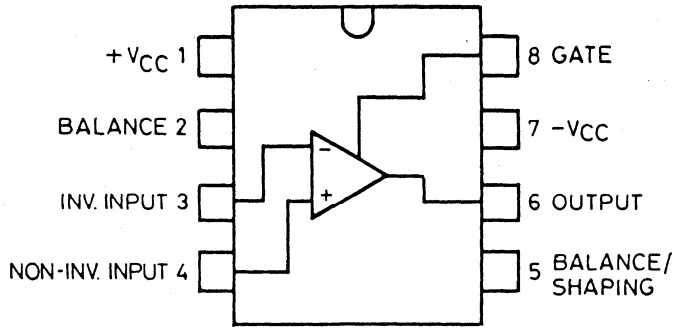
Circuit Diagram



GENERAL DESCRIPTION

The ZN424P is a versatile linear amplifier designed to satisfy the growing requirement for high quality signal processing. As a voltage amplifier the very low distortion and low noise performance makes the device ideally suited for audio applications. The gating facility, coupled with the ability to operate from a TTL supply, gives the device broad appeal in the instrumentation, computing and allied fields. The device is readily stabilised using an external capacitor, or capacitor/resistor combination.

PIN CONFIGURATIONS



ZN424P
(8 lead Moulded Dual in-line)
Viewed from top

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	250mW
Differential Input Voltage	5V
Storage Temperature Range	−65 to +125°C

RECOMMENDED RATINGS

Supply Voltage Range	±2 to ±18V
Operating Temperature Range	0 to +70°C

ELECTRICAL CHARACTERISTICS

($V_S = \pm 12V$, Load = 20kΩ, $T_{amb} = 25°C$ unless otherwise specified).

Parameter	Min.	Typ.	Max.	Units
Input offset voltage		2	6	mV
Input current		0.5	1.2	μA
Input offset current		0.1	0.5	μA
Input offset voltage drift		5		μV/°C
Input current drift		2.0		nA/°C
Input offset current drift		0.4		nA/°C
Input resistance		200		kΩ
Output resistance		4		kΩ
Voltage gain	10,000	20,000		
Mutual conductance		5		A/V
Common mode range	±10	±11		V
Output voltage swing	±10	±11		V
Maximum negative output current (load = 1kΩ)		3.0		mA
Supply current		5.5	7.0	mA
Open loop bandwidth (−3dB)		20		kHz
Unity gain bandwidth (−3dB) (See Note 2)		1		MHz
Common mode rejection ratio	70	100		dB
Supply rejection ratio	80	85		dB
Unity gain rise time(slew rate 1.5V/μs, see Note 2)		0.35		μs
Unity gain overshoot (see Note 2)		10		%
Output leakage current (gated off)		5	30	nA
Voltage gain $V_S = \pm 2.5V$, 3.3kΩ between gating input and $+V_{CC}$, load = 10kΩ	5,000	12,000		
Slew rising edge		100		V/μs
Slew rate falling edge		12		V/μs
Open loop distortion (2V ptp swing)		<1.5		%T.H.D.
Open loop distortion (10V ptp swing)		6		%T.H.D.

OPERATING NOTES

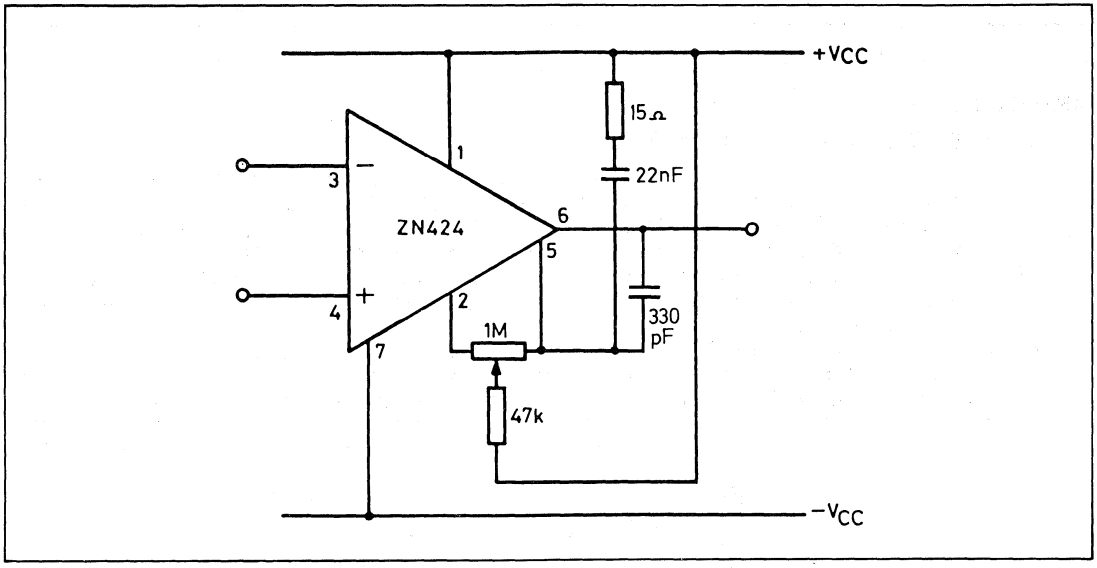
1. When operating with low supply voltages the output bias current may be maintained at about 3mA by connecting an external resistor between the gating input and $+V_{CC}$. Under these conditions the output current is given approximately by:

$$I_C = \frac{(V_{CC} - 1.4) \times 3}{R}$$

R is the parallel combination of the external and internal (23kΩ) resistors.

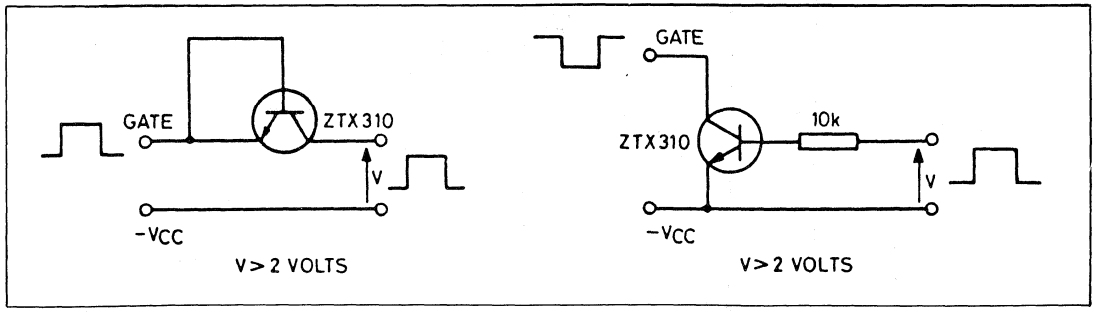
2. Unity frequency stability is achieved by connecting a 22nF capacitor and a 15 ohm resistor in series between 'shaping' and +Vcc, and 330pF between 'shaping' and output.

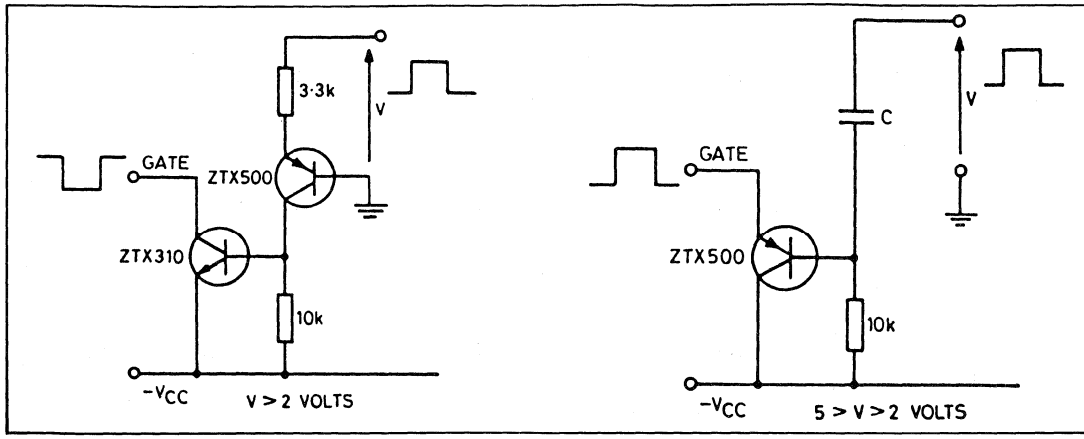
3. Input offset voltage is nullified by connecting a 1MΩ potentiometer between 'balance' and 'balance/shaping' with the wiper connected through a 47kΩ resistor to $+V_{CC}$.



Offset and Frequency Compensation Circuit

4. The ZN424P is gated 'off' by shunting the current source bias current to the negative rail. Four methods of gating the ZN424P are illustrated below, two of which require a drive voltage with respect to the negative rail (e.g. from another ZN424P or from logic, when using a single supply), and the other two allowing the drive pulse to be with respect to earth or another convenient point.



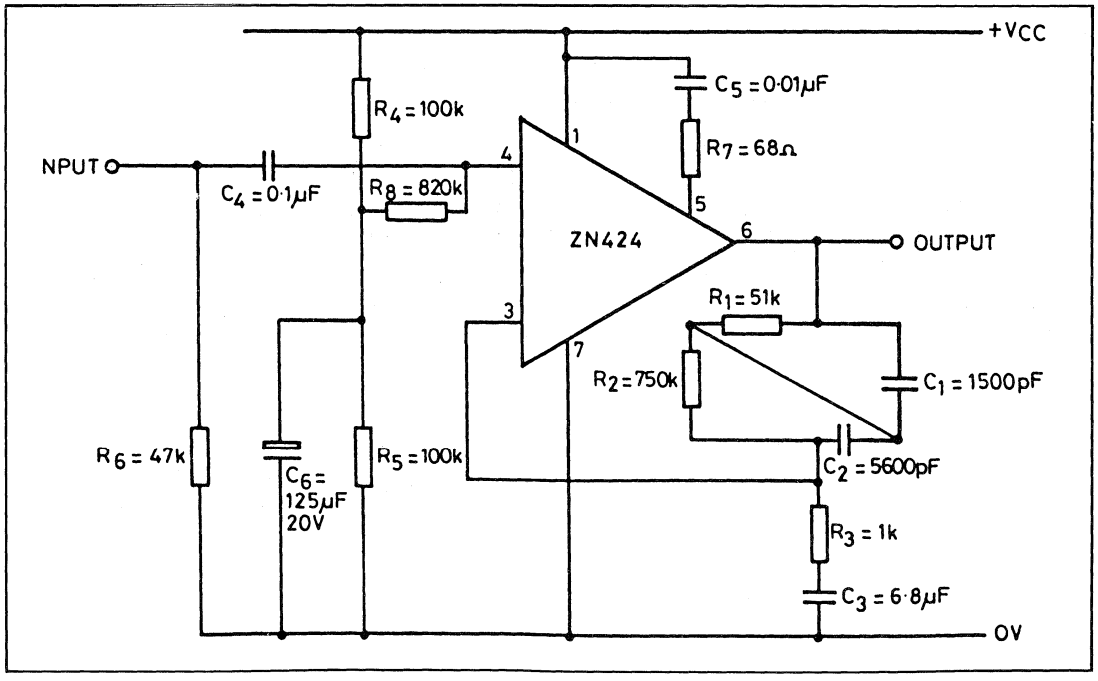


5. When gated off, the input-output coupling is representable by a 1pF capacitor.

APPLICATIONS

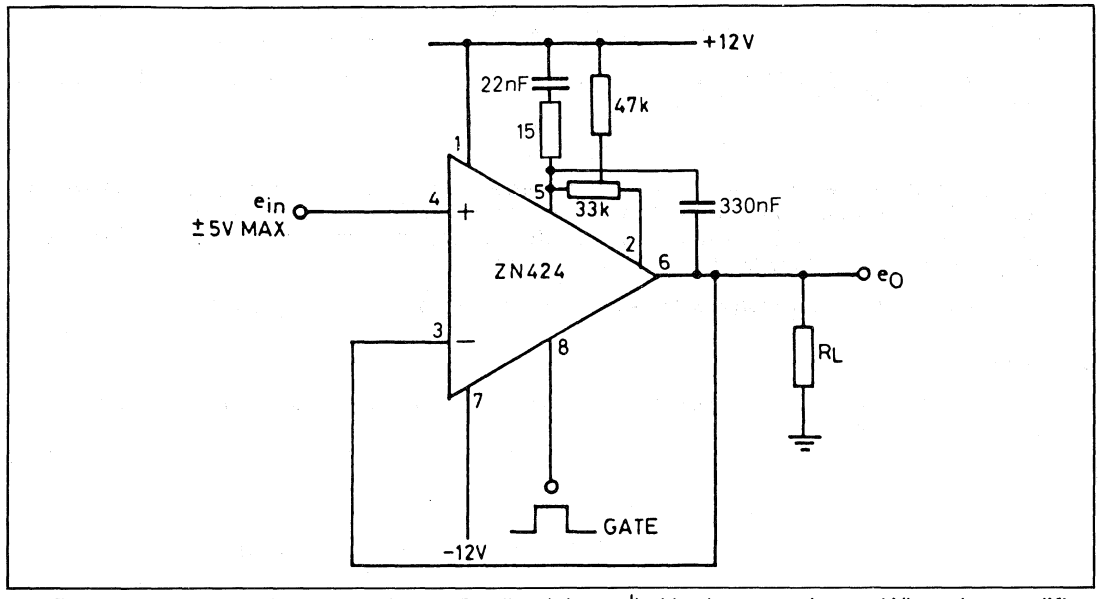
1. Magnetic Cartridge (R.I.A.A.) Preamplifier:

The open loop gain of the ZN424P is 20,000 (86dB) and the open loop distortion is typically, 1.5% corresponding to a 2 volt peak output swing (this is the maximum output ever likely to be encountered from a magnetic cartridge). To feed most power amplifiers a voltage gain, at 1kHz, of 50 (34dB) is necessary between cartridge and amplifier. Thus by applying 52dB of feedback (86dB to 34dB) the distortion figure at 1kHz becomes 0.004%. If more gain is required R_3 may be made smaller but C_3 must be increased proportionaly to avoid loss of bias. C_1, C_2, R_1, R_2 provide R.I.A.A. equlisation and, in addition, C_3 and R_3 provide an effective rumble filter. C_5 and R_7 provide stability for all supply voltages. Assuming a 30 volts supply the overload factor of the circuit is $\simeq$ 40dB referred to a 5mV input. The signal to noise ratio is better than 70dB below a 5mV input. The layout of the circuits is unimportant.



Magnetic Cartridge Preamplifier Circuit

2(a) X1 Non-Inverting Amplifier:

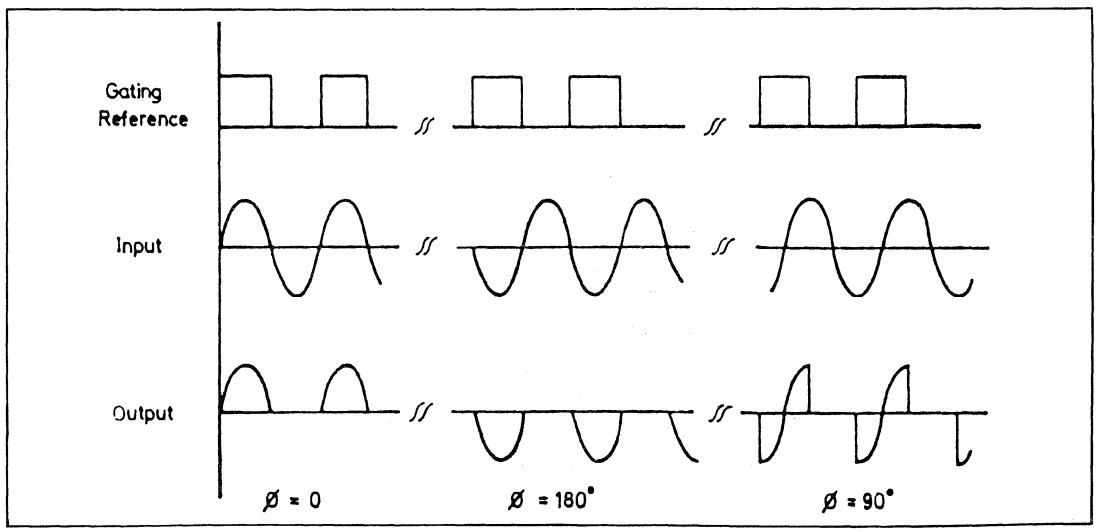


The circuit diagram is shown above. Feedback is applied in the normal way. When the amplifier is gated 'off' the input and output become open circuited as long as the maximum differential input voltage is not exceeded. This limits the input voltage range to ± 5V. This may be effectively increased by attenuating the input suitably and defining the gain of the amplifier to give an overall gain of unity. In order to obtain an overall gain of unity an attenuator comprising of $R_F = 47k\Omega$ and $R_S = 10k\Omega$ is required.

This method has the disadvantages of requiring four accurate resistors, giving a higher output offset voltage (unless an offset control is used) and lower input resistance (57kΩ). However, the settling time is reduced (see Table 1) since lower values of shaping capacitor can be used.

By applying a square wave to the gating point, an output may be obtained which is an amplified square wave modulated version of the input.

2(b) Rectification/Demodulation (no transformers ncessary):



The previous circuit may be used as a half-wave sensitive detector by applying a square wave reference voltage to the gating point and a phase related signal to the input. Typical waveforms are illustrated below for phase differences (ϕ) of 0, 90 and 180 degrees.

The mean d.c. output level is proportional to R cosϕ, where R is the input amplitude. For a half-wave detector with a gain of A:

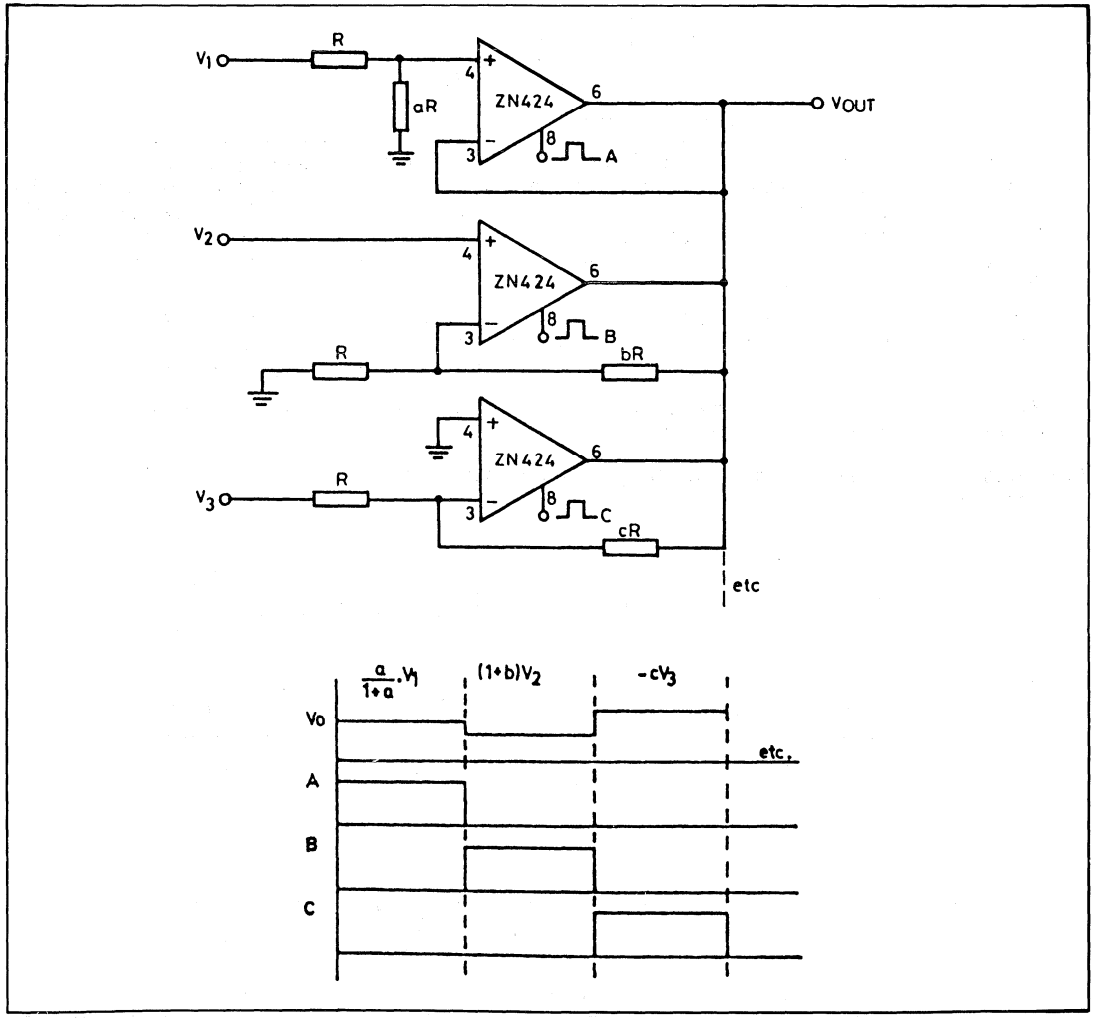
$$\overline{e_O} = \frac{AR}{\pi} \cos\phi$$

Using two phase sensitive detectors driven from square wave reference voltages 90 degrees out of phase, outputs proportional to Rcosϕ and Rsinϕ may be obtained. If these voltages are applied to the X and Y plates of a cathode ray tube the spot will describe the polar plot (R,ϕ). Nyquist plots may thus be obtained directly.

The square wave reference voltages may be generated using a ring counter.

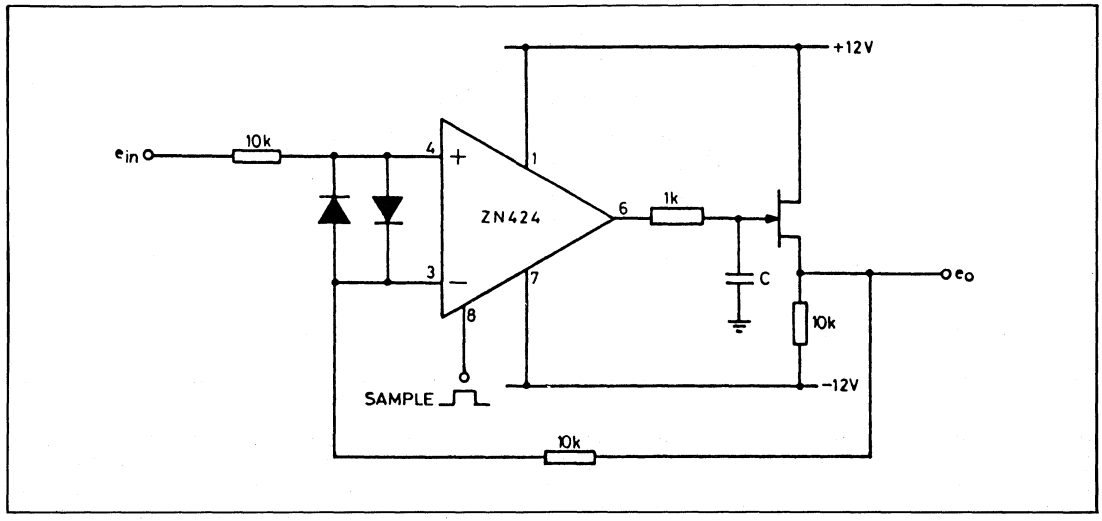
3. Multiplexing:

A ring counter is used to provide a gating pulse to enable the ZN424P to give a multiplexed output as shown below.



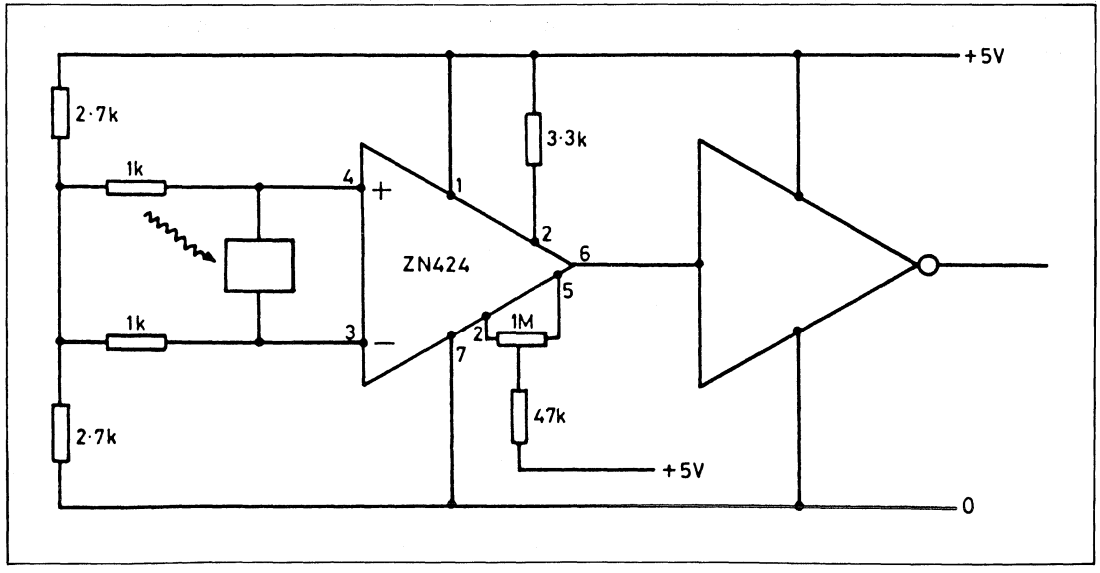
4. Sample and Hold Circuits:

A typical circuit is shown below. The output voltage, e_O, is determined by the choice of feedback resistor when the ZN424P is gated 'on'. When gated 'off', e_O is held for a time which is dependent on 'C', the leakage of the FET and the ZN424P. The value of the capacitor also determines the sampling time necessary. Integrator/Reset circuits can readily be derived from this type of circuit.



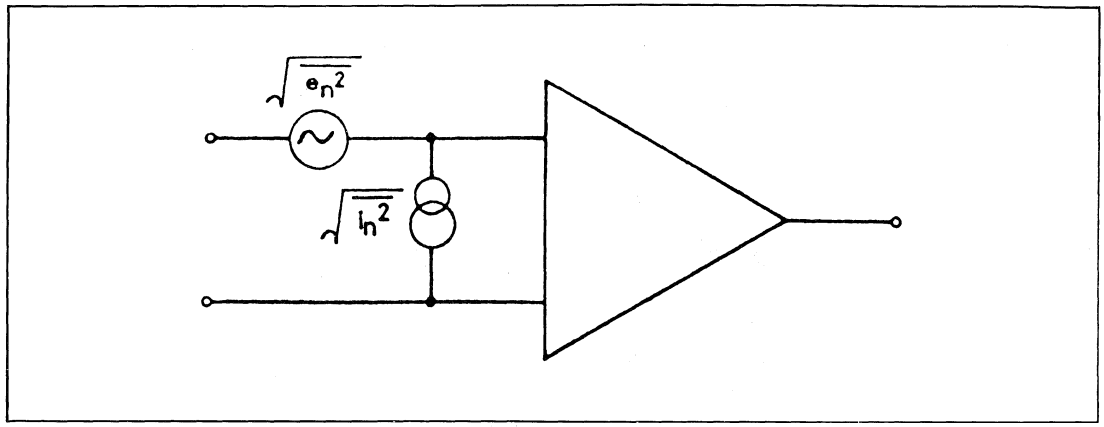
5. Photocell Trigger Circuit Driving TTL Gate(s):

A typical circuit is shown below. The input is biased, so the output is low, when the photocell is irradiated. With no output from the photocell the output is high. The photocell used below gave an output of 60mV, 30μA when irradiated. In this type of circuit the gating facility can be used to switch various combinations of photoelectic, encoder/decoder circuitry.



NOISE

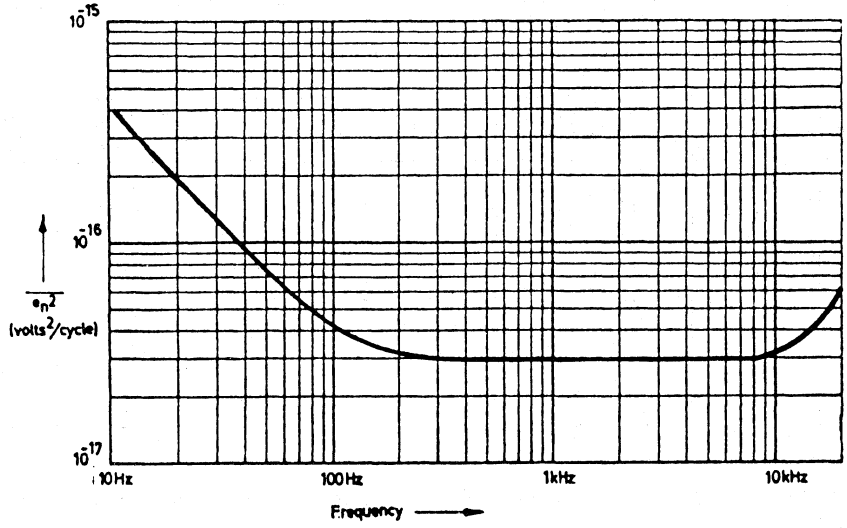
An amplifier always generates noise. At low frequencies flicker noise predominates and increases inversely with the frequency (though presumably not indefinitely). At a sufficiently high frequency this source of noise becomes insignificant compared with shot noise. This is white noise, i.e., has a constant energy/cycle.

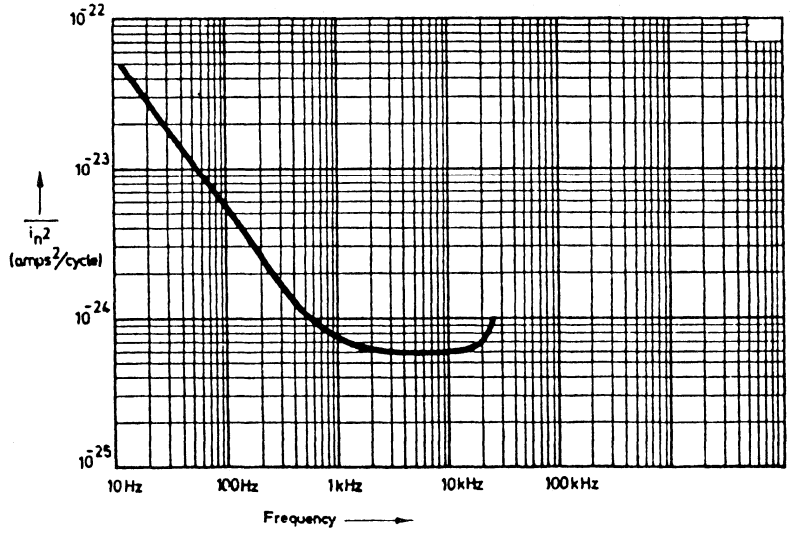


Any amplifier may be represented by an ideal amplifier with equivalent noise voltage and current generators at the input as shown above. The mean square noise voltage is shown as $\overline{e_n^2}$ volts^2/cycle and the mean square noise current as $\overline{i_n^2}$ amps^2/cycle. The noise voltage may be measured by short-circuiting the inputs so that no noise current flows into the amplifier. When the input terminals are open-circuited all the noise current flows into the amplifier and the noise voltage generator is open-circuited. The noise that appears at the output of the amplifier will obviously depend upon the shape of the frequency response. If the frequency response is measured the noise measured at the output may be referred back to the input. This is shown below where $\overline{e_n^2}$ and $\overline{i_n^2}$ are plotted against frequency. In an actual case, a source resistance R_S will be connected across the input terminals.

This resistance will itself generate white noise known as Johnson noise of magnitude $\overline{e_r^2} = 4kTR_S$ volts^2/cycle, where k is the Boltzmann constant and T is the absolute temperature. The noise current flowing in this resistance will also produce a mean square noise voltage of $\overline{i_n^2}\ R_S^2$volts^2/cycle.

TYPICAL CHARACTERISTICS





Graph 1. $\overline{e_n^2}$ and $\overline{i_n^2}$ against frequency for ZN424P

Stabilising the ZN424P in Various Gain Configurations

The ZN424P is designed such that any resistive feedback circuit can be stabilised with less than 50 per cent overshoot using $C_1 = 0.1\mu F$. For better than 10 per cent overshoot, the values given in the following table are suitable.

TABLE 1

Closed loop gain	R_F (kΩ)	C_F (pF)	R_1 (Ω)	C_1 (nF)	C_2 (pF)	Rise Time (μs)	Slew Rate (V/μs)
⩾ 250	10	-	-	-	-	0.35	45
100	10	10	68	4.7	-	0.65	12
50	10	10	68	4.7	3.3	0.55	10
20	10	10	68	4.7	7.5	0.4	8
10	10	10	68	4.7	15	0.35	5
5	10	10	68	4.7	33	0.3	3
2	10	10	68	4.7	68	0.22	1.7
1	0	-	15	22	330	0.33	1.5

The rise times and slew rates are given as a guide when the supply current is maintained at about 5mA (see Operating Note 1).

R_1 and C_1 are connected in series between pins 5 and 1; C_2 is connected between pins 5 and 6.

For other values of R_F it may be necessary to change C_F for optimum response.

ZN402 Gated Op Amp (Obsolete)

The ZN402 is electrically similar to the ZN424P and the devices are interchangeable. However, because testing procedures are more rigorous for the ZN424P, its performance is better than that of the ZN402; the ZN424P is therefore recommended for all new designs.

PLESSEY
Semiconductors

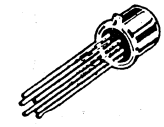
ZN459, ZN459CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

FEATURES

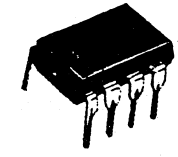
- High Controlled Gain : 60 dB ±1 dB typical
- Low Noise : 40Ω Equivalent Noise Resistance, or 800 pV/$\sqrt{Hz}$
- Wide Bandwidth : 15 MHz typical
- Low Supply Current : <3 mA from 5V

ZN459



CM6

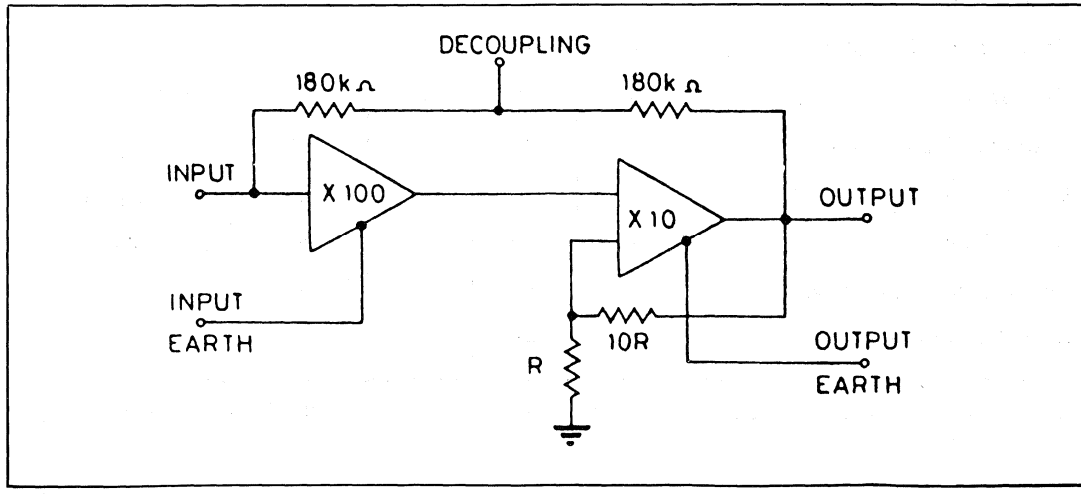
ZN459CP



DP8

DESCRIPTION

A versatile high grade a.c. pre-amplifier designed for applications requiring ultra low noise such as infra-red imaging and low noise wide band amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain coupled with small physical size make the ZN459 series ideal for multichannel amplification.



ZN459 OUTLINE CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6·0 Volts

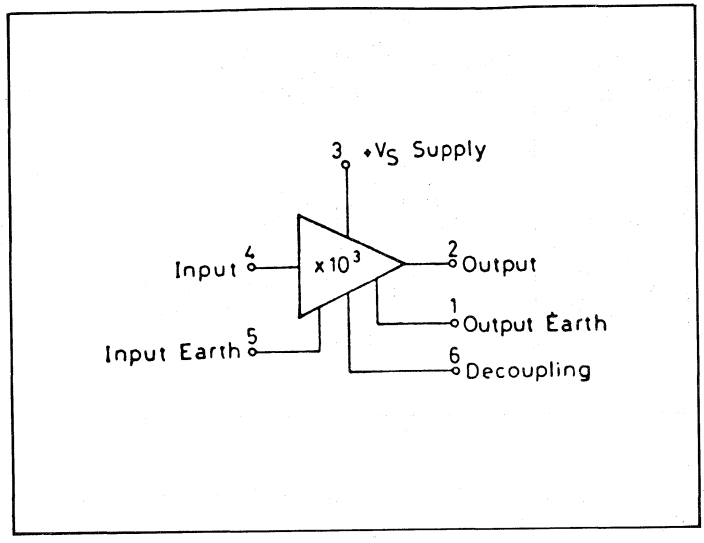
Operating Temperature Range:
for ZN459 .. .. .. −55 to +125°C
for ZN459CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. −55 to +125°C

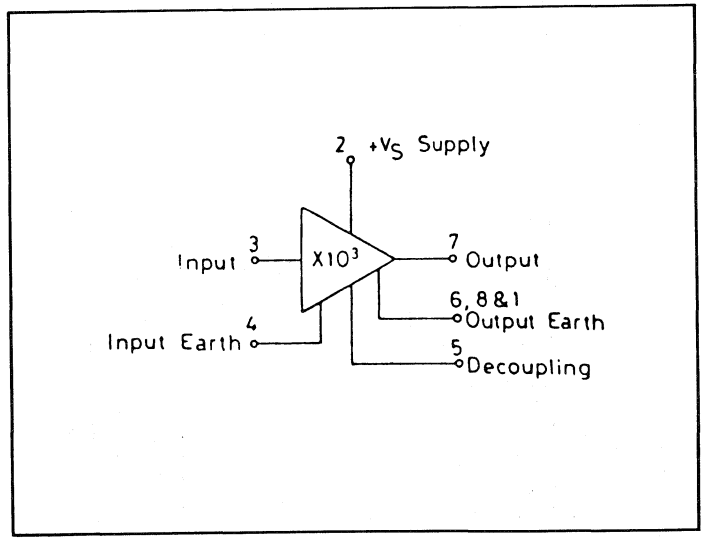
CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2·0	2·5	3·0	mA	
Voltage Gain	59	60	61	dB	10 kHz
TC of Voltage Gain	—	−0·2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	15	—	MHz	3 dB down
Input Resistance	3·5	7	—	kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 1
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3	—	$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1·5	2·0	2·5	V	
Supply Voltage Coefficient of Output Level	—	0·34	—	V/V	
Output Current Limit	0·6	0·8	1·1	mA	Sink current
Total Harmonic Distortion ..	—	0·15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42·5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	10	—	mA	
Negative Input Overdrive ..	—	−5	—	V	

Note 1: In P.C.B. The Input Capacitance may be reduced to 25pF by screening between output and input.

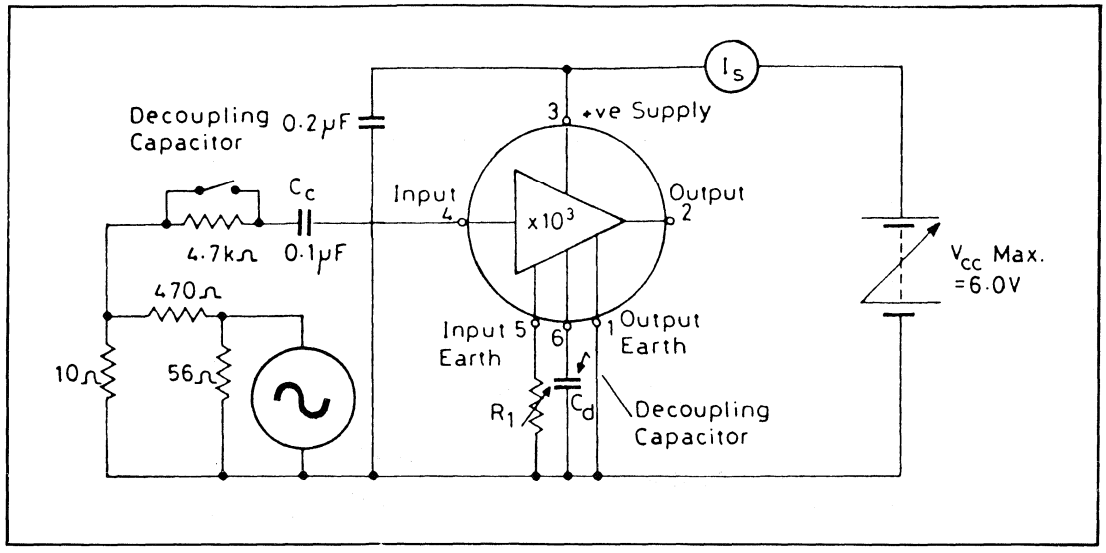


PINNING CONFIGURATION - ZN459



PINNING CONFIGURATION - ZN459CP

GAIN TEST CIRCUIT (ZN459)

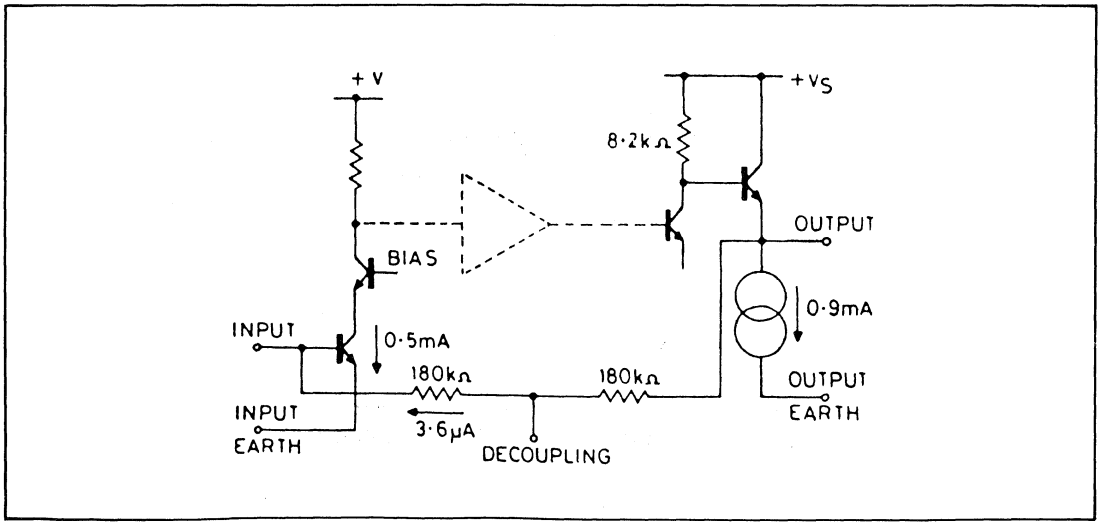


The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_d is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_d \geqslant C_c$.

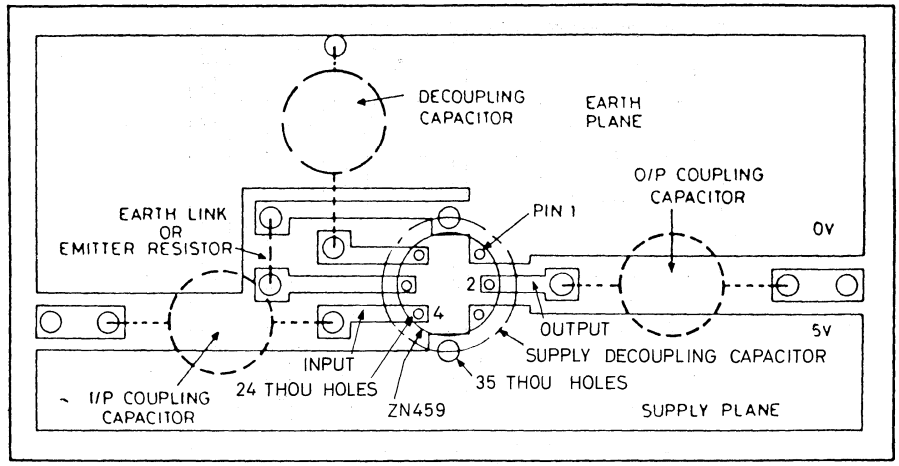
The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

For optimum Common Mode Rejection connect a twisted pair between source and pins 4 and 5 of the device, and complete the earth return from source ground.

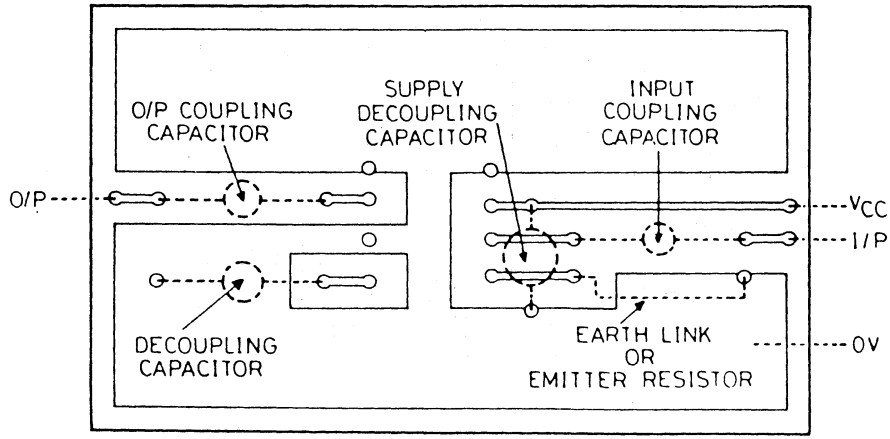


ZN459 INPUT AND OUTPUT CIRCUIT

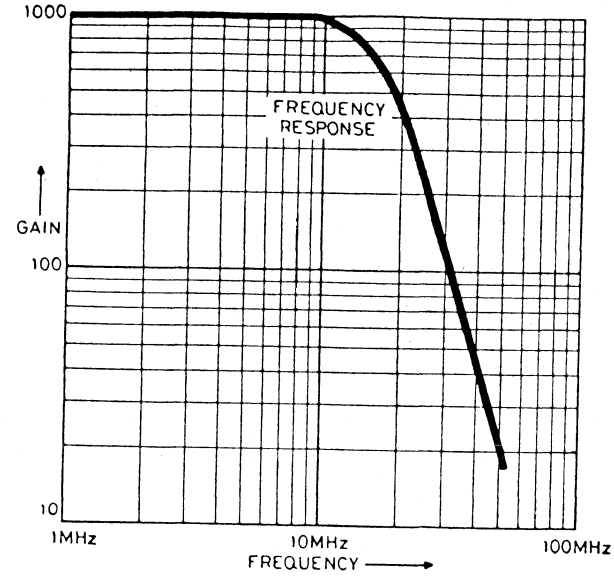
PCB LAYOUT (ZN459)



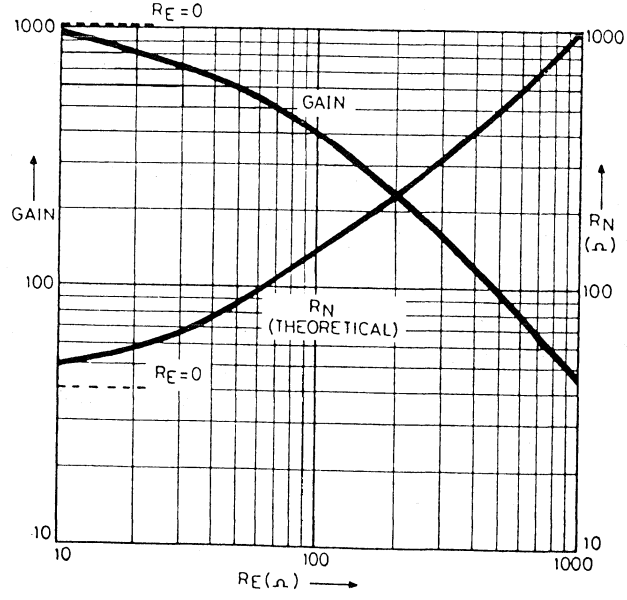
PCB LAYOUT (ZN459CP)



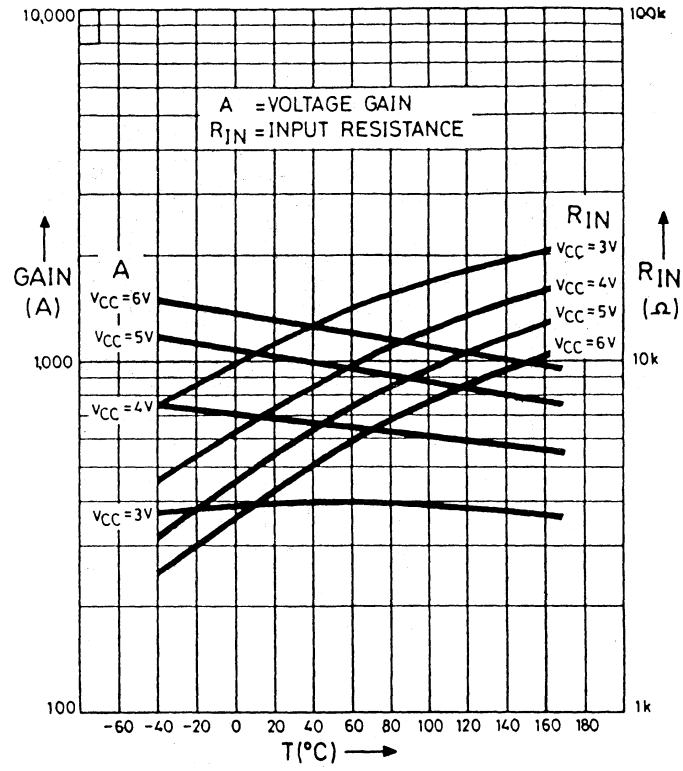
TYPICAL CHARACTERISTICS



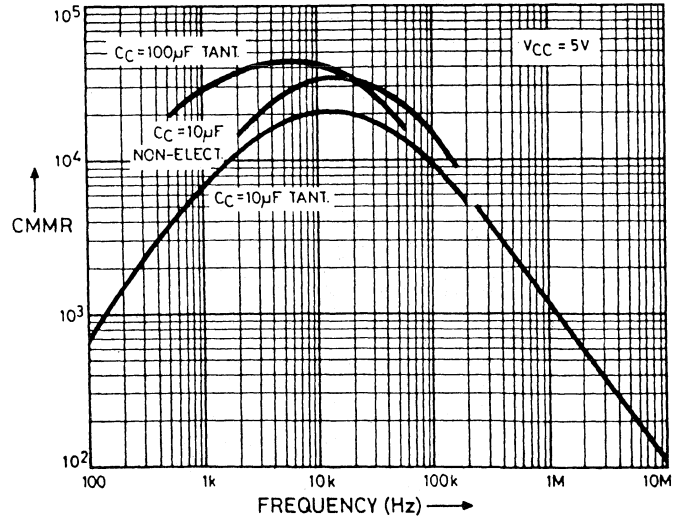
GAIN V_S FREQUENCY



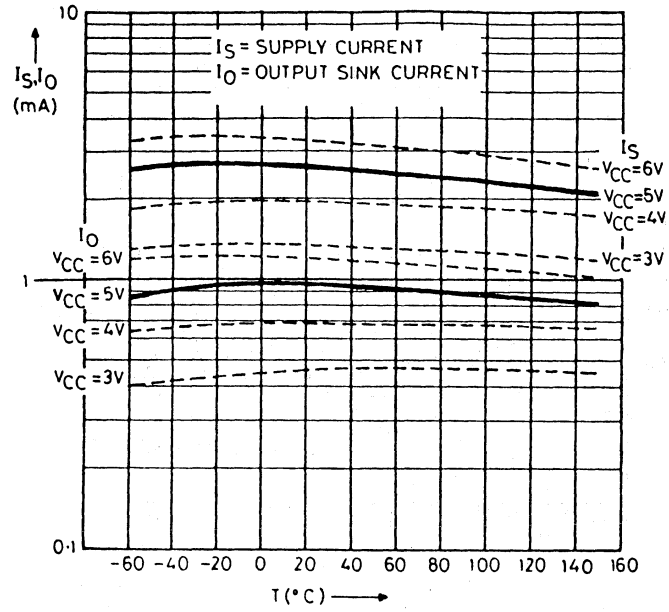
GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE



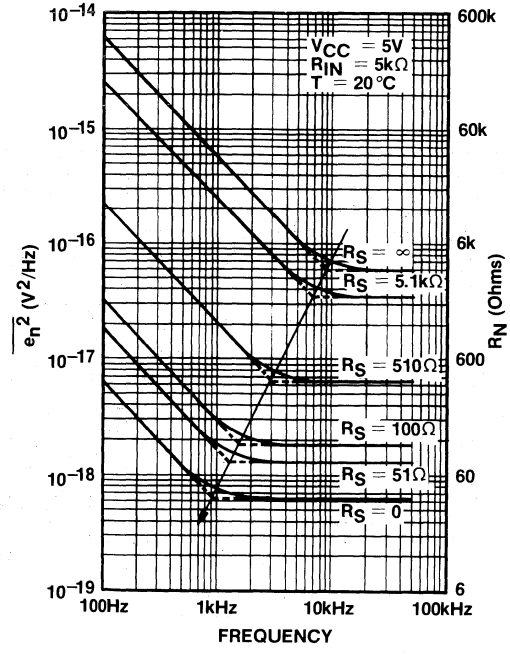
GAIN AND INPUT IMPEDANCE



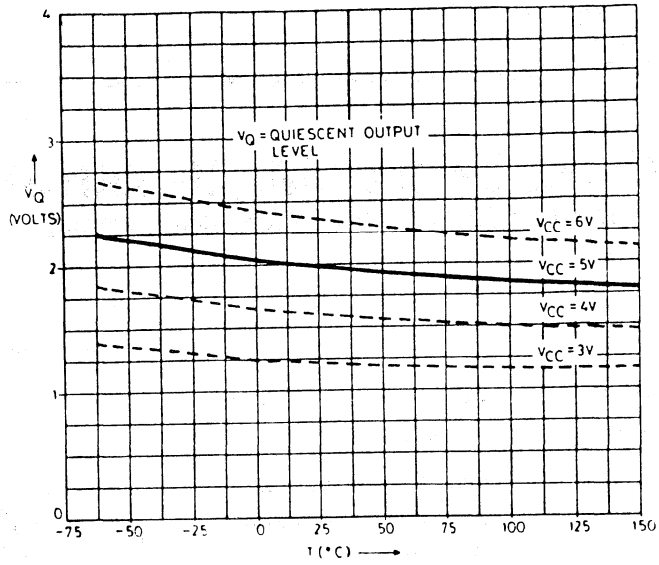
COMMON MODE REJECTION Vs FREQUENCY
(Measured between input earth and output earth)



SUPPLY CURRENT AND OUTPUT SINK CURRENT



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

PLESSEY
Semiconductors

ZN460, ZN460AM, ZN460CP

ULTRA LOW NOISE WIDEBAND PREAMPLIFIER

FEATURES

- **High Controlled Gain** : **60 dB ± 1 dB typical**
- **Programmable Gain** : **50-60 dB typical**
- **Programmable Bandwidth** : **6MHz downwards**
- **Low Noise** : **40Ω Equivalent Noise Resistance, or 800 pV/√Hz**
- **Low Supply Current** : **<3 mA from 5V**

ZN460

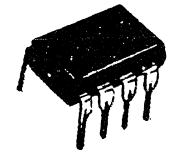
CM8

DESCRIPTION

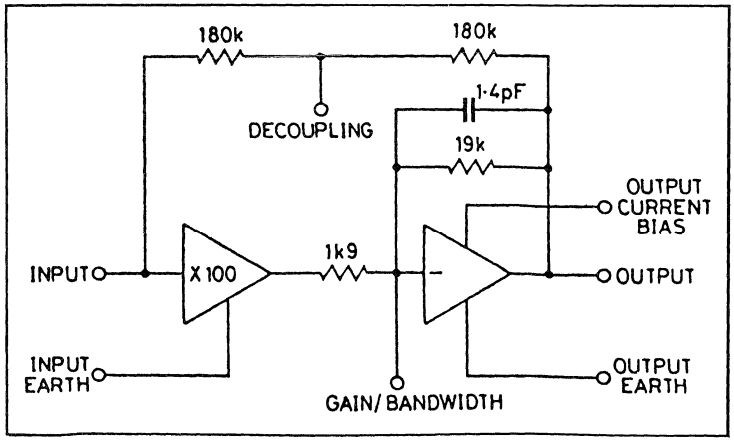
The ZN460 is a versatile high performance AC preamplifier, designed for applications requiring ultra low noise such as infra-red imaging and low noise wideband amplifiers e.g. microphone, acoustic emission, transducer bridge amplifier. The matching of open loop gain, coupled with small physical size, makes the ZN460 ideal for multichannel amplification.

The programmable gain feature allows variable detector gain factors to be trimmed out. The programmable bandwidth feature allows the noise bandwidth to be reduced to the required signal bandwidth, thus minimising the wideband output noise.

ZN460CP

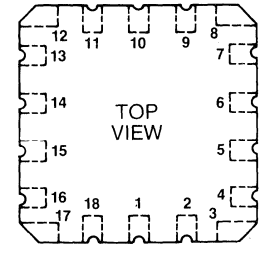


DP8



CIRCUIT DIAGRAM

ZN460AM



AM18

ABSOLUTE MAXIMUM RATINGS

Supply Voltage .. .. 6.0 Volts

Operating Temperature Range:
for ZN460 and ZN460AM .. .. .. −55 to +125°C
for ZN460CP .. .. .. 0 to +70 °C

Storage Temperature Range .. .. .. −55 to +125°C

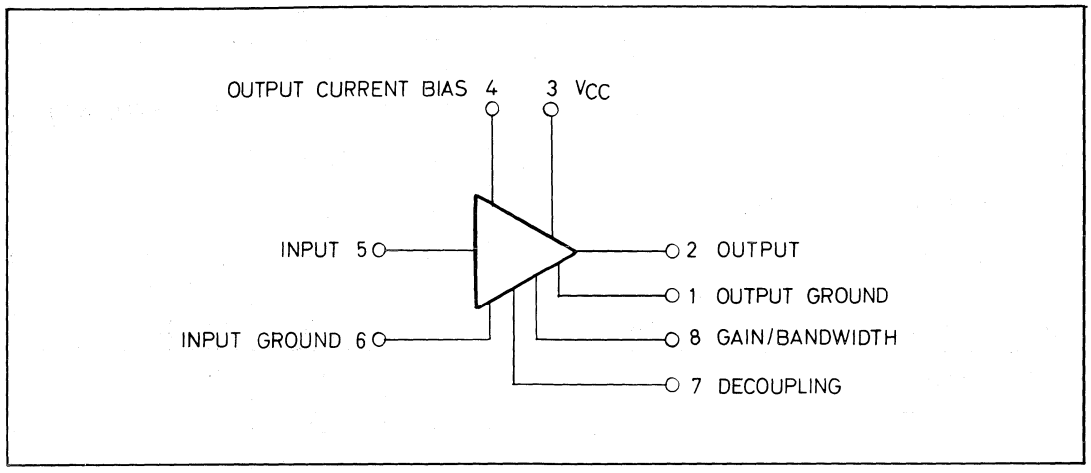
CHARACTERISTICS (at V_{CC} = 5V, T_{amb} = 25°C).

Parameter	Min.	Typ.	Max.	Units	Conditions
Supply Current	2.0	2.5	3.0	mA	
Voltage Gain	59	60	61	dB	10 kHz (Note 1)
TC of Voltage Gain	—	−0.2	—	%/°C	
V_{CC} Coefficient of Voltage Gain	—	25	—	%/V	
Cut-off Frequency	—	6	—	MHz	3 dB down (Note 1)
Input Resistance	3.5	7		kΩ	10 kHz
Input Capacitance	—	80	—	pF	Note 2
Noise Resistance	—	40	—	Ω	$R_S = 0$
White Noise Voltage	—	800	1100	$pV/\sqrt{Hz}$	$R_S = 0$
L.F. Spot Noise	—	3		$nV/\sqrt{Hz}$	$R_S = 0$, f = 25 Hz
White Noise Current	—	1	—	$pA/\sqrt{Hz}$	
Output Level	1.5	2.0	2.5	V	
Output Swing	2	4 —		V_{pp} V_{pp}	$R_F = \infty$ R_F = 6 kΩ
Supply Voltage Coefficient of Output Level	—	0.34	—	V/V	
Output Current Limit	0.6	0.8	1.1	mA	Note 3
Total Harmonic Distortion ..	—	0.15	—	%	1 V_{pp} at 10 kHz
Output Resistance	—	75	—	Ω	10 kHz
Supply Rejection Ratio ..	—	42.5	—	dB	
Delay Time	—	20	—	ns	Small signal
Delay Time	—	40	—	ns	100 mV rms input
Positive Input Overdrive ..	—	—	10	mA	
Negative Input Overdrive ..	—	—	−5	V	

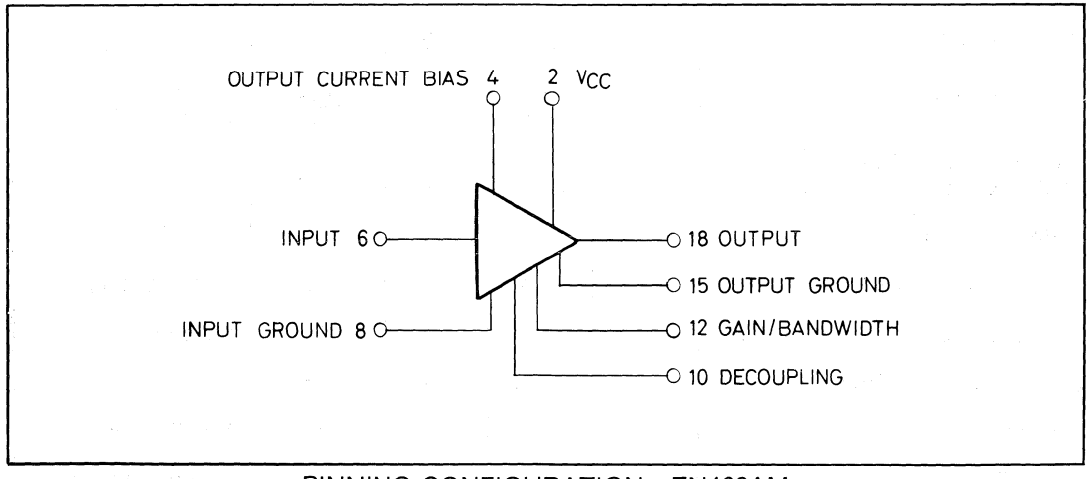
NOTE 1. Without external components.

NOTE 2. In P.C.B. The Input Capacitance may be reduced to 25 pF by screening between output and input

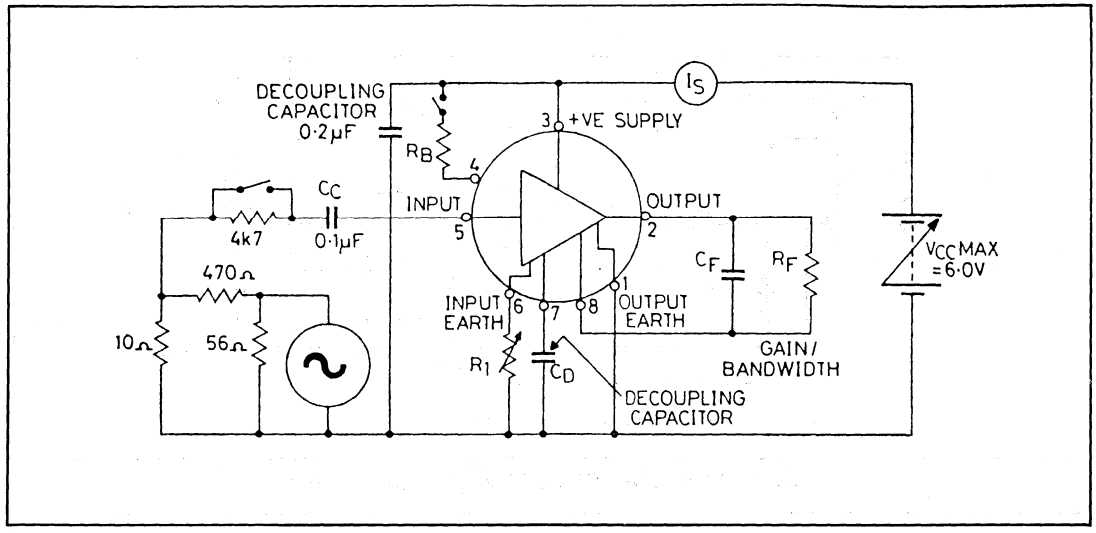
NOTE 3. Sink current without external bias resistor.



PINNING CONFIGURATION - ZN460 and ZN460CP



PINNING CONFIGURATION - ZN460AM



GAIN TEST CIRCUIT (ZN460)

The input impedance may be increased at the expense of noise by including R_1 to vary the gain ($R_1 = 0$, gain $= 10^3$; $R_1 = 470\Omega$, gain $= 10^2$).

C_D is required to decouple the internal feedback loop and in order to obtain a flat frequency response make $C_D \geqslant C_C$.

The earth lead of the supply decoupling capacitor should be as close as possible to that of R_1.

R_B may be used to increase the output quiescent current up to a maximum of 5 mA. The value is given by:

$$I_O = \frac{10(V_{CC} - 1.34)}{R_B'}$$

where R_B' is the parallel combination of R_B and 40 kΩ.

The gain and bandwidth may be modified by means of R_F and C_F. The gain is given by:

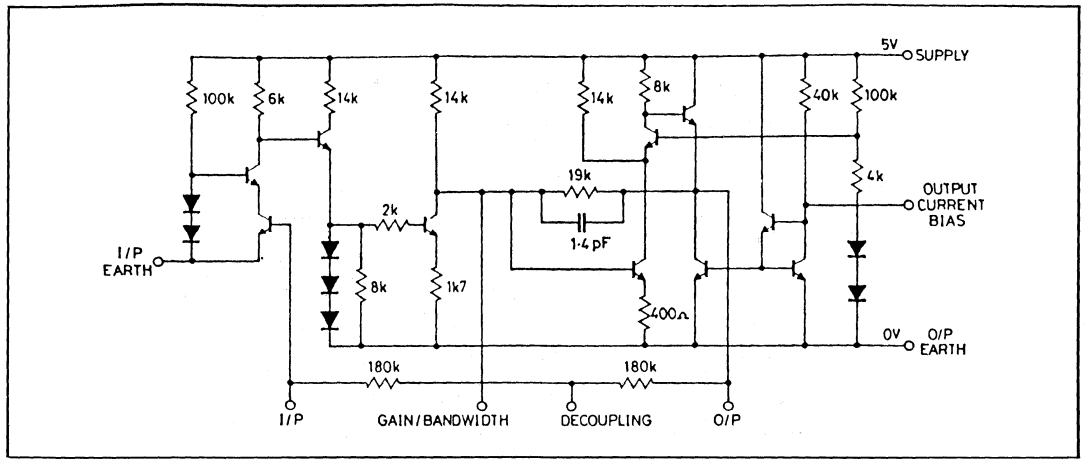
$$A = \frac{10^3 . R_F}{R_F + 19} \text{ with } R_F \text{ in k}\Omega$$

and the bandwidth by:

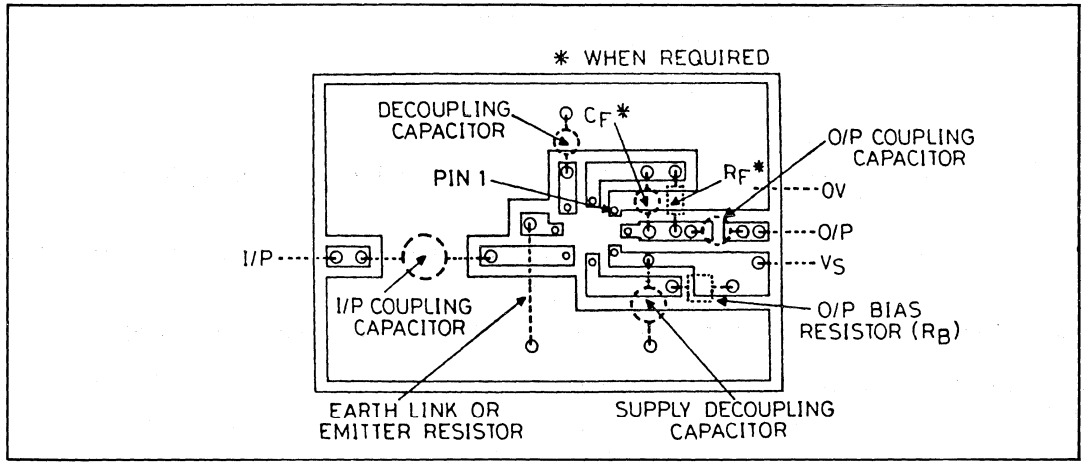
$$f_C = \frac{10^{12}}{2\pi R_F' (C_F + 1.4)} \text{ Hz with } C_F \text{ in pF}$$

where R_F' is the parallel combination of R_F and 19 kΩ.

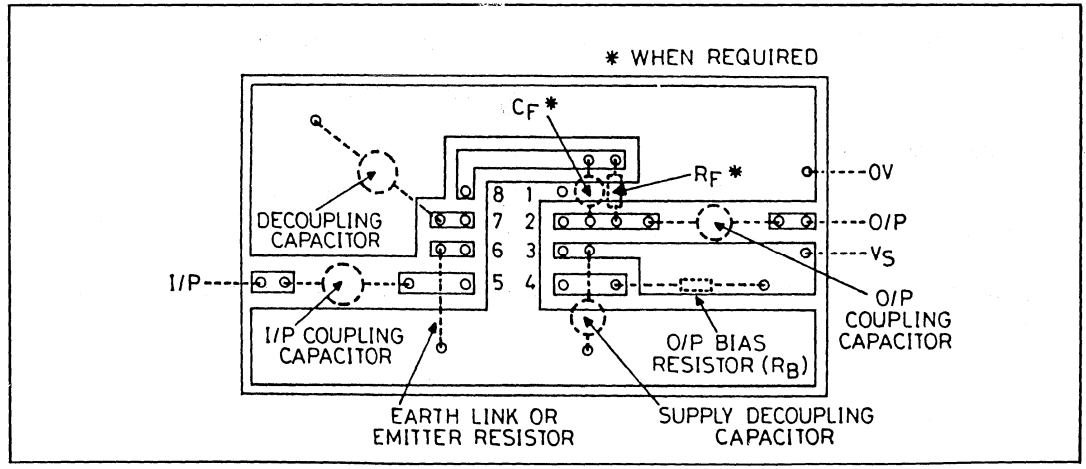
The recommended minimum value of R_F is 6 kΩ since a lesser value reduces the output swing below $2V_{pp}$.



ZN460 CIRCUIT DIAGRAM (Typical Values)

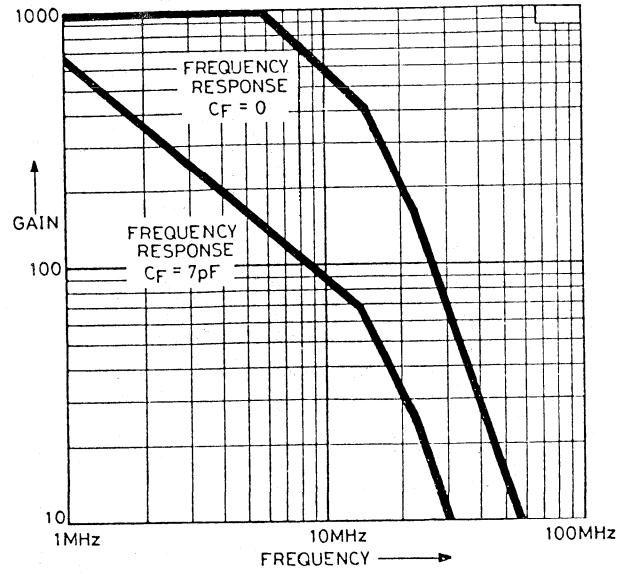


PCB LAYOUT -ZN460

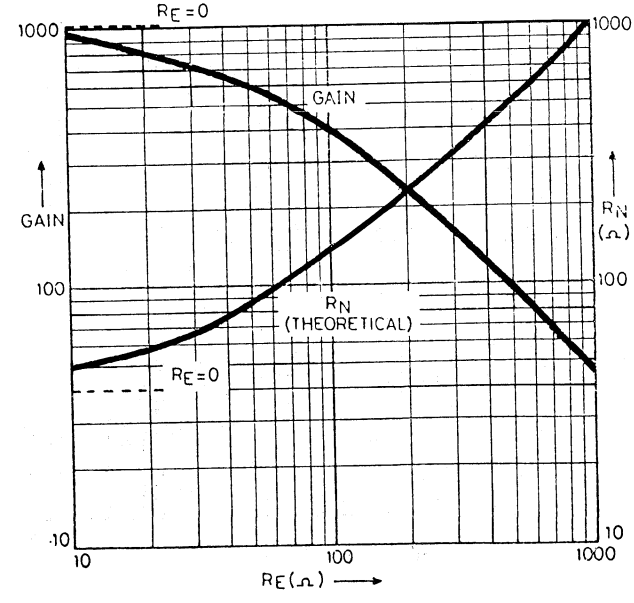


PCB LAYOUT ZN460CP

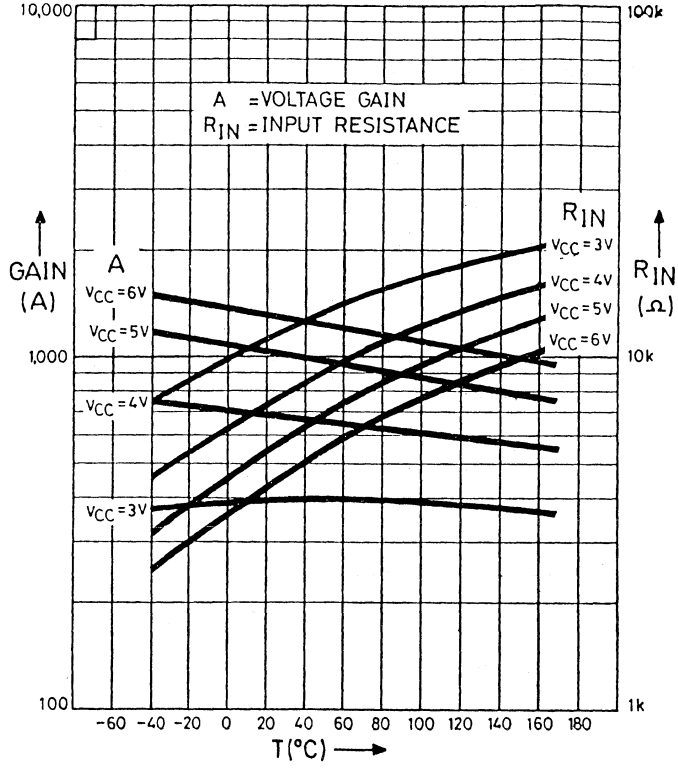
TYPICAL CHARACTERISTICS



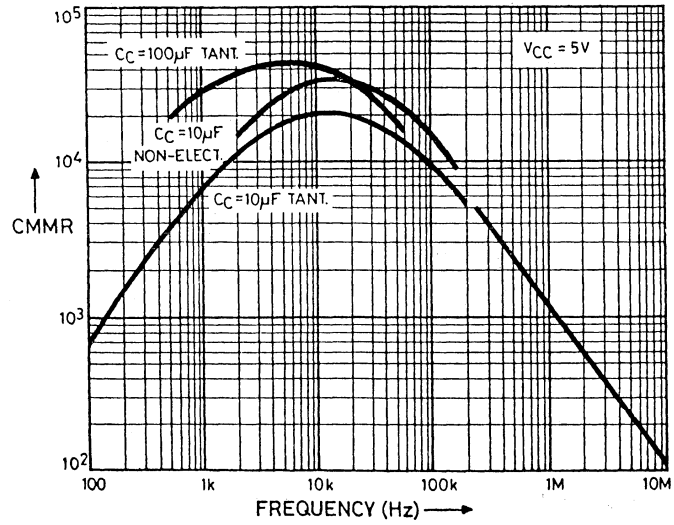
GAIN V_S FREQUENCY ($R_F = \infty$)



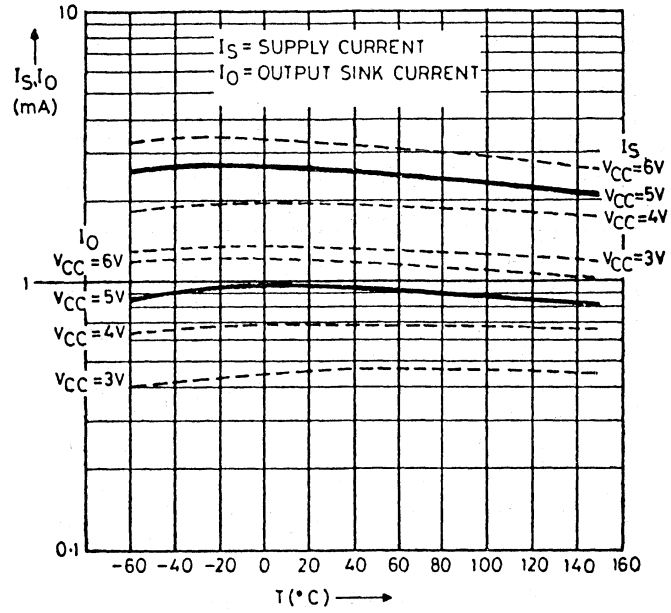
GAIN AND NOISE RESISTANCE V_S EMITTER RESISTANCE ($R_F = \infty$)



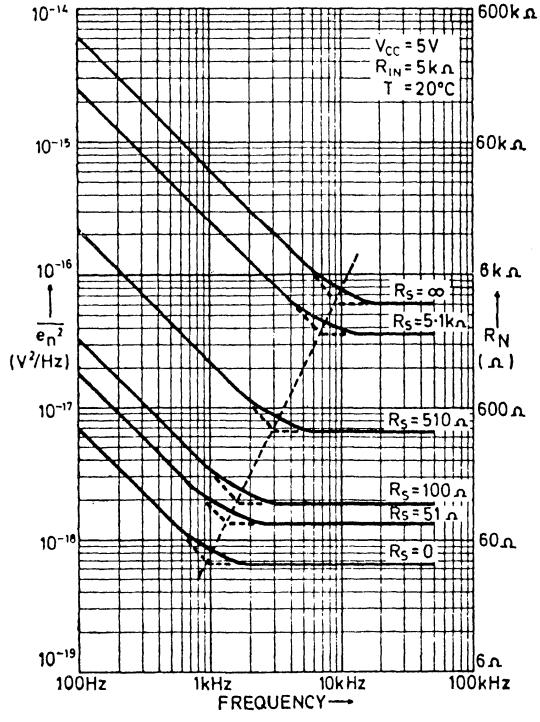
GAIN AND INPUT IMPEDANCE



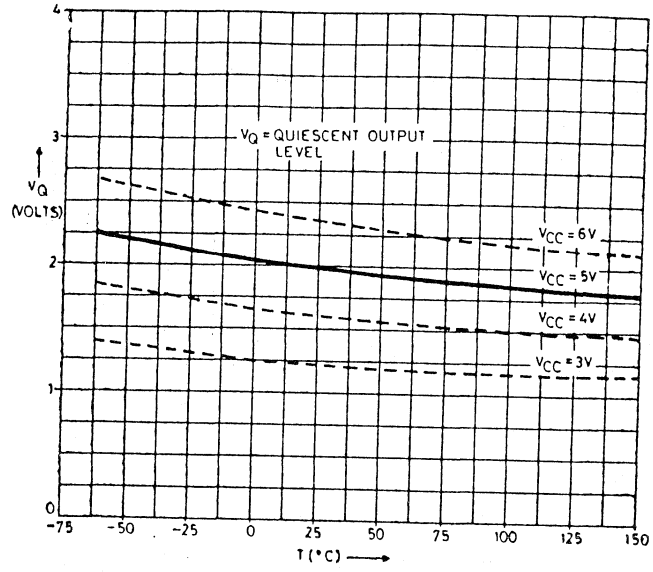
COMMON MODE REJECTION V_S FREQUENCY
(Measured between input earth and output earth)



SUPPLY CURRENT AND OUTPUT SINK CURRENT ($R_B = \infty$)



NOISE VOLTAGE



QUIESCENT OUTPUT LEVEL

Application Notes

Wideband VHF Antenna Booster using the SL560

The following is a brief description of a 40-260MHz antenna amplifier module suitable for any 50Ω VHF system. The module is constructed on a single sided PCB and layout is not critical as long as the usual precautions for VHF construction are observed.

An unusual feature of this module is the use of a transmission line transformer to provide 'noiseless' emitter feedback to the SL560.

The component count is minimal, i.e. 4 resistors, 7 capacitors, 2 inductors, 1 transformer, 1 SL560 IC and 2 diodes. The circuit for this application is shown in Fig.1.

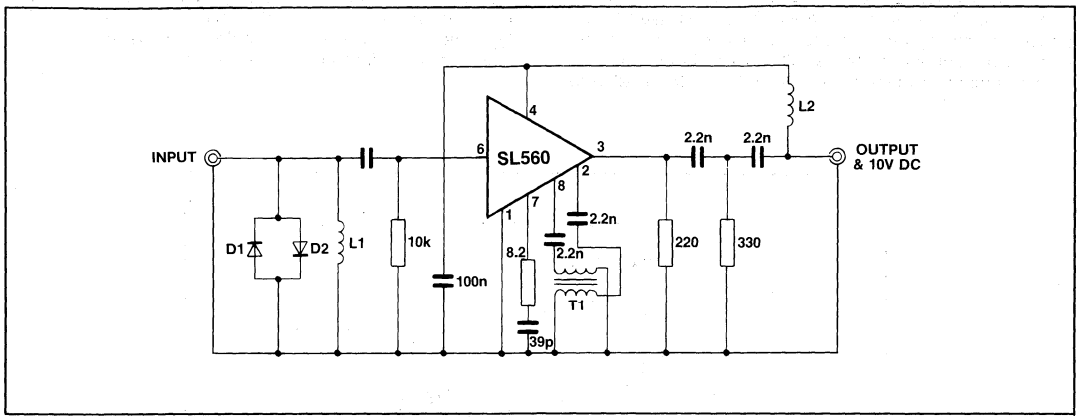


Fig.1

CONSTRUCTION

D_1 and D_2 are any general purpose silicon diodes.
L_1 is 8 turns of 26 gauge, ⅛ inch internal diameter.
L_2 is 20 turns of 26 gauge, 3/16 inch internal diameter.
T_1 consists of two lengths of 34 gauge wire approximately 6 inches in length, twisted together (8 twists/inch) and wound on a 6-hole ferrite bead (Mullard FX1898).
L_1 provides a degree of high pass filtering, some measure of protection against lightning by virtue of the DC path to earth, and it improves input SWR.
Resistor and capacitor values are not critical.
The module is powered through the coaxial cable and requires 10V at 30mA.

PERFORMANCE SPECIFICATION

The gain, 2nd and 3rd order intermodulation intercepts and SWR against frequency is shown in Fig.2. The gain flatness is within 5dB and the noise figure is better than 8dB.

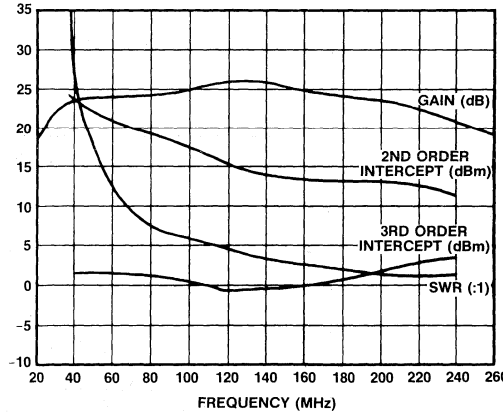


Fig.2

Using the SL561 in Pulse Amplifiers

The SL561 low noise preamplifier finds many applications in infra-red and ultrasonic equipments where a radar type signal is to be amplified. In such applications, large input signal levels can lead to unwanted pulse stretching. This application note describes the mechanisms involved and offers a simple remedy.

Generally, a large input signal which is of more than sufficient amplitude to severely overload the SL561 is applied and the amplifier is required to be at full gain as little as 10 microseconds later.

Study of the SL561 circuit diagram (Fig.1) shows that a large positive input pulse will lead to saturation of the input transistors. The effects of stored charge will lead to the transistors staying turned on for some time after the pulse, and a high source impedance will exacerbate the situation.

The amount of pulse stretching will vary from batch to batch of devices, as the amount of charge injected has a number of possible paths for its dissipation. By using a Schottky diode, as in Fig.2, the effects of the hard saturation can be avoided. When the cascode transistors saturate, the potential at the collector of the top transistor is low enough that the diode conducts, diverting input current away from the input transistor. The diode must be a Schottky barrier type and typically, the output pulse length is reduced by a factor of 12 to 15 when the diode is fitted.

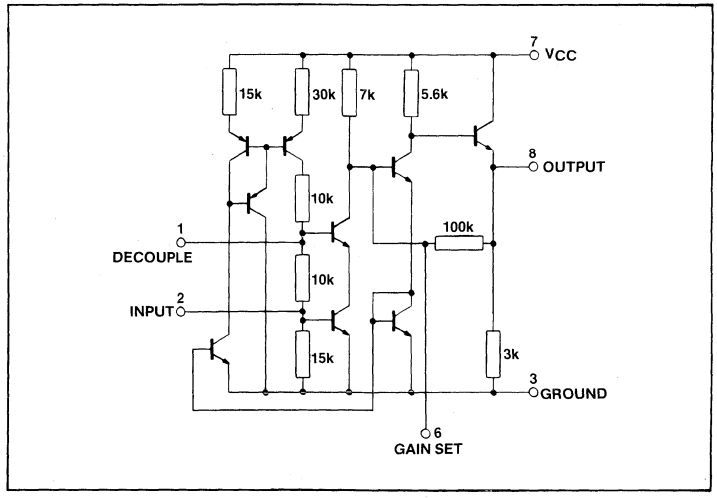


Fig.1 Circuit diagram

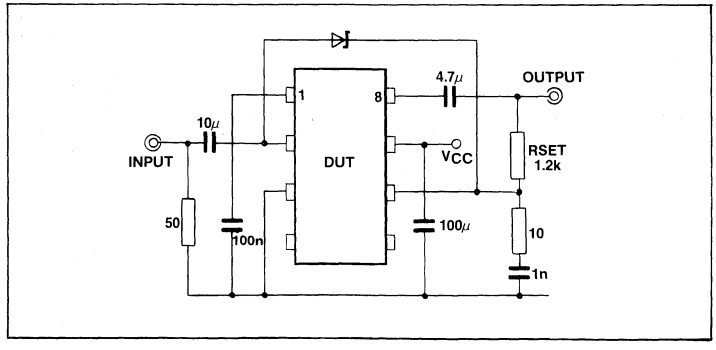


Fig.2 Application circuit

Stabilising the SL952 in Chip Carrier Package

High frequency amplifying devices are notoriously difficult to use satisfactorily unless great care is used in design and layout of the PCB. At times, even this is insufficient, and other means have to be used to obtain stability. The move to chip carrier packaging may then negate all previous experience, and a new approach is required.

The SL952 has been available in Ceramic and Plastic dual-in-line package for some considerable time. Originally designed for use as buffer amplifier limiters in TV tuners, other areas of application exist for this device, but the susceptibility of the device to oscillate with no input is sometimes a problem in such applications. An exercise to evaluate the device in a chip carrier package showed that a violent oscillation at about 700MHz prevented its use, and an investigation was carried out into causes and possible cures.

The problem with an oscillating device of this kind is that it is not amenable to theoretical analysis as a two port network: the S parameters cannot be measured on an oscillating device, which precludes the use of Linville or Sterns Stability analysis. Thus it was necessary to use an intuitive approach.

The circuit of Fig.1 was supplied ready built. The input and output tracks were long (about 1.25 inches) and were about 75Ω impedance. Although chip capacitors had been used, they were not returned to the top ground plane. Thus the RF layout was not ideal.

Initial investigation centred round reproducing the problem and the oscillation was found. A 56Ω resistor connected across the outputs improved performance and the input was approximately matched by connection of a 56Ω resistor across the input (see Fig.2). The oscillation still persisted and two possible causes were envisaged:

1. Feedback through the device, suggesting that at best it is only potentially stable.
2. A combination of (1) and spurious inductances.

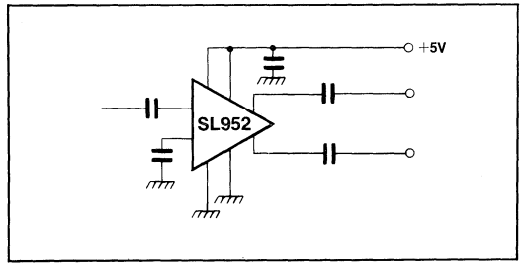


Fig.1

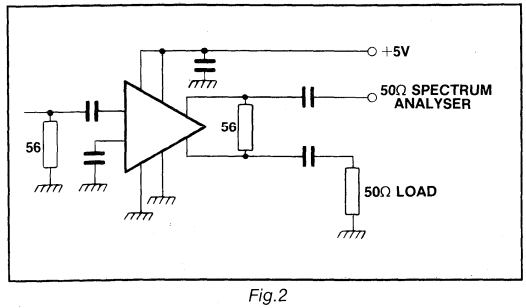


Fig.2

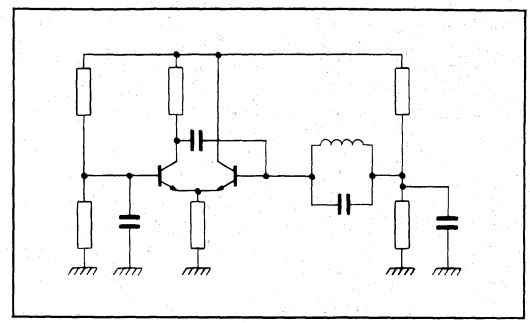


Fig.3

The emitter coupled oscillator of Fig.3 is obviously a candidate for suspicion as to mechanism; Fig.4 is the embedding of the transistors into an IC of SL952 form.

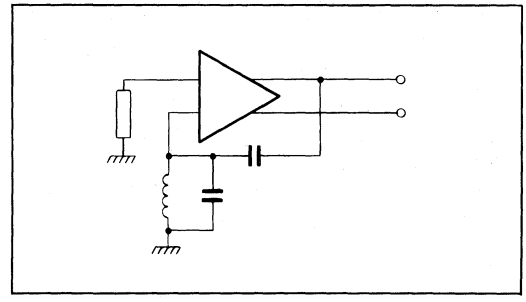


Fig.4

If this theoretical approach is correct, then it should be possible to estimate the frequency of oscillation and if this agrees with observed result, the theory is (possibly!) correct.

The track connecting the unused input to the bypass capacitor is a 150-ohm transmission line of length 10mm, which is 0.023λ at 700mHz.

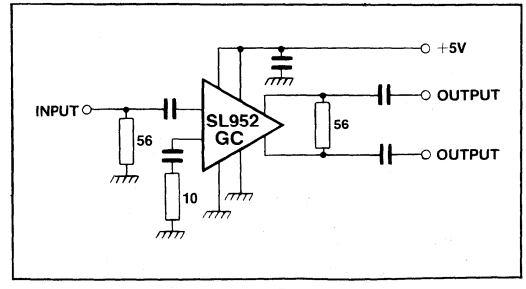


Fig.5

This corresponds from the Smith Chart to a normalised reactance of 0.15, or 22.5Ω, which converts to 5.2nH. The bond wire inductance is likely to be about 3nH and the input capacitance about 5pF. This gives a resonant frequency of 795MHz: the observed frequency was 735MHz and so agreement exists within the limits of error in estimating capacitances, impedances and strays.

From these figures, it appears likely that removal of the inductance by open circuiting the unused input should stop the oscillation, and this was empirically confirmed.

Leaving this input open circuit is undesirable and so it is required to 'ground' it in some way. The connection of a 10Ω resistor in Fig.5 reduces the Q of the tuned circuit to a value:

$$Q = XL/R = 3.5$$

However the question remains of the adequacy of this.

Q without the resistor is probably about 50. This gives an effective impedance of 1.8k from the unused input to ground. If this is decreased to 123Ω by the inclusion of a 10Ω resistor, then feedback to this point must be increased by 23dB. The output of the device when oscillating was about -12dBm, so it appeared probable that a 10Ω resistor would suffice - and it did.

Table 1 lists the saturated output level and unsaturated gain against frequency.

Frequency (MHz)	Saturated Output Level (dBm)	Gain (dB)
30	-2.4	21.0
60	-2.2	23.1
100	-3.1	24.3
150	-2.8	24.6
200	-3.4	22.1
250	-2.4	26.5
300	-3.3	21.1
350	-2.1	25.9
400	-3.7	26.0
450	-3.8	23.2
500	-3.7	28.9
550	-3.6	22.5
600	-4.2	23.9
650	-3.9	21.7
700	-3.2	29.1
750	-4.3	22.2
800	-4.4	15.7
850	-4.5	15.5
900	-4.8	16.3
950	-5.4	14.3
1000	-5.4	14.4
1050	-6.2	14.5
1100	-8.2	8.9

NB Inaccuracies are likely to be 1.0dB.

Table 1

SUMMARY

The analysis given above is somewhat detailed and has been included in this application note to give a guide to the processes used to obtain stable amplification with high frequency devices. The use of correct design techniques with S parameters where available is recommended, although even then, curing an instability is not readily predictable from theoretical grounds and computer designs are just as likely to give problems as the old fashioned approach. However, an understanding of the basic technical parameters, an appreciation of parasitic impedances and the use of good layout techniques will assist in achieving the desired peformance.

SL2365 Applications

The SL2365 is an array of transistors configured to form a dual long-tailed pair with tail transistors which are current mirrored to similar transistors whose bases and collectors are connected internally.

The ICs are manufactured on a very high speed bipolar process which has a typical f_T of 5GHz. The device is available in a surface mounted DIL package (MP14), the pin connections of which are shown below.

Various applications are described including a 900MHz amplifier, a frequency doubler, a frequency tripler and a single balanced mixer.

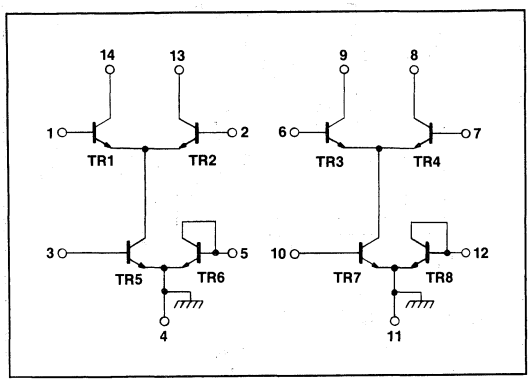


Fig.1 SL2365 schematic diagram

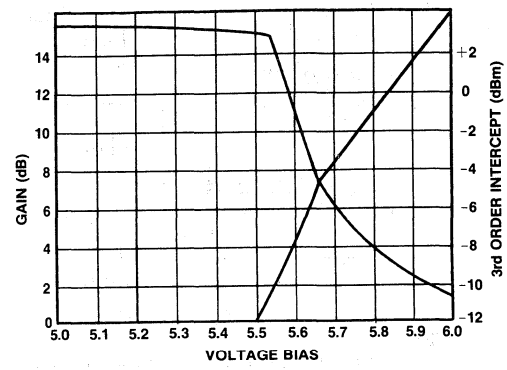


Fig.3 3rd order intercept at gain of 12.5dB (using current mirror at 4mA) = -7dBm

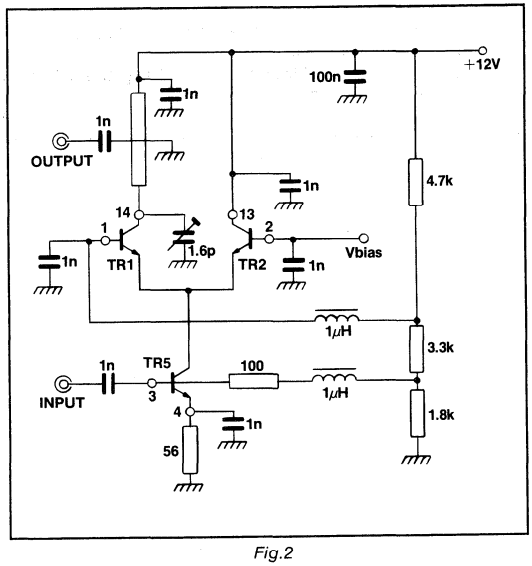


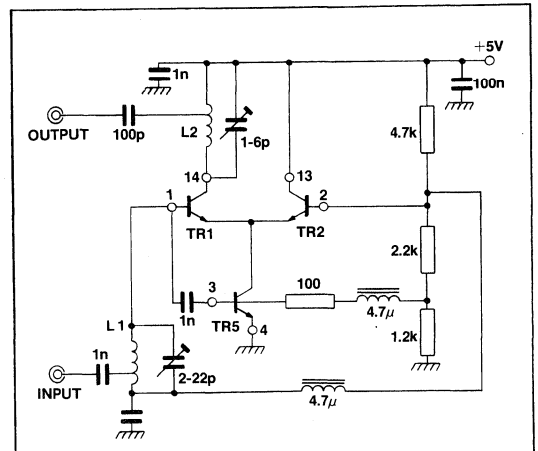
Fig.2

A 900MHz GAIN CONTROLLED AMPLIFIER

In Fig.2, the collector load of TR1 is a transformer composed of a 14mm length of 75Ω stripline resonated with a 1-6pF variable capacitor. The secondary of the transformer is a small loop of stiff wire grounded at one end and located a few mm above the stripline. The gain and 3rd order intercept versus V bias is shown in Fig.3. The noise figure at full gain is 9dB.

A 150-300MHz FREQUENCY DOUBLER

The frequency doubler, Fig.4, has a gain of +1dB for a -20dB input and input frequency rejection of 18dB.

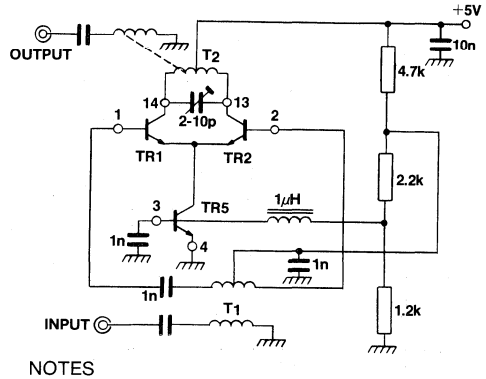


NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
L_2 = 3 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from 5V rail end

Fig.4

A 100-300MHz FREQUENCY TRIPLER

Fig.5 shows a 100-300MHz frequency tripler with a gain of -40dB, input frequency rejection of 30dB and second harmonic rejection of 28dB.

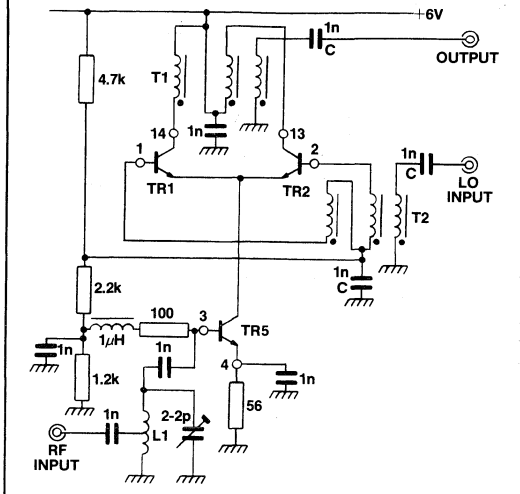


NOTES
T_1 Primary = 4 turns 36 swg enamelled wire wound on ferrite core
T_1 Secondary = 4 turns 36 swg enamelled wire wound on LF ferrite core (twisted pair)
T_2 Primary = 2 turns 20 swg tinned wire 5mm diameter
T_2 Secondary = 4 turns 20 swg tinned wire 5mm diameter, positioned axially relative to T_2 Primary

Fig.5

A SINGLE BALANCED MIXER

The mixer of Fig.6 has a gain of 13dB, 3rd order intercept = -13dBm. -10dBm (using 2mA in current mirror) and noise figure = 10dB.



NOTES
L_1 = 4 turns 20 swg tinned wire 5mm diameter. Tapped 1 turn from ground end
T_1 and T_2 = 4 turns of trifilar wound 36 swg enamelled wire wound on LF ferrite core

Fig.6

Tuned Amplifier using the SL6140

The SL6140 wideband AGC amplifier, when used in a 50Ω system, has a gain of 15dB. By tuning, or matching, the inputs and outputs of the device the gain can be increased. This produces a higher gain amplifier that will work over a limited bandwidth. The bandwidth of the amplifier depends on the Q factor of the tuned/matching circuits used. Fig.1 shows a single ended amplifier with a tuned input and output network.

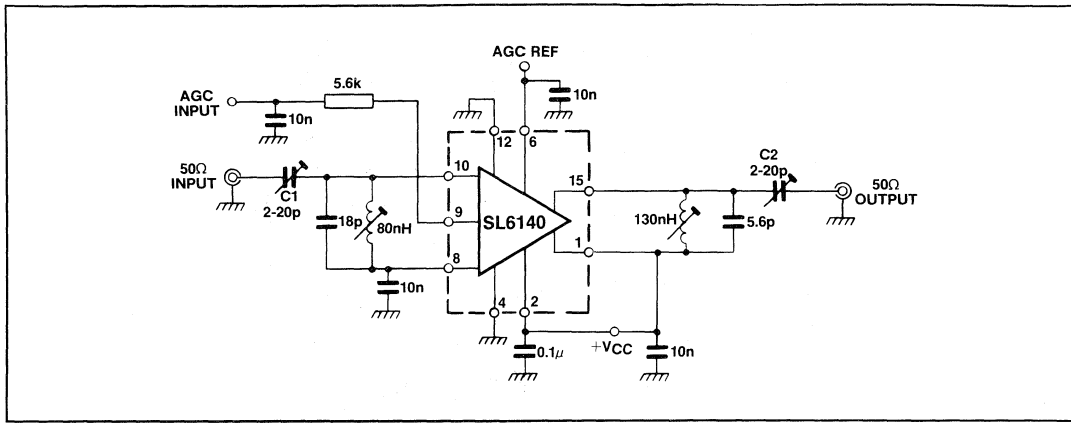


Fig.1 A 100MHz tuned amplifier application 35dB power gain (leadless chip carrier pinout)

DESCRIPTION

The input circuit consists of a parallel LC network connected across the differential inputs. The input signal is applied to one input, via a coupling capacitor (C1), whilst the other input is decoupled. The coupling capacitor also forms part of the impedance matching network, matching a 50Ω source with the high input impedance of the device (see Smith chart, Fig.3).

The tuned frequency is given by the following equation:

$$f = \frac{1}{2\pi \frac{\sqrt{L \times C \times C1}}{\sqrt{(C + C1)}}}$$

The output circuit consists of a parallel LC network connected from one of the open collector outputs of the device to V_{CC}. The other output is connected directly to V_{CC}. The coupling capacitor (C2) and LC network transforms the 50Ω load to a high impedance load for the open collector outputs of the device, hence improving the gain.

By adjusting C1 and C2 the gain can be optimised. But if too high an impedance is seen by the input or output of the device the circuit may oscillate. L1 and L2 are adjusted to set the tuned frequency.

The high gain is achieved at the expense of bandwidth. So for maximum gain the matching network should be adjusted to provide the minimum bandwidth necessary, for the particular application.

An alternative method of tuning the output of the device is to transformer couple to the 50Ω load. The primary winding is connected across the outputs (a centre tap providing V_{CC}) and resonated, at the required frequency, with a capacitor, see Fig.2. This circuit has a 6dB improvement in gain over the previous circuit as both outputs are used.

PCB LAYOUT

For best performance a ground plane should be used with 50Ω track from the matching networks to the 50Ω source and load. The matching network and decoupling capacitors should be positioned as close to the device as possible.

If a very high gain, low bandwidth, amplifier is required the addition of some shielding between input and output may be necessary to prevent oscillation.

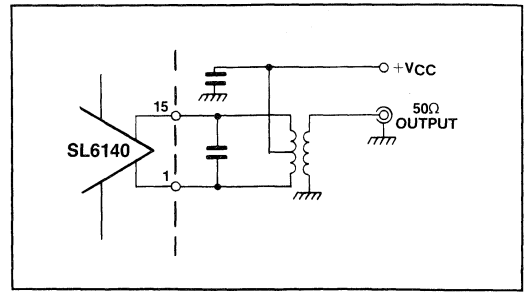


Fig.2 Differential tuned output

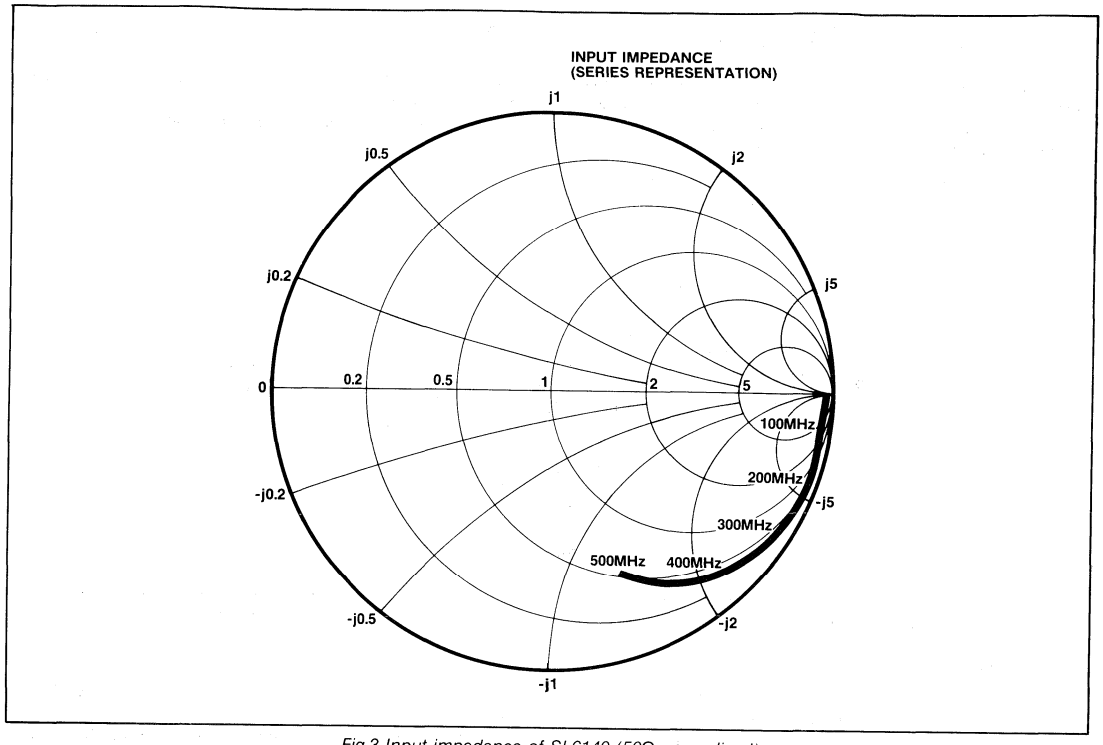


Fig.3 Input impedance of SL6140 (50Ω normalised)

SL6270C — An Integrated VOGAD Circuit

The SL6270C is a monolithic integrated circuit intended for use in audio applications requiring constant output levels. It finds applications in radio communications, tape recorder applications, sound surveillance instrumentation and related areas. It has a differential input, and a constant output level of 90mV RMS, with a sensitivity of 1mV.

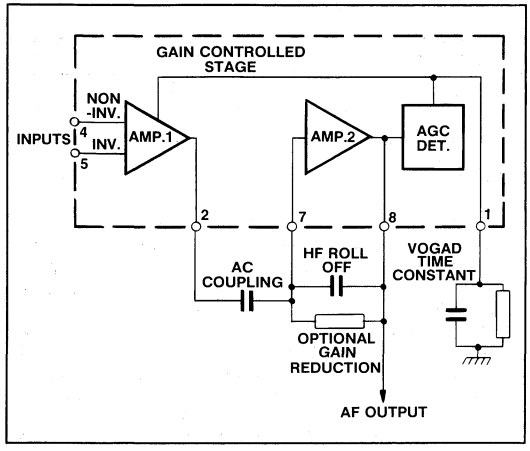


Fig.1

Voltages

The voltages given in Table 1 were measured in the circuit of Fig.2, with R2 = ∞, C1 = 2.2μF, C2 = 4700pF, C3 = 47μF and R1 = 1MΩ. The input was coupled via 2.2μF to pin 4, with pin 5 open circuit. Voltages were measured with a 20kΩ/V meter.

Pin	Input = 0mV	Input = 10mV	Input = 100mV
1	0V	1.6V	1.7V
2	3.5V	3.6V	3.6V
3	6.0V	6.0V	6.0V
4	1.6V	1.6V	1.6V
5	1.6V	1.6V	1.6V
6	0V	0V	0V
7	1.4V	1.4V	1.4V
8	1.4V	1.4V	1.4V

Table 1

DESCRIPTION

Refer to Block diagram - Fig.1.

The differential input amplifier is AGC controlled, and, being a true differential input, can be driven single ended, without the problems caused by other forms of push-pull input. The output from the AGC stage is coupled via a capacitor to the second stage, which is gain programmable by a single resistor. Adding a capacitor in parallel with this resistor allows the HF response to be programmed, if desired.

The output of this amplifier provides the main audio output from the device, and also drives the AGC detector. The detected output, which is input level dependent, is applied to the time constant circuit, and also to the gain controlled stage.

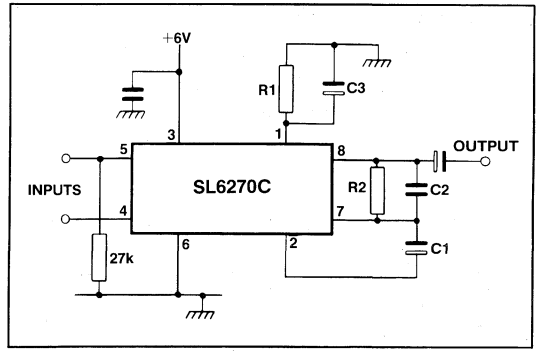


Fig.2 Connection diagram for SL6270C used as a microphone amplifier

Pin Functions

Pin	Function
1	**Gain control line.** An increasing voltage decreases the gain of the 1st amplifier.
2	**Audio output** from the gain controlled amplifier.
3	**Vcc supply.**
4	**Non-inverting input** to the gain controlled amplifier.
5	**Inverting input** to the gain controlled amplifier.
6	**Ground (0V).**
7	**Input to the second amplifier.** This is an inverting amplifier.
8	**Output of the second amplifier.**

The frequency response of the circuit of Fig.2 is shown in Fig.3: the input/output and overload characteristics are shown in Figs.4 and 5 respectively. Fig.8 shows the intermodulation distortion, and Figs.9 and 10 the pin connections. In the circuit of Fig.2, the microphone may be connected between pins 4 and 5 or between either pin 4 or 5 and ground.

Because of the careful design of the input stages, the device has an extremely high input dynamic range, and Fig.5 shows the distortion characteristics at various inputs.

The gain of the second amplifier can be programmed with a resistor between pins 7 and 8. This resistor value should not be less than 390Ω, while the threshold point is increased to about 8mV with a 1kΩ resistor. The gain of this amplifier without any feedback is approximately 50dB.

Decay rate is fixed by the RC network on pin 1, and with the values given is approximately 20dB/s.

In order to ensure that amplifier internal offsets are of such polarity as to inhibit oscillation at the onset of AGC, a 27kΩ resistor should be connected from pin 5 to the negative supply line.

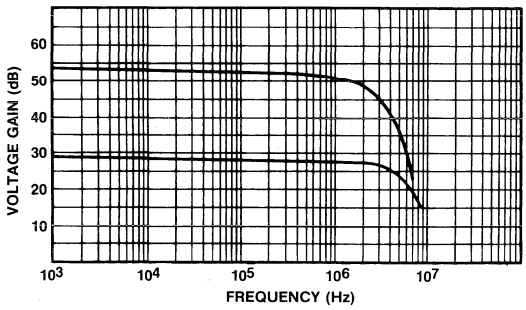


Fig.3 Frequency response

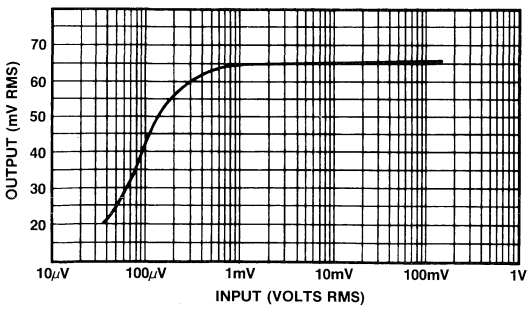


Fig.4 SL6270 Input/output characteristics Vs = +6V, T_{amb} = +25°C, f = 1kHz single ended input

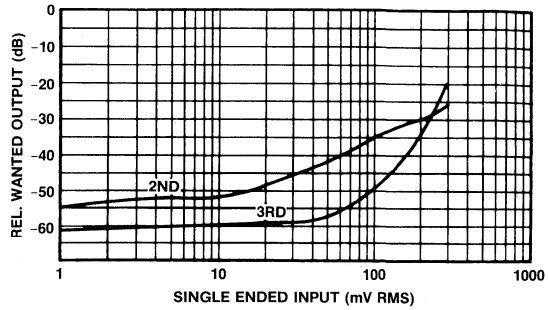


Fig.5 SL6270 distortion products v. input signal Vs = 6V 1kHz

APPLICATIONS

The simplest application for the SL6270C is in such applications as a radio transmitter. Fig.6 shows its use as a microphone amplifier and VOGAD with differential input.

Because of the separation of the gain controlled stages and the AGC generator, it is possible to use two SL6270C devices to control one audio signal by another one - see Fig.7. Here, a signal in Channel 1 causes gain reduction in Channel 2, and so, by suitable interconnection, a 'priority' system can prevent interference to the used channel.

IC1 acts as a VOGAD for Channel 1: IC2 for Channel 2. Whichever VOGAD is in operation reduces the gain of the other channel and thus, for multiple input sources, inteference from 'open' microphones is prevented.

Such a system may also be used for controlling voice operated switching devices since 'Antivox' can be applied to one device from a receiver output, and while the microphone is connected to the other. Receiver noise will then reduce the sensitivity of the transmit channel, preventing spurious triggering on received signals.

Where the SL6270 is used in applications with a DC path between pins 4 and 5, the resistance of this path should not exceed 10Ω. Otherwise, this path should remain open circuit.

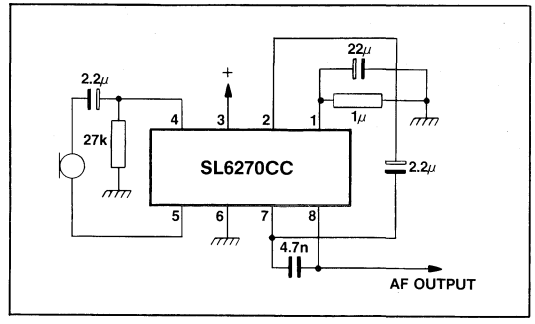


Fig.6

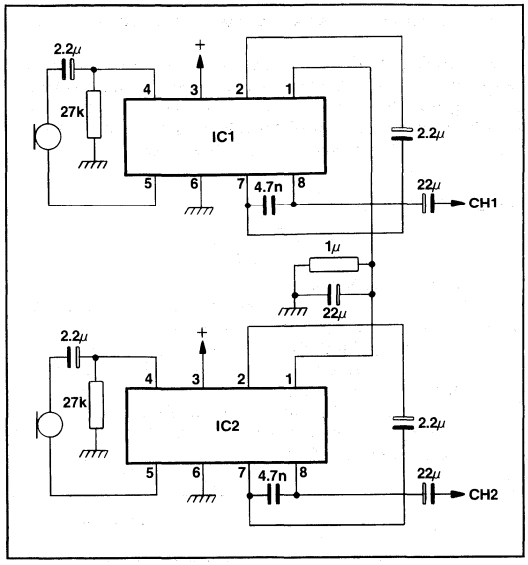


Fig.7

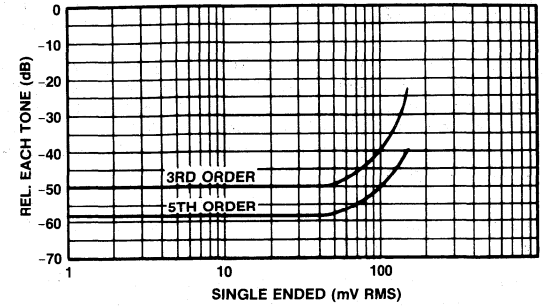


Fig.8 SL6270 3rd and 5th order IPs 1.55 and 1.85kHz Vs = 6V

Applications of the SL6310C

The SL6310C is an integrated circuit designed specifically for use as an audio amplifier. It will operate from supplies of 4.5 to 15V, and will typically deliver an output of 500mW into 8Ω with less than 3% distortion at 9V, while at 12V, it can deliver up to 1W. It is a highly attractive circuit for hand held radio equipment, incorporating a mute or shutdown circuit, allowing the current consumption to be reduced to less than 600μA. In addition, being basically an operational amplifier with a power output stage, it is suitable for many other applications, such as a voltage regulator with shutdown, lamp driver, PIN diode driver, power comparator, and many other applications.

Fig.1 shows the block diagram of the SL6310C. In the AF amplifier application circuit (Fig.2), typical pin voltages and uses are as follows:

Pin 1 This is the non-inverting input pin, and is normally biased externally to half the supply voltage.

Pin 2 The inverting input: This will also be at half the supply voltage, being biased from the output.

Pin 3 Negative supply pin.

Pin 4 Output pin: This will be at half the supply voltage.

Pin 5 Positive Supply: This should be decoupled with an electrolytic capacitor connected with short, wide tracks.

Pin 6 Leave open circuit.

Pin 7 Mute control 1: This pin, when taken to earth via 100k, shuts down the circuit.

Pin 8 Mute control 2: This shuts down the circuit when taken to a potential greater than 2.2V above the negative supply line.

Both mute circuits should not be used simultaneously, but doing so will not damage the circuit.

A 1W AF AMPLIFIER APPLICATION

In this application (Fig.2) the circuit is biased by R1 and R2 to half the supply voltage on the non-inverting input, while DC feedback via R3 ensures that the amplifier acts as a voltage follower at DC.

The gain is fixed by R3 and R4, and is given by:

$$G = \frac{R3 + R4}{R4}$$

at mid-band frequencies.

The frequency response is fixed by C1, C2, and C4. C2 alters the amount of feedback at low frequencies, C4 is a series impedance with the load, while C1 is in series with the input. The HF response may be reduced by shunting R3 with a capacitor. As a guide, the LF response will be down by 6dB when XC4 = RL, or when XC2 = R4, while the reactance of any capacitor shunting R3 is equal to R3: With no capacitor across R3, and values of R3 and R4 to give a gain of 20dB (10 times), the frequency response exceeds 20kHz.

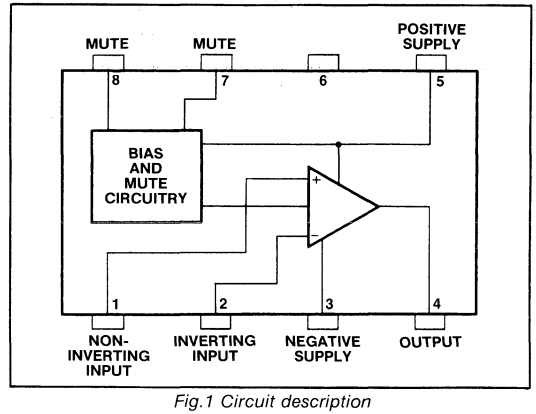


Fig.1 Circuit description

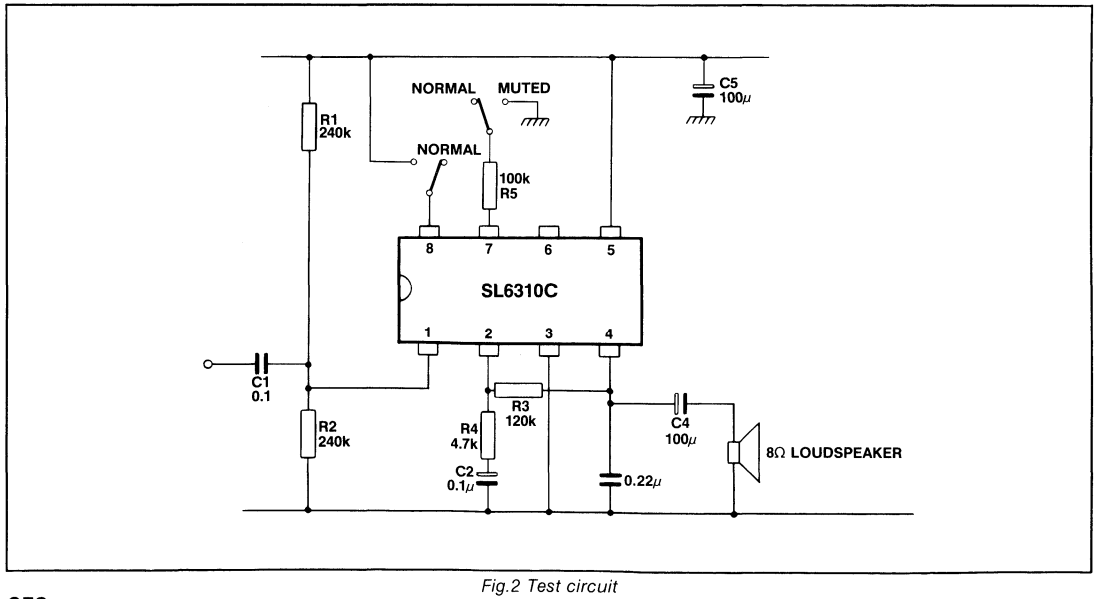


Fig.2 Test circuit

Because of high peak current (0.7A at 500mW in 8Ω), the supply pin (5) should be bypassed with an electrolytic capacitor, connected with short, wide leads, to obviate modulation of the supply rail.

The output power available is dependent on the supply voltage, and typical output powers range from 500mW into 8Ω at 9V to 1W at 12V and 1.3W at 15V.

Muting (or Shutdown)

There are two methods of muting the SL6310. Pin 8 may be lifted to a voltage greater than 3Vbe above the negative supply rail or, alternatively, Pin 7 may be pulled down to 1Vbe below the positive supply. Pin 7 should not be directly connected, but should have a resistor of 100kΩ in series to limit the current. Pin 8 has an input resistance of around 100kΩ, and so may be driven directly from TTL, LPTTL or CMOS is required. Both mutes should not be used simultaneously.

MORE APPLICATIONS

Fig.3 is a simple voltage follower application: the output current must be less than 0.4A and the dissipation must not exceed 1W at +25°C. The output voltage will need more than 2V below the supply voltage and will be equal to the voltage of the Zener diode, D1. The 220nF capacitor prevents instability.

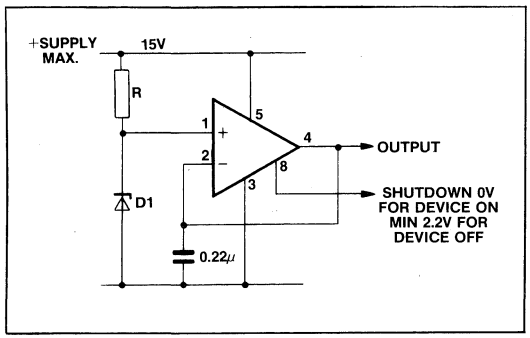


Fig.3 Power supply with shutdown

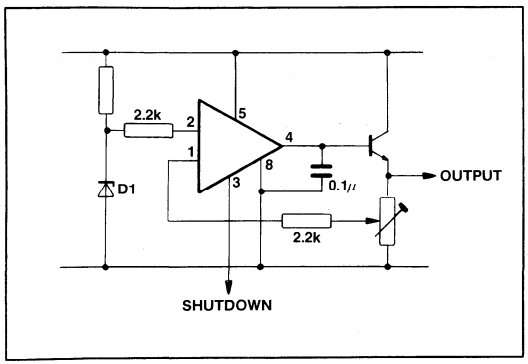


Fig.4 Preset power supply with boost transistor

In Fig.4 the output voltage is less than the Zener voltage, while the boost transistor allows a substantial increase in current capability. At high current levels, series pass transistors suffer from a drop in current gain, and thus require more base drive. The high output current capability of the SL6310C obviates the requirements for expensive Darlington transistors.

Applications of the SL6310C for use as a power comparator, lamp driver and DC servomotor driver are shown in Figs.5, 6 and 7, respectively.

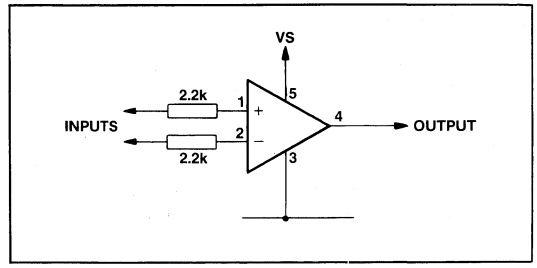


Fig.5 Power comparator

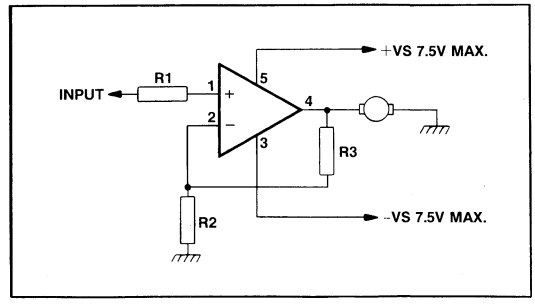


Fig.6 Lamp driver

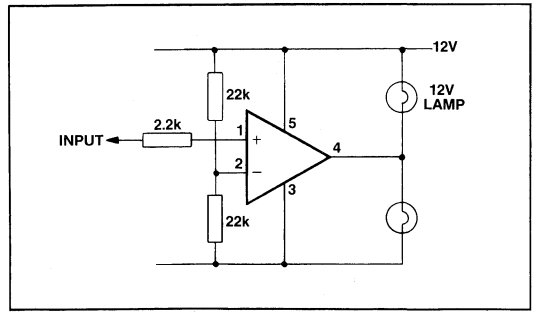


Fig.7 DC servo driver

SL6440 High Level Mixer Applications

High performance modulators and frequency changers have historically used gain-less commutative mixer circuits such as the diode ring, or one of its derivations using FETs.

Integrated circuit mixers are available for only low signal levels, but also with relatively poor intermodulation performance. Other active mixers have not offered particularly good performance.

Typically, radio receivers requiring 3rd order intermodulation intercept points of +25 to +30dBm have used diode or FET commutative mixers with their inherent disadvantages of termination sensitivity and loss. The SL6440 is capable of 3rd order intermodulation distortion (IMD) performance far in excess of what has been previously available in integrated circuits together with gain and the advantages of integrated circuit technology.

MIXER TYPES AND DERIVATIONS

The basic balanced mixer is the single balanced type of Fig.1. This offers balance to the frequency f_2, but not f_1, and is analogous to a switch driven at f_2 opening and closing the connections between the transformers. Thus, f_1 is 'chopped' at f_2, and sidebands at $f_2 \pm f_1$ are produced. However, the output also contains components at f_1, and this is often an inconvenience. Fig.2 shows the diode ring modulator. In this, the signal current due to f_1 is switched alternately through the diodes to appear across the output transformer.

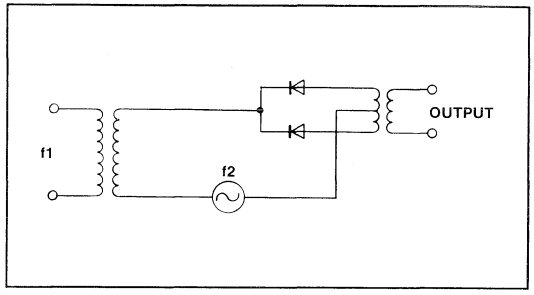


Fig.1 Single balanced mixer

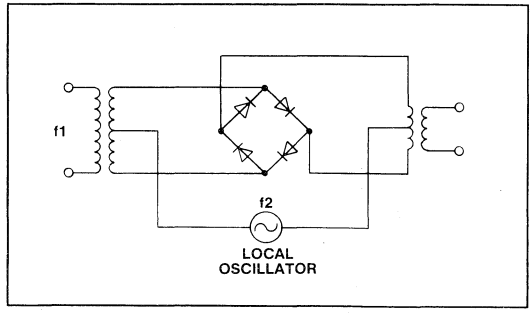


Fig.2 Diode ring

This switching is accomplished by the f_2 signal, which need not be applied across the centre taps of the transformers as shown but may be applied at a transformer port. The double balanced ring mixer of this variety is balanced to both input frequencies and is a very versatile and useful device. However, there are certain disadvantages, and these are:

1. High local oscillator power is required.
2. There is a loss inherent in the circuit.
3. The IMD performance is dependent upon the source and load termination impedances.
4. The balance (and thus the rejection of f_1 and f_2) is dependent upon the transformers and the diode matching.

Of these disadvantages, (1) is dependent upon the power handling required, while (2) can be shown to be $(3.12 + \log R_2/R_1)$dB, where R_1 and R_2 are the forward and reverse resistances of the diodes. This expression neglects transformer losses, and may be achieved only by proper termination. Unfortunately, this termination is one such that the image frequency components are reflected back into the mixer, and this can be shown to conflict with (3), where good IMD performance can be shown to require broadband terminations. Balance, however, can be relatively easily obtained with simple transformers and matched diodes.

One of the major disadvantages of the diode ring for very high performance is the amount of local oscillator power required, which is apparent if consideration is given to the diode characteristics. For example, if the total current through the diode is $I_{osc} + I_{sig}$, then at room temperature the forward resistance of the diode is $25/I_{total}$ ohms (where I is in mA). If I_{sig} is very small, the resistance of the diode is determined by I_{osc}, but if the I_{sig} is comparable with I_{osc}, the forward resistance is affected by the signal current. Because this is a non-linear relationship, intermodulation distortion will follow.

Where FETs are used, modulation of the ON channel resistance by the signal is a cause of Intermodulation Distortion. Unlike the ring mixer, this IMD cannot be decreased by increasing the local oscillator driver power, careful choice of FETs is required to achieve best results. Because the FET is used as a bi-lateral switch, the comments on terminations are as applicable to the quad FET mixer as to the diode ring. It should be noted that the simple non-commutative FET mixer is not particularly good on IMD or rejection of the LO signal.

One of the advantages of the double balanced mixer is its rejection of AM noise on the local oscillator, which can be a definite advantage in synthesised radio receivers.

The relative advantages and disadvantages of the various types of mixer are set out in Table 1. Although these tables provide a guide, they should not be considered as inviolable rules, applicable to all mixers of that particular type, because any particular mixer may or may not suffer from all the faults listed.

The transistor double balanced mixer is capable of minimising many of these problems. The circuit diagram is shown in Fig.3; because of the vertical stacking, it is often referred to as the 'transistor tree' mixer.

The performance of the 'tree' mixer of this sort is dependent upon several of the parameters of the transistors, and the ultimate performance requires some compromises of overall performance. However, noise figure and IMD can be easily optimised for best dynamic range, and this has indeed been done in the SL6440.

Mixer type	Advantages	Disadvantages
Single diode	Wide bandwidth, low LO power, low cost.	No rejection of any component, no interport isolation, low input impedance.
Single FET transistor	Low noise, low loss or some gain, low cost.	Very poor IMD, no isolation, no AM rejection, poor overload, low input impedance.
Diode ring	Good IMD possible, high overload and compression.	6dB loss at least. IMD critically dependent on load termination. High LO drive power, and limited isolation. Low input impedance.
Quad FET	Good IMD range possible, overload good, low noise.	Expensive. Conversion gain, IMD and noise not easy to optimise. IMD performance is load dependent.
SL6440 IC balanced mixer	IMD performance set by current. Good LO isolation. Low LO power requirement. May be used with single ended or differential drive. IMD performance independent of load impedance. High input impedance. Can give gain by choice of output impedance.	Bandwidth limited to 200MHz. Noise figure 11dB for best IMD. Compresion Compression point lower than best diode rings.

Table 1

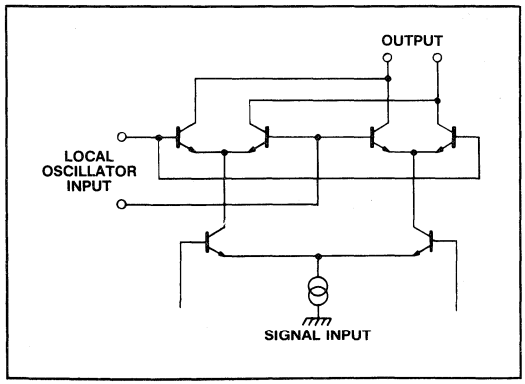


Fig.3 Transistor tree

THE SL6440 HIGH PERFORMANCE MIXER

Refinements to the transistor 'tree' allow the IMD of the simple tree to be improved. This improvement is dependent upon the amount of current in the transistors at the bottom of the tree. Obviously, for large input signals this current must be quite high and is modulated by the input signal current.

For best IMD results, the voltage-to-current conversion in the bases of the lower transistors should be as linear as possible, while minimum noise requires the lowest possible amounts of emitter resistance. The gain is also dependent upon the magnitude of the load resistance, but obviously, this magnitude must not be such as to saturate the transistors when the maximum current is flowing. In the SL6440, this current, and thus the IMD performance, is programmable by means of an external resistor, thus allowing a great deal of flexibility in use.

Figs. 4, 5 and 6 show the relationships between IMD performance, compression point, bandwidth and current and voltage. In general, it can be seen that increased supply power gives increased performance. However, it must be remembered that where the SL6440 is used such that conversion gain occurs, the compression point is reduced.

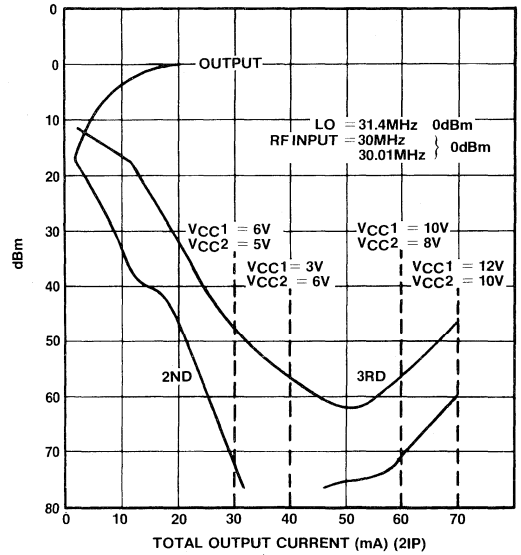


Fig.4 Intermodulation v. total output current (2IP). Average composite readings.

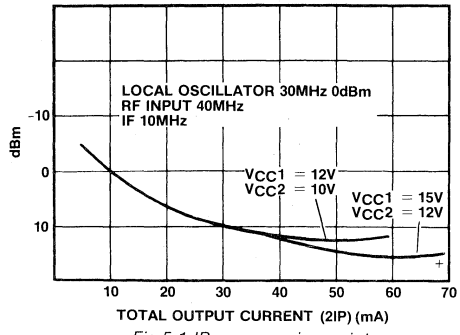


Fig.5 1dB compression point

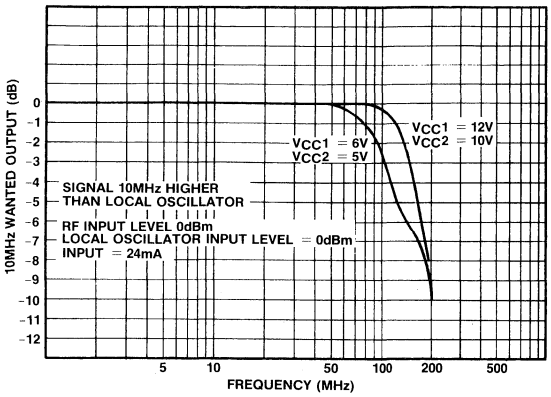


Fig.6 Frequency response with constant output IF

USING THE SL6440

The SL6440 is very flexible insofar as it can be used with differential or single ended inputs and outputs. For best balance, the use of a differential input is recommended, and Figs.7, 8 and 9 show that variation in carrier rejection with circuitry. The use of the differential output allows 6dB gain to be obtained while the high input impedance allows voltage step-up to be achieved.

Pin Functions

Pin	Function
13 & 12	**Signal input.** These pins may be connected together for best carrier suppression, but should not be DC coupled to any external voltage source or load.
3 & 14	**Open collector outputs.** These are connected to Vcc1, via load resistors, transformer windings, or as required.
4	**Vcc2,** normally about 2 to 3V lower than Vcc1, but for large output swings should be such that the instantaneous voltage at pins 2 and 3 is greater than Vcc2 + 2V.
5	**Local oscillator input.** The LO requirements are for approximately 200mV RMS with an impedance of about 1500Ω.
6	**The negative supply line.**
11	This is the current programming pin. It is connected to Vcc2 via a suitable value of resistor or fed from a current source. The current in at this pin is equal to the current in Pin 2 or Pin 3.

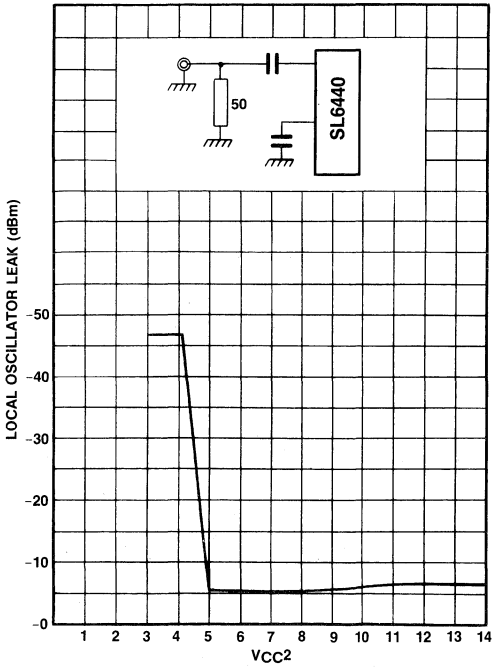


Fig.7 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, single ended input.

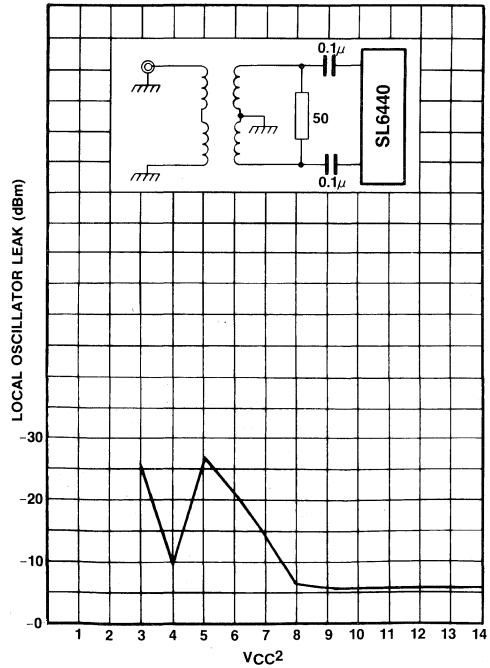


Fig.8 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, capacitively coupled transformer input.

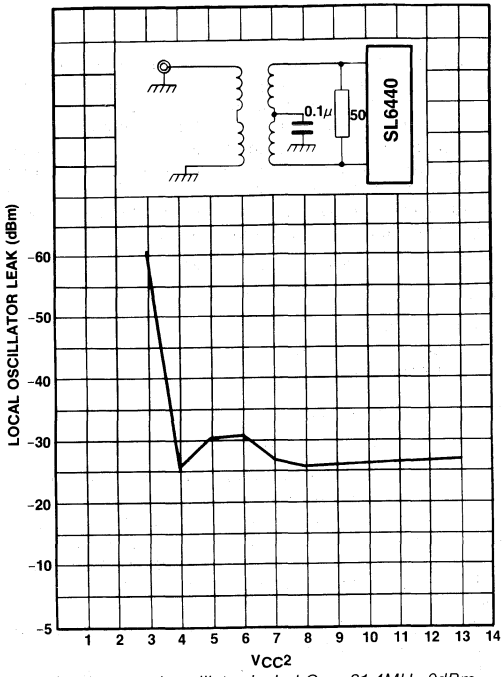


Fig.9 Local oscillator leak, LO = 31.4MHz 0dBm, Vcc1 = 15V, direct coupled transformer input.

The simplest use of the SL6440 is in the circuit of Fig.10. Here the input and outputs are single ended, and because of the voltage drop in the output load resistors, Vcc1 should be at a voltage of [(51 x I programme) + 2 + Vcc2] V. By increasing Vcc1 and the load resistors, gain can be obtained.

If transformer coupling is used, then the high input impedance can be utilised, and Fig.11 shows an application as the signal frequency stage of a high performance HF receiver. Table 2 lists the characteristics of this mixer stage, which can be improved for transmitter use by increasing the supply voltages to improve the compression point. The 500Ω resistor allows the current to be programmed as desired. The use of transmission line transformers increases the frequency range over which a good match can be obtained: those used in Fig.11 are adequate for most applications in the HF range.

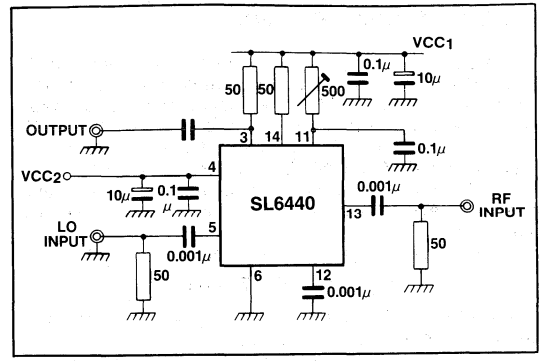


Fig.10 SL6440 basic application circuit

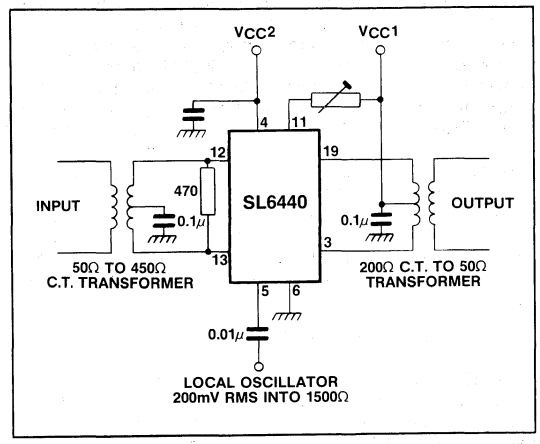


Fig.11 High performance HF receiver mixer

Parameter	Performance	Conditions
Sensitivity	15dB S + N/N	1μV EMF, SSB Bandwidth 30MHz, f = 1MHz
IMD 3rd	>-70dB	Input = 142mV EMF each signal 10kHz separation
IMD 2nd	-80dB	Input = 142mV EMF each signal
LO Radiation	-65dBm	Measured in 50Ω at input port
Blocking	100mV EMF	3dB blocking 1μV EMF wanted signal
IF Rejection	30dB	Rejection measured at input port
Input Matching	22dB	Returned loss in a 50Ω system
Gain	10dB	

Table 2 Performance of Fig.11

THERMAL CONSIDERATIONS

The SL6440 chip temperature should not exceed 170°C. As a result of this limitation, the maximum power dissipation depends upon the thermal resistance from junction-to-ambient θ_{JA}, which is in free air, approximately 125°C/W. This may be reduced by using a suitable heat dissipator, such as the IERC PEP50AB, which reduces θ_{JA} to about 65°C/W. Dissipators designed to be attached by thermally conductive epoxy generally have a somewhat higher thermal resistance.

The dissipation is given by the expression:

$$P_{dmW} = 2\ Ip\ Vo + Vp\ IP + 0.75\ (V_{CC}2)^2 + 1.5\ V_{CC}2$$

where Vo = DC level at pin 3 or 14, Vp = Voltage on pin 11 and Ip = Programming current in mA.

Vp is approximately 3Vbe, and may be assumed for most purposes to be 2.0V. Curves given on the data sheet indicate the typical performance for given dissipations.

In many applications, it will be possible to run the mixer at a low enough dissipation to allow use with minimal heat-sinking. The circuit of Fig.11 is usable without a heatsink to +60°C under the conditions shown while a simple 'glued-on' dissipator, such as an EG & G Wakefield 651B allows operation to an ambient of +80°C. For the full military temperature range of -55°C to +125°C a dissipator similar to the IERC PEP50AB coupled with a maximum dissipation of 0.75W is required for the SL6440A to be satisfactorily cooled. Note that the SL6440C is only available for the -30 to +80°C temeperature range.

The use of forced air, thermoelectric or 'cold wall' cooling systems allows increased dissipation at high temperature where required. Nevertheless, it is good practice to maintain chip temperature below the maximum rated wherever possible.

DESIGNING WITH THE SL6440

Because of its programmable capabilities, the SL6440 needs slightly more consideration in the design of the circuitry around it than is required for simple mixers. The following parameters may be chosen, although some characters are relaxed: Gain, intercept point, compression point and dissipation.

Gain is given by the expression:

$$G = 20\ \text{Log}\ \frac{R_L\ Ip}{56.6\ Ip + 0.0785}\ dB$$

for single ended output, and is 6dB greater where a differential output is used.

R_L is the load resistance in Ohms from pin 3 or 14 to $V_{CC}2$, Ip is the programming current. Intercept point is primarily dependent upon the value of Ip and can be chosen from the graphs.

Compression point is more complex. It is more convenient to work in terms of output compression, as input compression is dependent upon the gain. The voltage on the output pins should not be so low that the output transistors can saturate. This means that the quiescent voltage on these pins must be greater than $V_{CC}2$. Should the output transistors approach saturation, the frequency response may be reduced, which is most noticeable when using the SL6440 for 'up-conversion'. The minimum value of $V_{CC}1$ is:

$$V_{CC}1\ (\text{min}) = (Ip\ R_L) + Vs + V_{CC}2$$

where

Ip is the programming current
R_L is the DC load resistance
Vs is the peak output voltage.

If $V_{CC}1$ is set such that

$$V_{CC}1 = (2\ Ip\ R_L) + V_{CC}2$$

then compression will occur at the input of the device.

The information given above, in conjunction with the data sheet allows the optimum working conditions to be decided. Because of the flexibility inherent in the SL6440, there are many possible modes of operation, but once the required circuit parameters are known, these conditions are readily determined.

The measurement techniques required for the accurate and repeatable evaluation of intermodulation performance covered in Plessey Semiconductors Radio Telecoms IC Handbook (Publication No. PS2123). When measured with a correctly designed test system, the SL6440 performance can be evaluated, while its flexibility in use coupled with its high performance offer many advantages to equipment designers.

REFERENCES

1. Mixers for High Performance Radio, Session 24, WESCON, 1981. Published by Electronic Conventions Inc., 999 N. Sepulveda Blvd., El Segundo CA.
2. CHADWICK P.E. High Performance Integrated Circuit Mixers. I.E.R.E.Conference on Radio Receivers and Associated Systems, Leeds, 1981. (I.E.R.E. Conference Publication No. 50)

SL6655 — A Very Low Power FM Receiver IC

The SL6655 is a single conversion receiver IC and consists of an RF amplifier, mixer, oscillator, IF amplifier and detector. The current consumption is extremely low (typically 1mA) and the device can be powered down to currents of 1μA. The device will operate over a voltage range of 0.9V to 8V, with a sensitivity of typically 250nV (for 12dB SINAD) at 1.3V. The low voltage and current consumption of this integrated circuit, together with its good sensitivity make it ideal for radio pager applications, where minimum physical dimensions and low power are essential requirements. The design is optimised for the use of low cost and readily available ceramic filters.

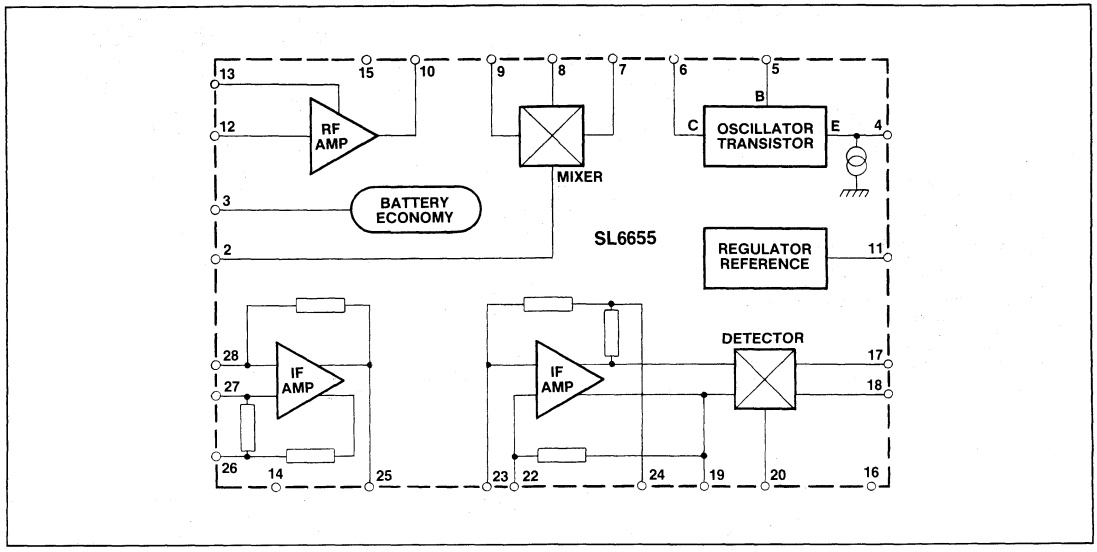


Fig.1 Block diagram. Pin numbers are identical for Quad Plastic J Lead (HP28) and Miniature Plastic DIL (MP28) packages. Refer to datasheet in Technical Data section for details.

THE SL6655 CONTAINS THE FOLLOWING BLOCKS

RF Amplifier

Input on pin 12, output on pin 10. The input is diode biased with a bias current of 50μA. The output is left open circuit allowing the gain to be selected externally.

Mixer

RF input on pin 9. LO input on pins 7 and 8 (however, the mixer is normally driven single ended with the remaining input biased at Vcc). Output on pin 2. The output resistance is 1.5kΩ.

Oscillator

This is a single transistor, base pin 5, collector pin 6 and emitter (connected internally to a 50μA current source), pin 4.

IF Amplifier 1

Input pin 27, output pin 28. Feedback and input bypass pins are 26 and 28 respectively.

IF Amplifier 2

Input pin 23, output for quadrature coil drive in on pin 19. Feedback and input bypass pins are 24 and 22 respectively. Both IF amplifiers have input impedances of 1.5kΩ.

Detector

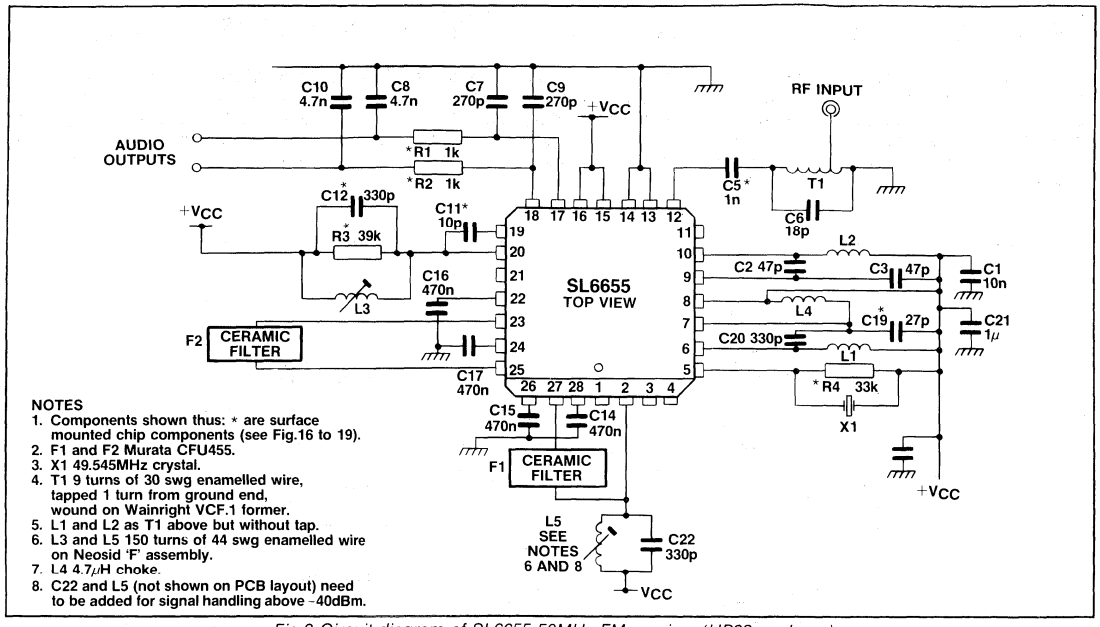
This is fed internally from the 2nd IF amplifier. The quadrature input is on pin 20 and is fed externally using a capacitor and phase shift network. The differential audio outputs are available on pins 17 and 18.

Regulator

The regulated output is on pin 11 and is supply independent and partially temperature compensated. It can source 6mA.

Battery Economy

Input pin 3. A logic low of <20% Vcc powers down the receiver.



NOTES
1. Components shown thus: * are surface mounted chip components (see Fig.16 to 19).
2. F1 and F2 Murata CFU455.
3. X1 49.545MHz crystal.
4. T1 9 turns of 30 swg enamelled wire, tapped 1 turn from ground end, wound on Wainright VCF.1 former.
5. L1 and L2 as T1 above but without tap.
6. L3 and L5 150 turns of 44 swg enamelled wire on Neosid 'F' assembly.
7. L4 4.7µH choke.
8. C22 and L5 (not shown on PCB layout) need to be added for signal handling above -40dBm.

Fig.2 Circuit diagram of SL6655 50MHz FM receiver (HP28 package)

A 50MHz FM RECEIVER (Fig.2)

A 50MHz frequency modulated signal is fed to the RF amplifier, which uses tapped tuned circuits to match the input and output, at the expense of spurious rejection. the input of the mixer by means of another π filter.

The local oscillator is a Colpitts design and uses a 49.545MHz 3rd overtone crystal. The collector load is a resonant circuit, tuned to 49.545MHz, and is capacitively tapped to match the output of the oscillator to the high impedance input of the mixer. The other input of the mixer is biased at Vcc, the bias for the input on pin 7 being obtained via an RF choke. A 455kHz tuned circuit identical to that used in the detector quadrature network is connected between the output of the mixer and Vcc, thus ensuring that the output transistor of the mixer does not saturate when large input signals are applied to the receiver. **NB** A resistor of 1.5kΩ connected between pin 4 and ground will bypass the oscillator current source. This will allow input signals as large as -5dBm to be applied to the receiver without stopping the oscillator and obviates the use of the tuned circuit at the output of the mixer.

The 455kHz output from the mixer is fed via a ceramic filter to one input of the 1st limiting IF amplifier, the remaining input is bypassed to ground via a 470nF capacitor. The input bias network is also bypassed via a 470nF capacitor.

The output from this first IF amplifier is fed via another 455kHz ceramic filter to one input of the 2nd IF limiting amplifier, the output of which is fed internally to the detector and via an external quadrature network to pin 20, which is the quadrature input of the detector.

The differential outputs of the detector are decoupled to ground via 270pF capacitors to remove the 455kHz component of the output and thence connected via RC low pass filter networks to the audio outputs. The regulator output is decoupled to ground with a 1µF capacitor, but is not used in this particular application. The receiver may be powered down by a logic low signal on pin 3. **NB** An alternative configuration for the RF amplifier is shown in Fig.3. This uses π networks to match the input and output. The use of the π network matching improves rejection of spurious signals of the form $fs \pm fosc = 455kHz$, but because of the low pass filter action, may degrade the response to signals of half the tuned frequency.

It is advised that this receiver is constructed on a double sided PCB, using, where possible, surface mounted components for economy of space.

Suitable PCB layouts are shown in Fig.4 (HP28 package) and Fig.5 (MP28 package).

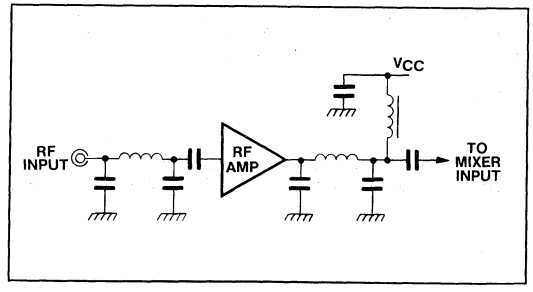


Fig.3 Alternative configuration for RF amplifier

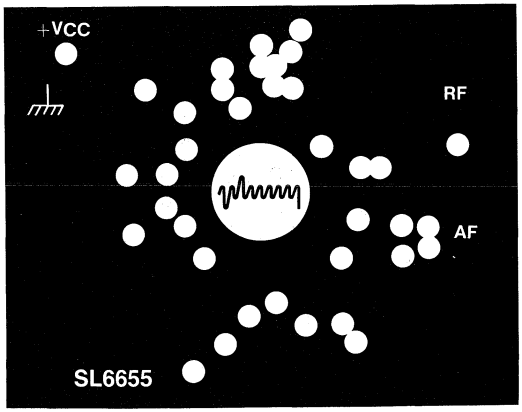


Fig.4a Ground plane (1:1)

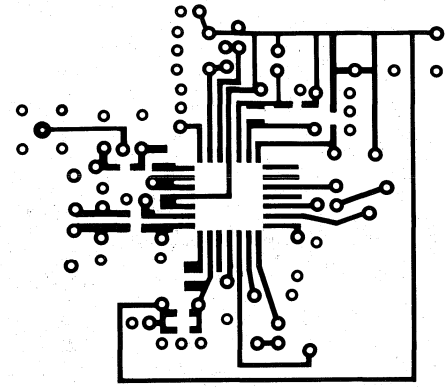


Fig.4b Copper track (1:1)

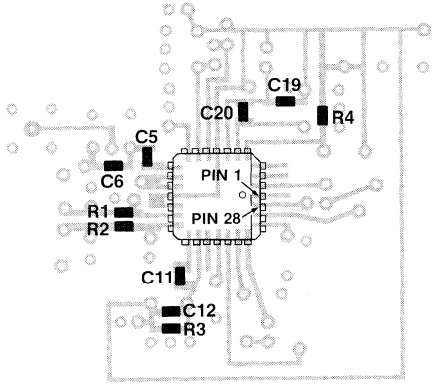


Fig.4c Surface mounted component overlay (1:1)

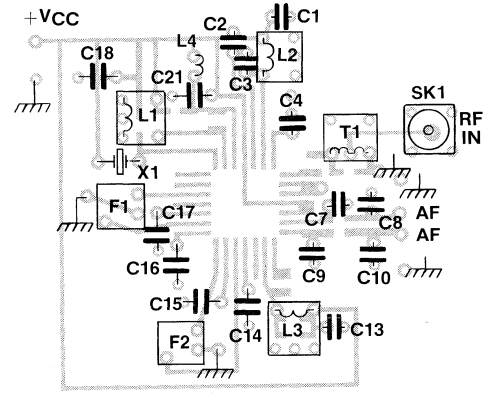


Fig.4d Component overlay (1:1)

Fig.4 SL6655 50MHz FM receiver PCB layout (HP28 package)

SL6655 Receiver Performance

Input signal 50MHz (Modulation = 1kHz with ±3kHz deviation).

Sensitivity	-119dBm for 12dB SINAD (V_{CC} = 1.3V)
	-113dBm for 12dB SINAD (V_{CC} = 0.9V)
Adjacent Channel Rejection	50dB (V_{CC} = 1.3V)
	68dB (V_{CC} = 0.9V)
Co-Channel Rejection	10dB (V_{CC} = 1.3V)
	9dB (V_{CC} = 0.9V)
3rd Harmonic Rejection	100dB (V_{CC} = 1.3V)
RF Amp 2nd Order Intercept	0dB
RF Amp 3rd Order Intercept	-14dBm
RF Amp Noise Figure	6dB
RF Amp 1dB Gain Compression	-16dBm
Mixer 3rd Order Intercept	-4dBm
Mixer 1dB Gain Compression	-14dBm
Audio Output Level	7mV (RMS)

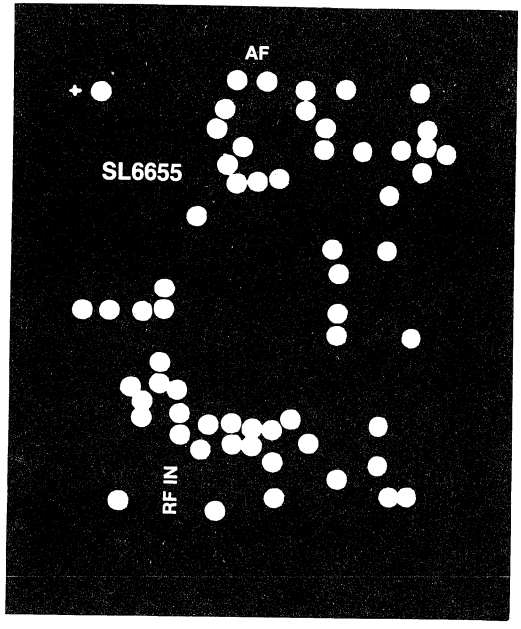


Fig.5a Ground plane

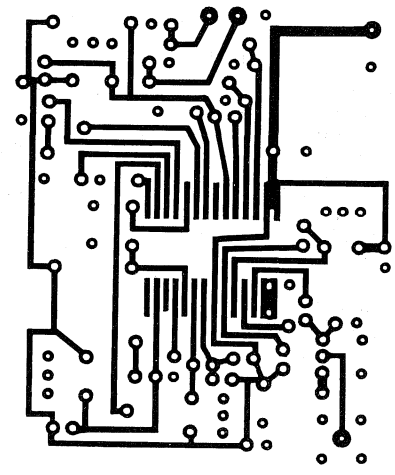


Fig.5b Copper track

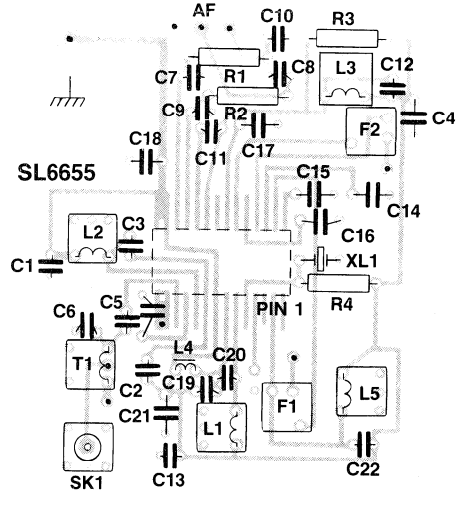


Fig.5c A component overlay (SL6655 in MP package surface mounted on track side of board)

Fig.5 SL6655 FM receiver PCB layout (MP28 package)

OPERATION AT HIGHER FREQUENCIES

It is possible to use the SL6655 at input frequencies of 150MHz and higher, with the modifications shown in Figs. 6 and 7.

Alternative Local Oscillator (Fig.6)

The current source on pin 4 is not used and is bypassed with a 1k resistor.

The 4.7μH choke between pins 7 and 8 is replaced by a 0.47μH choke.

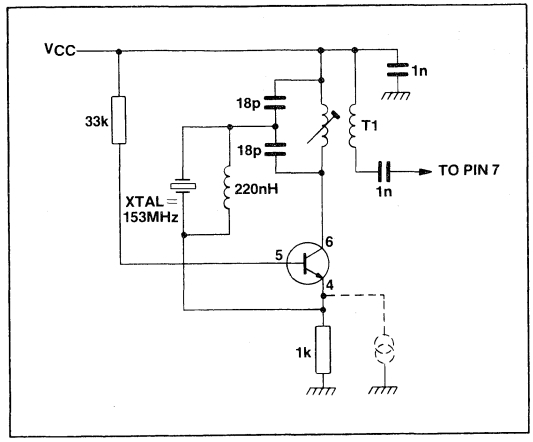


Fig.6

T1: Primary is 3 turns of 0.46mm diameter enamelled wire on 3.5mm diameter form. Secondary is 4 turns axially wound on same form.

Alternative RF Amplifier (Fig.7)

The RF amplifier is modified by using a tuned circuit resonant at 150MHz as the output load and π matching network at the input, as shown in Fig.6. The sensitivity of the SL6655 at 150MHz is 3μV for 12dB SINAD (V_{CC} = 1.3V).

A set of S-parameters are provided to facilitate further design of the RF amplifier (Figs. 8 to 11).

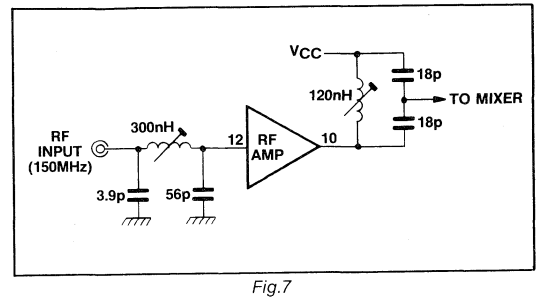


Fig.7

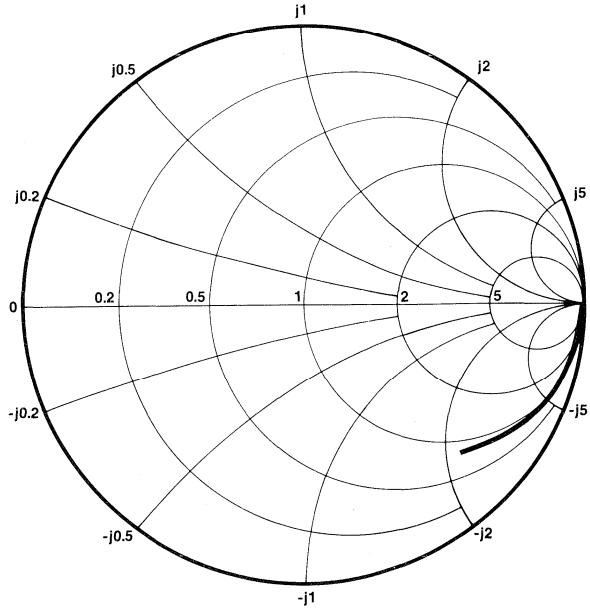


Fig.8 S_{11} (V_{CC} = 1.3V)

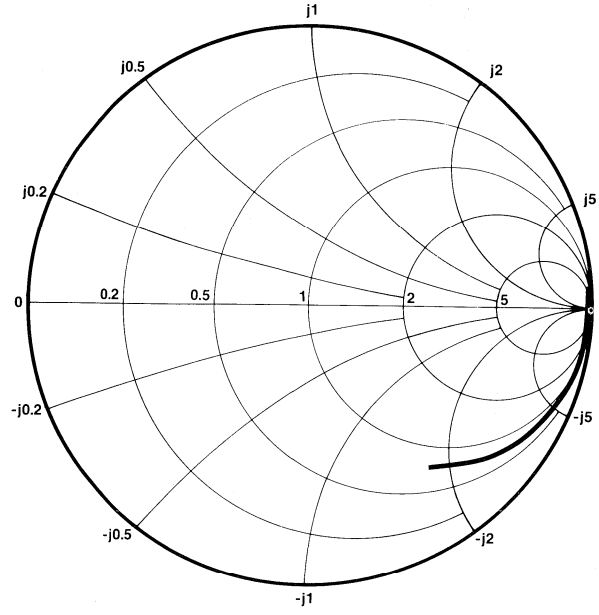


Fig.9 S_{12} (V_{CC} = 1.3V)

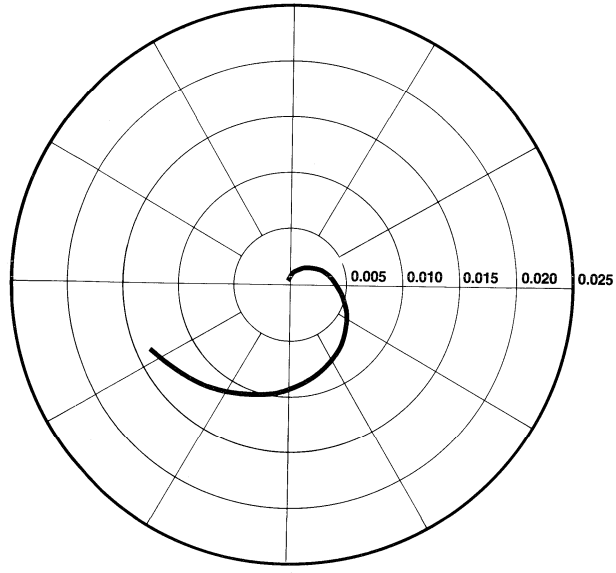


Fig.10 S_{21} (V_{CC} = 1.3V)

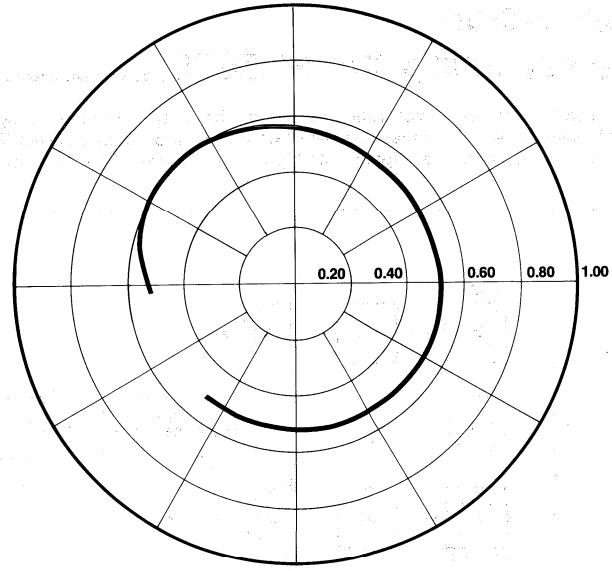


Fig.11 S_{22} (V_{CC} = 1.3V)

A Direct Conversion Paging Receiver using the SL6638

The SL6638 is a lower power direct conversion radio receiver for the reception of frequency shift keyed transmissions. It features the capabilities of 'power down' for battery conservation and control of an external DC-DC converter if single cell operation is required. The device also comes equipped with high current beeper drive and low battery flag indicator.

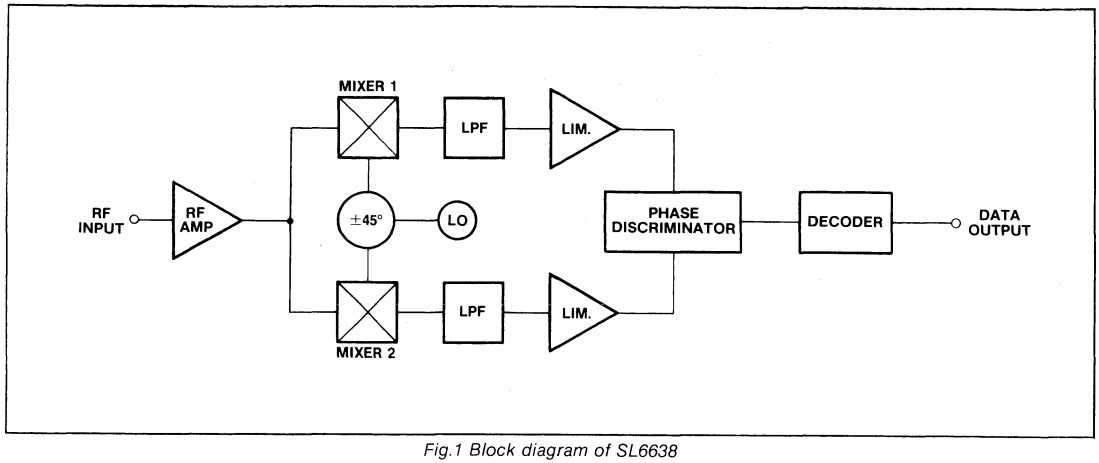


Fig.1 Block diagram of SL6638

PRINCIPLE OF OPERATION

The incoming signal is split into two parts and frequency-converted to base band. The two paths are produced in phase quadrature (see Fig.1) and detected in a phase detector which provides a digital output. The quadrature network may be in either the signal path or the local oscillator path.

The input to the system is an FSK data modulated signal with a modulation index of 18. This gives a spectrum as in Fig.2. f_1 and f_0 represent the 'steady state' frequencies (i.e. modulated with continuous '1' and '0' respectively). The spectrum in Fig.2 is for reversals (a 0-1-0-1-0-1 etc. pattern) at the system bit rate; f_c is the nominal carrier frequency.

When the LO is at the nominal carrier frequency, then a continuous '0' or '1' will produce an audio frequency, at the output of the mixers corresponding to the difference between f_0 and f_c or f_1 and f_c. If the LO is precisely at f_c, then the resultant output signal will be at the same frequency regardless of the data state; nevertheless, the relative phases of the two paths will reverse between '0' and '1' states.

By applying the amplified outputs of the mixers to a phase discriminator, therefore, the digital data is reproduced.

If the waveform at limiter '1' input leads the waveform at the limiter '2' input by 90°, output at detector output will be a high level and low at the Data Output.

If the waveform at limiter '1' input lags the waveform at the limiter '2' input by 90°, output at the detector output will be a low level and high at the Data Output.

The receiver design described in this application uses mainly surface mounted components and employs a ferrite antenna for maximum sensitivity and compactness. The receiver requires two supplies, $V_{CC}1$ and $V_{CC}2$ of 1.3V and 2.2V respectively. Single cell operation is possible using an inverter, a suitable circuit is shown in Fig.9. Alternatively $V_{CC}1$ may be derived from $V_{CC}2$, but $V_{CC}1$ must be at least 1 diode volt-drop down from $V_{CC}2$.

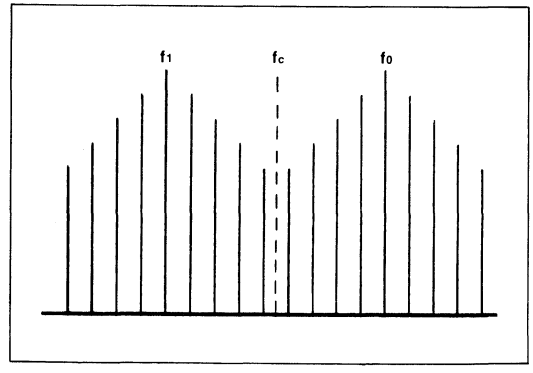


Fig.2 Spectrum diagram

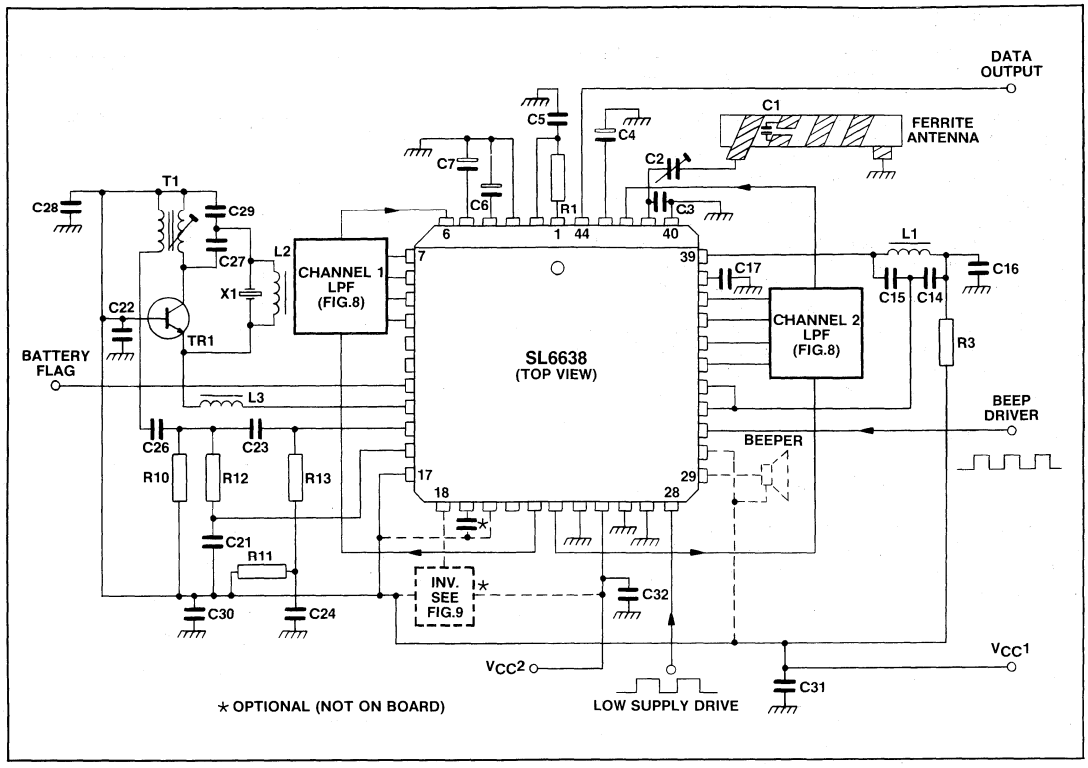


Fig.3 SL6638 applications circuit

R1	220k	C1	8.2p	C21	8.2p	IC1	SL6638
R2	15k	C2	2-10p	C22	1n		
R3	100	C3	22p	C23	8.2p	L1	3 turns of 0.45 dia.
R4	39k	C4	10μ	C24	1n		enamelled wire on 3.5mm
R5	22k	C5	1n	C26	22n		dia. form (available from
R6	2.7k	C6	10μ	C26	1n		Wainwright Instruments,
R7	22k	C7	10μ	C27	15p		type VCF-1)
R8	15k//180k	C8	8.2n (5%)	C28	1n		
R9	6.8k//100k	C9	2.2n (5%)	C29	22p	L2	220nH choke
R10	100	C10	2.2n	C30	1n		
R11	100	C11	1.2n	C31	1μ	L3	10μH choke
R12	100	C12	2.2n	C32	1μ		
R13	100	C13	2.2n (5%)	C33	10n (5%)	T1	as L1 but with an
R14	6.8k//100k	C14	27p	C34	8.2n (5%)		axial winding of 4 turns
R15	22k	C15	8.2p	C35	22n		
R16	15k//180k	C16	1n	C36	180 (5%)	X1	153MHz 7th/9th
R17	2.7k	C17	1n	C37	1.2n		overtone crystal
R18	22k	C18	470 (5%)	C38	470p (5%)		
R19	39k	C19	180 (5%)				
R20	15k	C20	10n (5%)	TR1	BFY90		

Table 1 Component values for Fig.3

CIRCUIT DESCRIPTION See Figs.1 and 3

The RF input, which is an FSK signal, is applied to the RF amplifier, and from the output of this stage to the mixers. The local oscillator inputs of these mixers are driven in phase quadrature from the crystal controlled oscillator, phase shift being produced by a resistor-capacitor network. The frequency of the local oscillator is equal to the nominal carrier frequency, and the mixer outputs at baseband are filtered in the active filters, which provide selectivity. In theory, a receiver using 'zero IF' has infinite adjacent channel rejection. The AF outputs of the LPF's are in turn fed to the inputs of two limiting amplifiers which provide most of the receiver gain, and the outputs of which feed the detector. This consists of a number of phase detectors arranged to provide phase comparison on four pairs of signal edges, thus maximising sensitivity. The detected output is now filtered in the Bit Rate Filter, and applied to a further limiter, providing the received data at the output.

The RF Amplifier

This is a single NPN transistor whose bias is provided internally and whose terminals are available on pins 39, 40 and 41.

There is a collector tuned load and the input tuned circuit consists of the ferrite antenna and capacitors C2 and C3//Ci.

The ferrite antenna (Fig.6(a)) consists of a length of F29 ferrite rod on which is wound four turns of 0.2in copper tape. The tape is cut near the centre of the coil and an 8.2pF ceramic capacitor inserted. This capacitor effectively reduces the inductance of the coil allowing more turns to be used thus increasing the efficiency of the antenna.

The input circuit is shown in Fig.6(b). It will be seen that the antenna is resonated with the series combination of C2 and C3 in parallel with the input capacitance of the device. The resultant capacitive tap provides a 10:1 impedance transformation, thus keeping the Q of the tuned circuit fairly high.

A set of 'S' parameters is included (see Fig.15) to facilitate the optimum design of input and output networks for the RF amplifier.

The Mixers and Quadrature Network

The two mixers are fed with local oscillator energy via an RC network which provides 90° phase shift between the two LO inputs on pins 15 and 16. The signal inputs are on pins 33 and 32 respectively and the mixer outputs are on pins 23 and 22.

It is also possible to include the quadrature network in the RF signal path in which case pins 15 and 16 are fed directly from the LO.

A plot of S_{11} measurements is included to enable optimum matching of the quadrature network to pins 15 and 16 (see Fig.16).

The RC network employed in this application is shown in Fig.4.

The Local Oscillator

The circuit employed in this application uses a BFY90 transistor and a 7th or 9th overtone crystal and is illustrated in Fig.5. The 220nH inductor L2 in parallel with the crystal suppresses oscillation at the crystal fundamental.

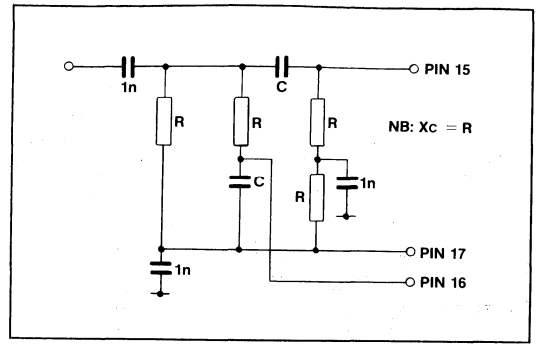


Fig.4

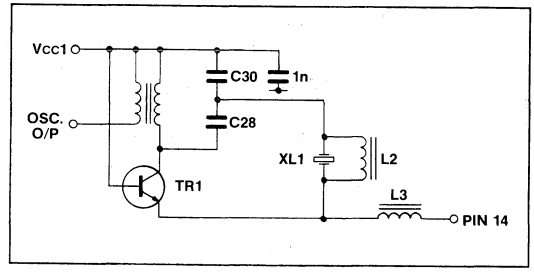


Fig.5

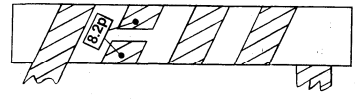


Fig.6(a) Construction

Antenna design by courtesy of Multitone Electronics plc, UK Patent No. 2110851B.

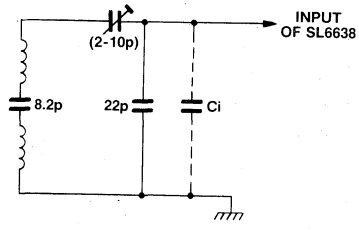


Fig.6(b) Antenna circuit

Fig.6 Ferrite antenna details

The Active Filters

These are 4-pole low-pass filters utilising the high gain inverting amplifier and the unity gain emitter follower available on the device. These amplifiers are configured as a multiple feedback LP filter and a Salen and Key LP filter respectively. There are two passive RC networks which provide a further two poles.

The following equations may be used to design the filters.

MFB low pass filter (Fig.7(a))

1. Select C_1 and C_2 such that $C_2 = 10/fc\ \mu F$ and $C_1 =$ or $C_{2/2}$ $(K + 1)$ where K is the required gain.

2. Resistance values are found by:

$$R_2 = \frac{2(K+1)}{\left[\sqrt{2C_2} + \sqrt{2C_2^2 - 4C_1C_2(K+1)}\right]\omega_c}$$

$$R_1 = R_2/K$$

$$R_3 = \frac{1}{C_1C_2\omega_c^2R_2}$$

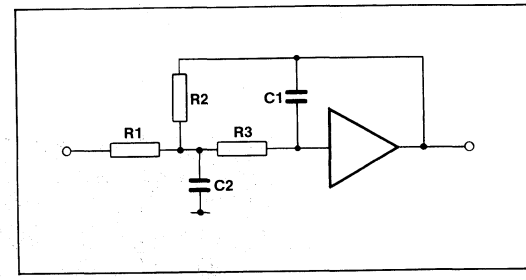


Fig.7(a)

Salen & Key low pass filter (Fig.7(b))

1. Select $C_2 = 10/fc\ \mu F$ and $C_1 = C_{2/2}$.

2. Resistance values are found by:

$$R_1 = \frac{2}{\left[\sqrt{2C_2} + \sqrt{2C_2^2 - 8C_1C_2}\right]\omega_c}$$

$$R_2 = \frac{1}{C_1C_2R_1\omega_c^2}$$

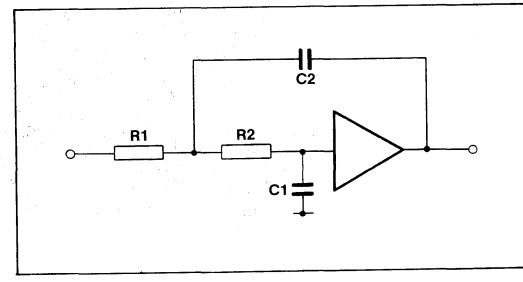


Fig.7(b)

RC single pole filter (Fig.6(c))

$C = 10/fc\ \mu F$

$R = 1/\omega_c C$

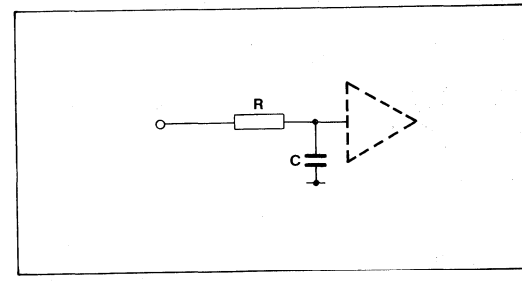


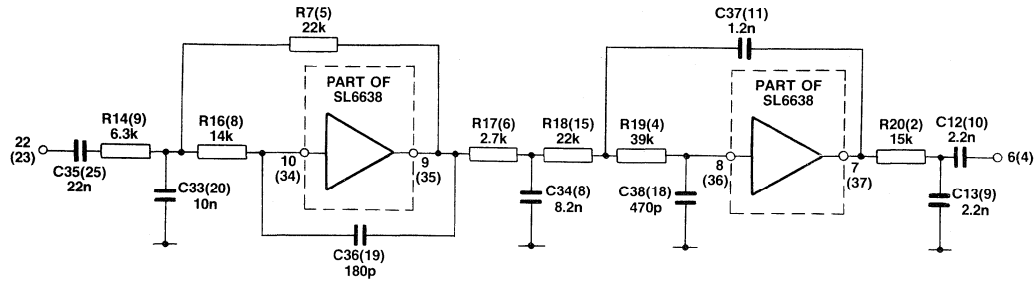
Fig.7(c)

NB. These equations are for 2nd order Butterworth LP filters.

The actual component values used in this application and a plot of the frequency response are illustrated in Fig.8.

The filters provide an adjacent channel rejection of 70dB at 25kHz separation with a 250Hz square wave modulated signal at 4.5kHz deviation.

It is possible to obtain similar performance at 12.5kHz separation with 2kHz deviation if all capacitance values shown above are doubled.



NB: ALL CAPACITOR VALUES ARE ±5% EXCEPT COUPLING CAPACITORS

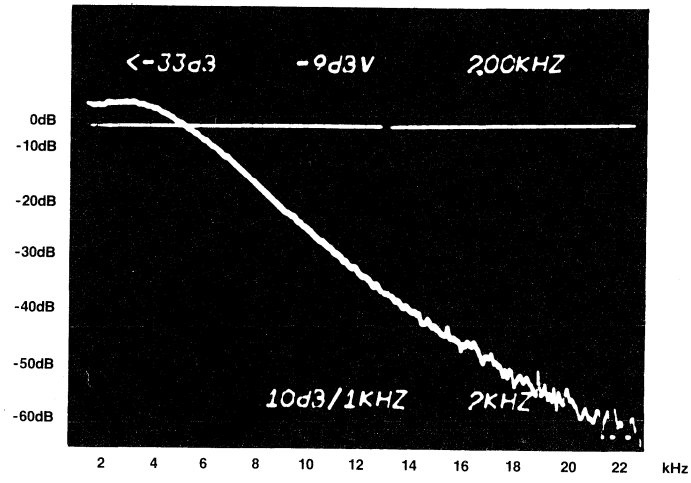


Fig.8 Active filter component values and frequency response for SL6638 DC pager

Limiting Amplifiers and Phase Discriminator

The limiting amplifiers limit with inputs of about 6μV on pins 6 and 42. Pins 4,5 and 43 are bypassed to ground by 10μF capacitors.

The outputs of the limiting amplifiers go directly to the phase discriminator and are not accessible externally. The discriminator output is at pin 1.

Decoder

This is a limiting amplifier which is internally slew-rate limited to prevent fast output edges being radiated back to the antenna.

The connection of a 1nF capacitor from pin 2 to ground is adequate as a LPF to the modulation frequency.

A 220kΩ resistor is connected between pin 1 and pin 2 to suppress feedback. The data output is available at pin 44.

Inverter Circuit

This inverter is used to provide $V_{CC}2$ which is 2.3V from a single supply $V_{CC}1$ which is 1.3V.

The inverter control output on pin 18 is derived from the ratio of the internal reference to the $V_{CC}2$ line and moves in phase with changes in the $V_{CC}2$ line. Pin 21 allows the value of $V_{CC}2$ to be adjusted.

Pin 13 is a battery flag which is activated when $V_{CC}1$ falls below about 1V. The inverter circuit is shown in Fig.9.

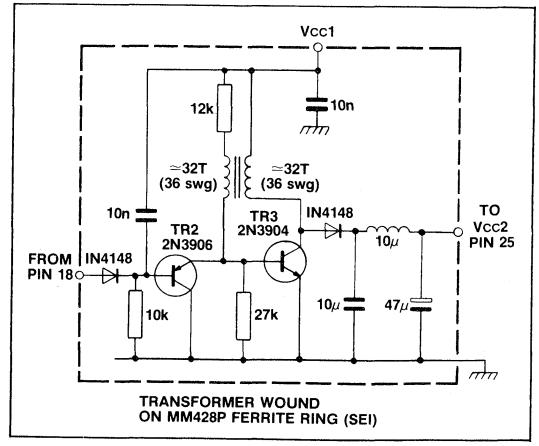


Fig.9 Inverter circuit for SL6638 pager

Beeper Drive

This stage accepts an input from an external source and provides a high current drive to the beeper. This current drive can be as high as 200mA and the arrangement is such that the output waveform may be modified when the battery is low. This modified waveform is generated externally and applied to pin 28. When the battery is low pin 28 will override the beep input on pin 31. A logic high will remove beep drive and a logic low will connect beep drive.

The internal band-vap reference is 1.2V and this is divided down to a suitable voltage.

An internal diode connects pin 29 to pin 30 to protect the driver transistor when used with inductive loads.

Battery Economy

The following functions will have their bias removed during power down (high on pin 24):

RF amplifier
Oscillator current sources
Mixers
Active filters
Phase discriminator
Bit-rate filter and decoder

RECEIVER PERFORMANCE

The performance of the paper circuit is measured using a quasi bit-error detector which is illustrated schematically in Fig.10. Errors on the +ve or -ve half cycles of the recovered data (depending on the setting of SW1) are examined.

A reading of 8Hz on the frequency counter corresponds to a bit-error rate (b.e.r.) of 1 in 30. The sensitivity at a b.e.r. of 1 in 30 with a square wave modulated signal and a deviation of 4.5kHz is of the order of 10μV/m.

Adjacent channel rejection = 70dB (for 6dB degradation 25kHz separation)
Co-channel rejection = 1dB (wanted signal 6dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 12dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 0dB (wanted signal 20dB above level for 1 in 30 b.e.r.)
Co-channel rejection = 1dB (wanted signal 30dB above level for 1 in 30 b.e.r.)
3rd order input intercept = -6.5dBm

The above measurements are all made using a wanted signal of 153MHz modulated by a 250Hz square wave at a deviation of ±4.5kHz

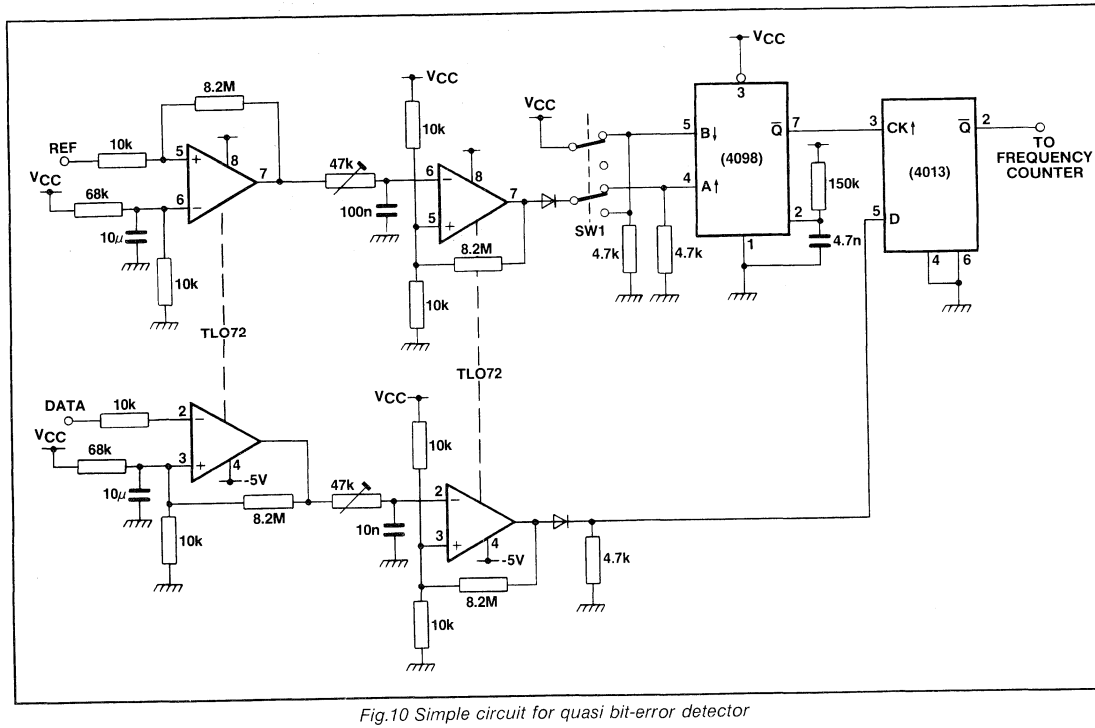


Fig.10 Simple circuit for quasi bit-error detector

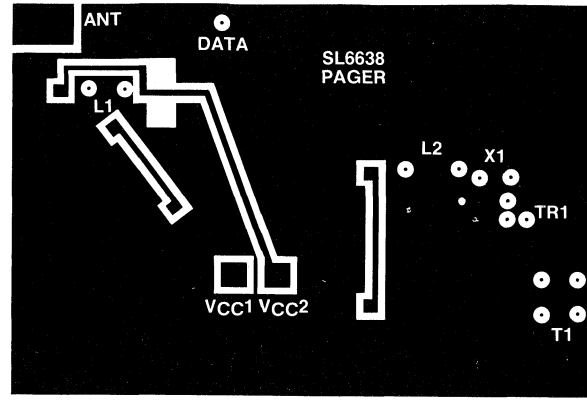


Fig.11 PCB ground plane (1:1)

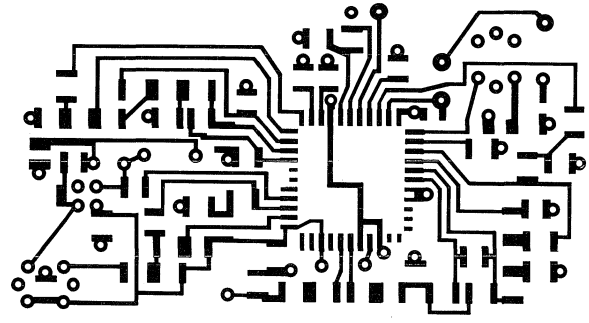


Fig.12 PCB track side (1:1)

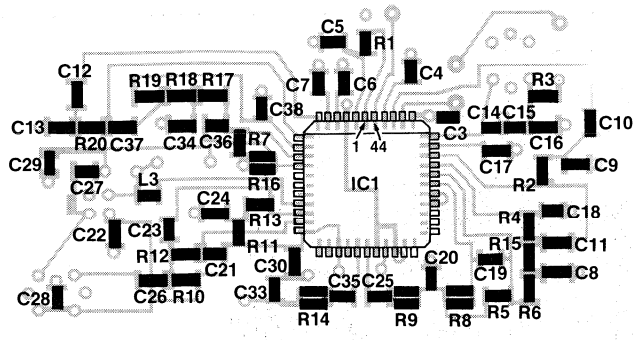


Fig.13 PCB surface mounted component overlay (1:1)
NOTE: R8, R9, R14 and R16 each comprise two chip resistors connected in parallel (see Table 1)

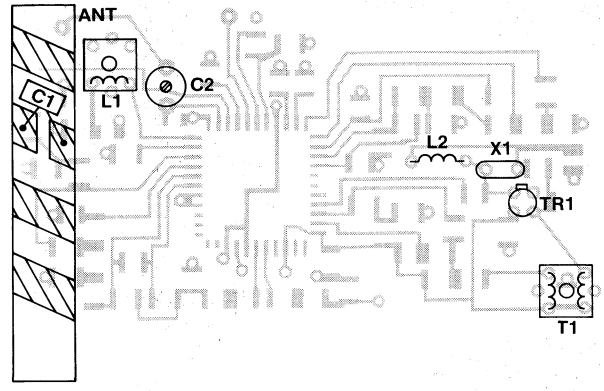


Fig.14 PCB component layout for ground plane side (1:1)

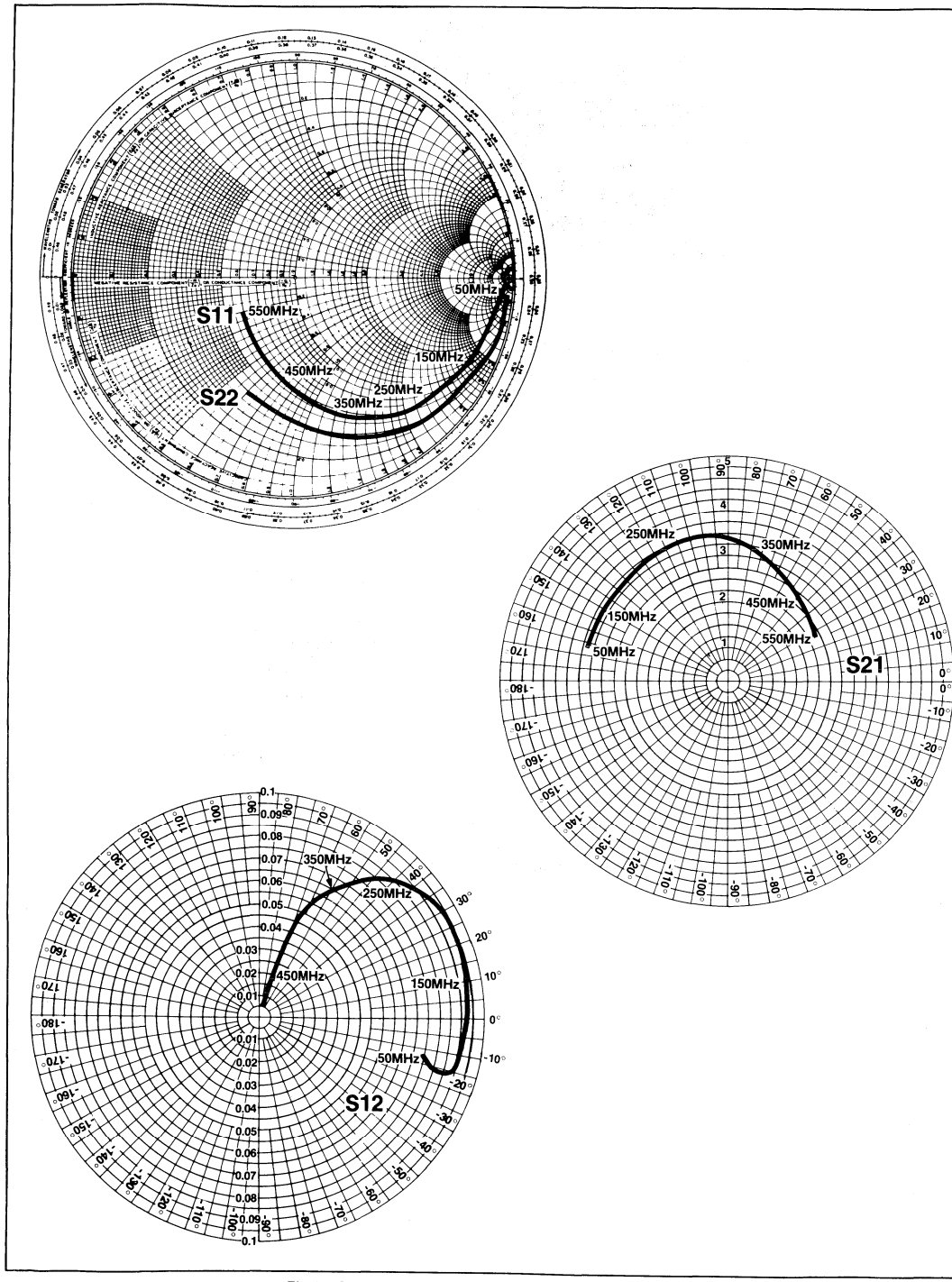


Fig.15 'S' parameters for the RF amplifier of the SL6638S

SL6700 — A Versatile Radio Integrated Circuit

The SL6700 is designed for use in low voltage AM applications. However, its versatility and access to internal functional blocks allows its use in many more applications. The original use of this circuit required the incorporation of a specialised noise blanker, which is still present, and may be used if desired. The low power consumption (<60mW) of this circuit makes it ideal for a number of applications, while its design, optimised for use with ceramic filters, allows lower cost circuitry to be obtained.

The SL6700 block diagram is shown in Fig.1. The IC contains the following functions:

Amplifier 1, input on pin 18 and output on pin 3. This amplifier is AGC controlled.

Amplifier 2, input on pin 3 and output on pin 5. This amplifier is also AGC controlled, but has a lower signal handling capacity than amplifier number 1.

Double balanced mixer, input on pin 7, oscillator on pin 9 and output on pin 8. The output is an open collector, and the mixer has a 3rd order intermodulation intercept point of about -9dBm.

Monostable multivibrator, used for the noise blanker, connected to pins 11 and 12.

Amplifier and detector, input on pin 13, with AF output on pin 15.

AGC amplifier with delayed output, output on pin 5.

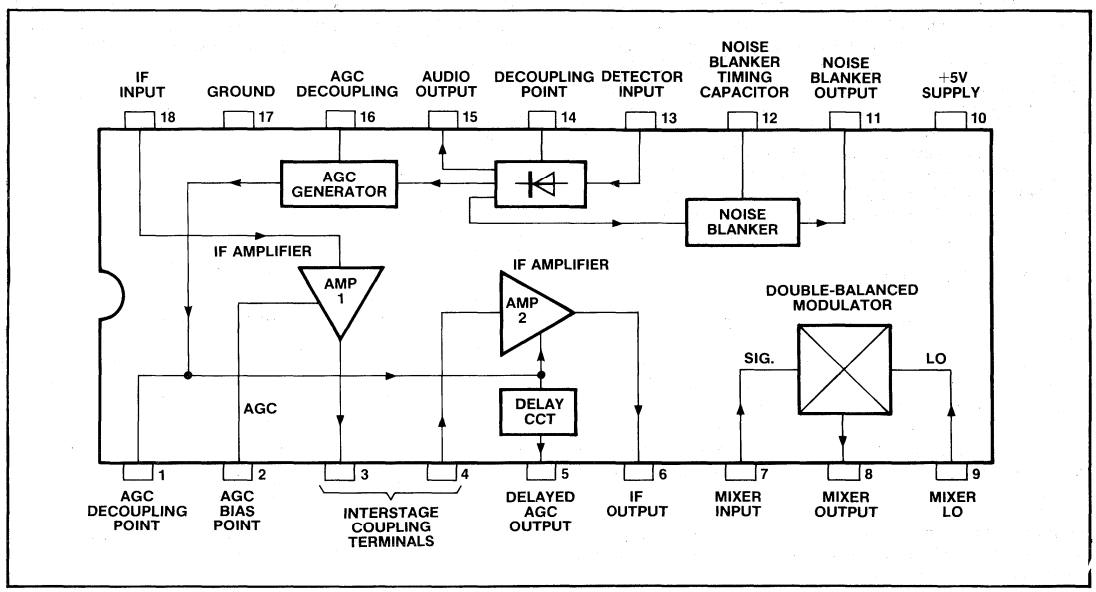


Fig.1 SL6700 block diagram

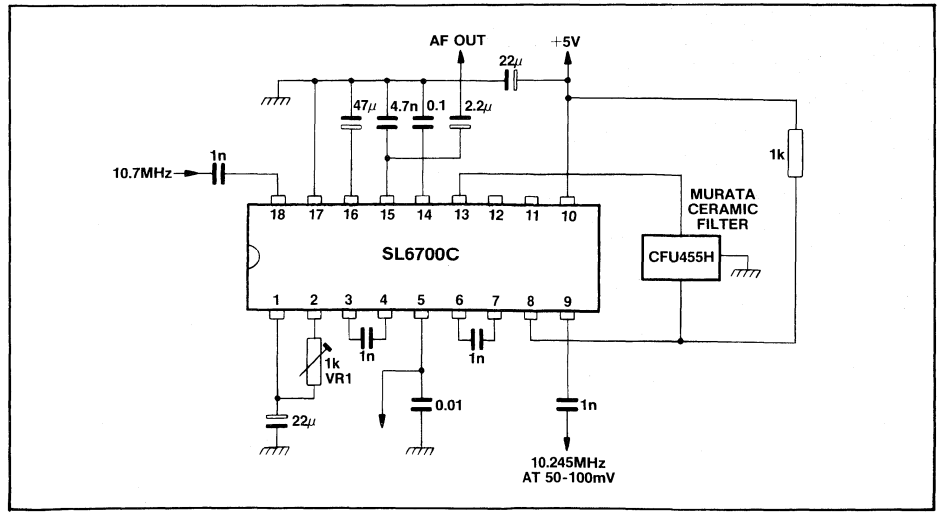


Fig.2 Double conversion IF strip 10.7MHz and 455kHz

DOUBLE CONVERSION IF STRIP (Fig.2)

The 10.7MHz input is amplified in both IF amplifiers and converted to 455kHz in the mixer. The 455kHz output is filtered in a ceramic filter, and applied to the detector input. AGC is applied to the two amplifier stages, and the 1kΩ variable resistor, RV1, is used to set the delayed AGC threshold level. This AGC output is positive going with increasing signal, and reaches a sufficient voltage to control the Plessey SL600 and SL1600 series amplifier devices.

The sensitivity of this circuit is typically 5μV RMS, with 30% modulation for a 10dB signal to noise ratio, and it will accept signals up to 100mV RMS at 80% modulation with distortion below 5%.

The frequency response of the AGC controlled amplifiers extends up to 25MHz, allowing a wide choice of IF to suit any particular requirement.

The type of detector used in the SL6700C has the great advantage of producing carrier-derived AGC. It is a full wave detector (see Fig.3) in which the input signal is an emitter coupled transistor pair with common collectors (TR53 and TR54), and the signal, phase inverted by TR50 and TR52, to the other input. TR53 and TR54 act as a full wave rectifier, and the emitters rise to a voltage determined by the input. The modulation also appears on the emitters, and is fed out via pin 15, whle a further transistor, with suitable filtering, provides the AGC voltage. The detector is extremely linear - for example, the increase in audio output from 30% to 80% modulation is 8dB, against a theoretical rise of 8.52dB.

AM BROADCAST RADIO (Fig.4)

The SL6700C is ideally suited for this application. Its high linearity and low distortion allow quality reproduction of AM broadcast signals, while the minimum of external components allows small size and low cost. TR1 is the oscillator transistor: almost any small signal NPN device will function.

C1, L1 and C2, L2 are proportioned to track - L1 may, of course, be a ferrite road aerial. The values of C1, L1, C2, L2 and C3 may be determined from any of the standard formulae (Refs. 1,2,3,4).

Where minimum component count is necessary, and degradation of selectivity may be accepted, the filter F2 may be replaced with a 100pF capacitor. Similarly, R1 and C2 may be omitted where a well-filtered supply line is available.

The input impedance of the mixer is typically 300Ω, allowing a tight coupling to the coil L1 without excessive loss of Q, which is an important consideration when using ferrite rod aerials.

The delayed AGC line is not used in this receiver and is left disconnected. However, should it be desired to produce a broadcast receiver covering the SW broadcast bands, the addition of an SL1610C RF amplifier will improve the sensitivity by a useful amount, while an extra tuned circuit will be given extra image rejection. Under these circumstances the 22kΩ resistor from pin 1 to ground should be omitted, and a 1kΩ potentiometer connected between pins 1 and 2 as in Fig.2. In the majority of cases, a 330Ω resistor will provide a suitable AGC characteristic, if some variation between ICs is not objectionable. The low supply voltage and current requirements make this ideal for portable applications.

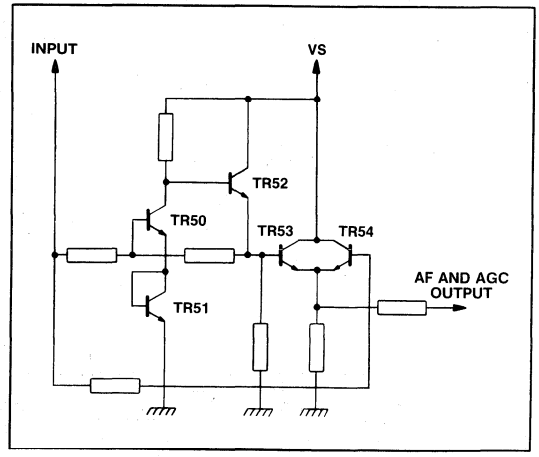


Fig.3 AM detector

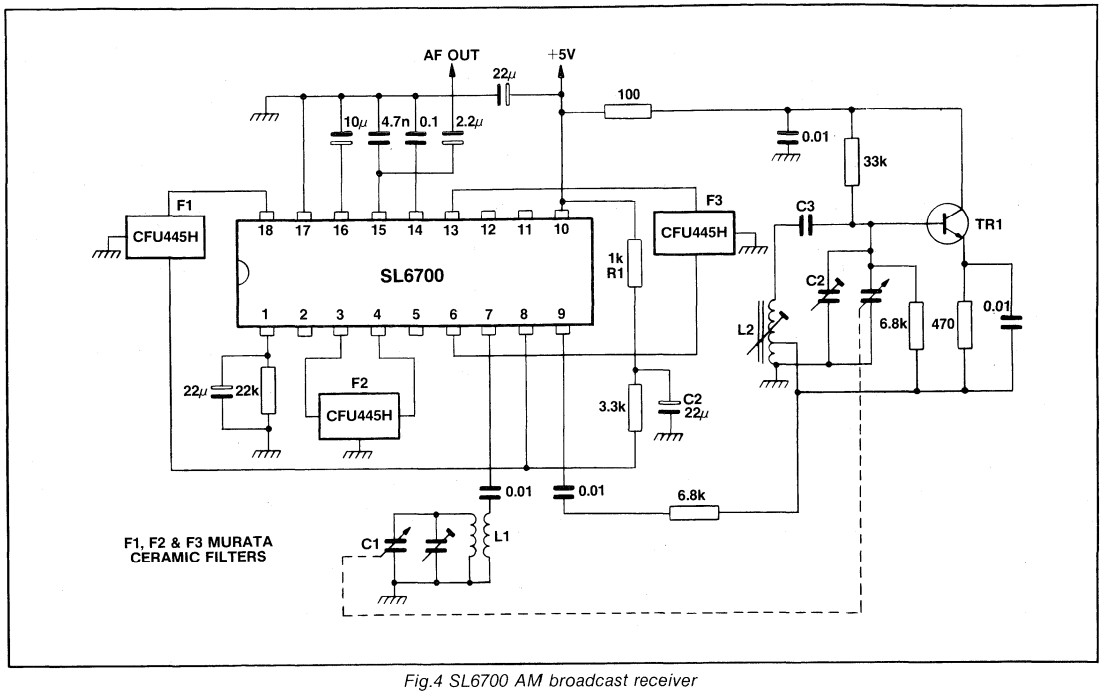


Fig.4 SL6700 AM broadcast receiver

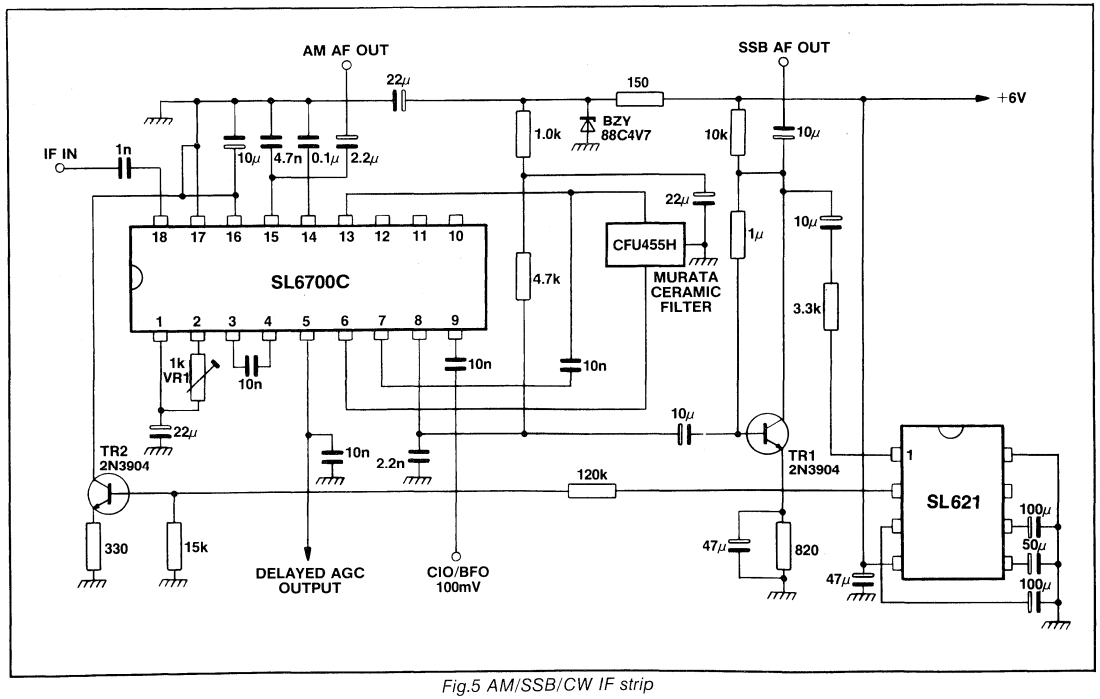


Fig.5 AM/SSB/CW IF strip

AM/SSB/CW IF STRIP (Fig.5)

This is one of the more complex applications of the SL6700C. The two gain controlled amplifiers are cascaded, and feed, via a band limiting filter, the detector and AGC circuits, and the input of the mixer, which is used as a product detector. Although a ceramic filter is shown in Fig.5, a suitable tuned circuit may be used. The load appearing across the circuit is low (1.5kΩ) and to obtain a suitable Q, it may be necessary to tap down the circuit, either by means of capacitive or inductive taps.

Because of the limited frequency response of the detector and the amplifier feeding it, this circuit is not recommended for use above 1.6MHz.

The audio output from the product detector is amplified in TR1, and the output applied to the input of an SL621 AGC generator. The output of this stage controls the internal AGC circuitry via TR2. For AM operation, the carrier insertion oscillator (or BFO for CW) is switched OFF, and as a result, there is little output from the product detector. The AM detector and AGC thus work normally, while the SL621 provides no output. In the SSB/CW modes, the product detector output activates the SL621, and the AGC is 'taken over' by this stage. However, RF derived AGC is still applied in the event of strong signals at zero beat. R1 was chosen to set the outputs on AM and SSB approximately equal for single SSB and 80% modulated AM signals respectively.

Although selectivity will usually be obtained by means of block filters, it often happens that provision of a multi-element filter for CW reception is not viable, although some narrowing of the passband from the SSB condition is required.

Under these conditions, a useful narrowing of the passband can be obtained by replacing the capacitor between pins 3 and 4 with a suitable selective network, such as Fig.6. With a quartz crystal, this gives a very narrow peak to the passband, and the use of a single ceramic resonator may be preferred (at 455kHz). At 1.4MHz or 1.6MHz, the 2200pF capacitor should be reduced to around 470pF, and the response will be less sharp then at 455kHz, but will still be found to be adequately narrow.

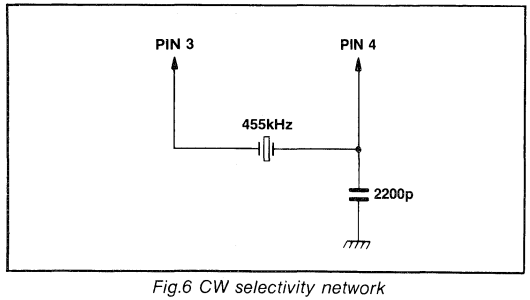


Fig.6 CW selectivity network

The AM and SSB outputs should be kept completely separate, and should be switch selected. During AM reception, the BFO/CIO must be switched OFF to avoid heterodyne interference and production of audio derived AGC. For CW reception only the circuit in Fig.9 may be used. The SL621C is designed for use as a fast attack SSB AGC generator, and, because of the large capacitors used, draws a large transient current from the supply when an SSB signal is first applied. To avoid instability, pin 4 of this device, the supply pin should be decoupled by a 47μF capacitor with short leads. In this connection, it must be remembered that a capacitor mounted on a PCB with long, thin tracks connected to it may have an appreciable increase in its ESR (Equivalent Series Resistance). The decoupling of the product detector output load (1kΩ and 47μF connected to the 4.7kΩ load at pin 6) gives an appreciable reduction in supply line noise, and should not be omitted.

The SL6700 has, unlike some ICs attempting to offer similar facilities proved remarkably 'tame', and provided sensible layouts and grounding are attained, should not give any problems with instability. In fact, attempts to use one of the amplifiers as an oscillator have proved rather fruitless - unusual phenomena to many IC users.

Nevertheless, under some conditions, the SL6700 may give the impression of instability at low signal levels. This manifests itself as a heterodyne whistle at low inputs, typically around 5μV. This is caused by some samples of the ceramic filter from pin 6 to 13 appearing to ring, and substitution of a tapped tuned circuit obviates these problems.

The performance of the AM/SSB/CW strip is set out in Table 1. The ultimate signal to noise ratio on SSB is not exceptionally high, but is adequate for all except the highest grade of point-to-point, independent sideband type communications. Intermodulation products were typically at -30dB representing 3% distortion, and are thus better than those of most received transmissions.

For designers of battery operated equipments, the low power requirements of the SL6700/SL621 combination (typically 90mW), combined with the small size and simplicity of use, after an attractive method of obtaining high performance.

SSB GENERATOR (Fig.7)

This is perhaps the most unusual application for a device designed for use in receivers. It is possible to obtain simple circuits offering adequate quality SSB, with no adjustments - a time consuming and expensive part of production. Indeed, it is considered that in many companies, the real cost of a trimming potentiometer is £2 - £3 ($4 - $6) when consideration is given to the real cost of adjustment by skilled testers.

Parameter	AM mode	SSB mode	Notes
Sensitivity	7dB SND/ND 15dB SND/ND	15dB SND/ND	5μV RMS input,m = 0.3 5μV RMS input, m = 0.8
AF output	42mV RMS -	- 43mV RMS	5μV RMS input, m = 0.8, fm = 1kHz f audio 1kHz
AGC	4dB	5dB	Change in AF output from 5μV to 100mV RMS input
Distortion	2.8 %	- 4.2 %	V_{IN} = 100mV RMS, m = 0.8 at 1kHz V_{IN} = 100mV RMS, f_{OUT} = 1kHz
Signal-Noise Ratio at higher inputs	28dB 36dB -	- - 35dB	V_{IN} 50μV, m = 0.3 V_{IN} = 50μV, m = 0.8 V_{IN} = 50μV, f_{OUT} = 1kHz
Ultimate Signal to Noise ratio	50dB	40dB	V_{IN} = 100mV RMS

Table 1 Results obtained from Fig.5

The SL6270 is a Voice Operated Gain Adjusting Device (VOGAD) which maintains a constant output level for a wide range of inputs. The input may be fed differentially, if desired, by removing the 2.2μF capacitor from pin 5 and feeding between pins 4 and 5. The usual precautions should be taken against RF pickup in transmitter, and bypass capacitors of 10nF should be provided on the inputs.

The mixer of the SL6700 is used as a balanced modulator, giving some 20dB of carrier suppression. The SSB filter gives another 20-25dB to produce an acceptable signal. (-40dB relative to each tone, -46dB rel. PEP is the usual professional standard). Rt and Ct are the termination components for the filter and should be chosen accordingly. However, impedances in the range 1-4kΩ are preferred. Less than 1kΩ gives greater loss in the balanced modulator, thus degrading carrier suppression, and more than 4kΩ needs other techniques to maintain the DC feed to the mixer. However, filters at 455kHz such as the Collins 526-9939-010, with Rf at 2.7kΩ and Ct at 360pF give very good results - see Table 2. At 1.4MHz, stray capacitances make the carrier leak somewhat worse, but still usable. Suitable filters at this frequency are the Cathodeon BP4707/BP4708, which require values of Rt = 1kΩ and Ct = 15pF. At 1.4MHz, it may prove useful to connect a 6.8kΩ resistor in series with pin 18 of the SL6700, breaking a ground loop through the low Z22 of the filter, minimising degradation of the carrier suppression.

The value of R1 should be set at the design stage. This resistor controls the input to the detector stage, and thus the amount of AGC produced, so setting the gain of the first amplifier. The value of this resistor sets the ALC threshold, and values vary from 47kΩ at 1.4MHz to 120kΩ at 455kHz, depending on the desired output and amount of ALC required. An additional ALC input is available at pin 13: feeding in an ALC voltage derived from later in the transmitter via a suitable resistor will give a multiple level ALC action. The 47μF capacitor from pin 15 sets the ALC time constant, and should not be reduced: otherwise distortion will introduced. The 1kΩ resistor from pin 3 to ground increases the current through the emitter follower driving this pin, and allows an undistorted output to be obtained in as low an impedance as 50Ω.

For transceiver use, the switching required between receive and transmit is probably too complex to be economical, and the use of two SL6700s with a switched filter is recommended.

Typical results are shown in Table 2.

Parameter	455kHz	1.4MHz	Notes
Carrier Suppression	50dB	46dB	Relative PEP
3rd order IMD	-40dB	-40dB	Relative each tone of a 2 tone signal, with separations down to 50Hz.
2nd order IMD	-43dB	-38dB	as 3rd order
Output Level	200mV pk-pk	200mV pk-pk	Into 600Ω load
Carrier Level	50mV	50mV	RMS
Audio Level	30mV	30mV	RMS input to SL6700 pin 7

Table 2 Results of the SSB generator in Fig.7

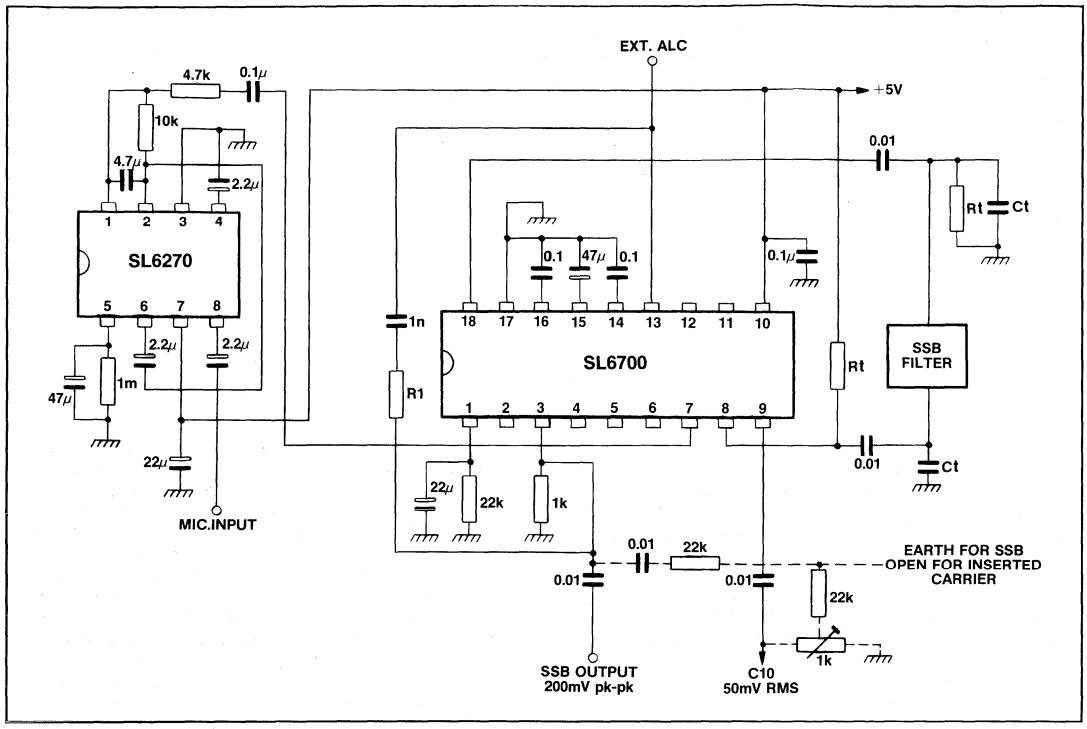


Fig.7 SL6700 SSB generator

Shown dotted in Fig.7 is a means of re-inserting carrier for A1A, J2H, J3A or J3H operation. The level of the carrier is set by the potentiometer: however, care should be exercised in the return from the carrier switch to avoid earth loop currents. For J3H operation, it is recommended that the carrier be set between -4 and -5dB rel. PEP to avoid excessive distortion at modulation peaks. To obviate carrier 'pumping' (carrier level being dependent on AF level) no more than 2 or 3dB of ALC should be used.

Use of this circuit above 1.6MHz requires care for several reasons. Firstly, the balance of the balanced modulator degrades, and, secondly, the ALC detector sensitivity falls. However, it may, by careful design and layout prove practicable up to about 12MHz. By decreasing R1, the fall in sensitivity of the detector and its amplifier may be compensated, but filters at this frequency do not generally have the carrier suppression obtainable at lower frequencies. Nevertheless, acceptable results may be obtained at 9MHz. For a very simple SSB generator, the 'spare' amplifier in the SL6700C may be used as a VOGAD, although the input range is limited. However, the circuit shown in Fig.8 produces very effective results for simple low power SSB generation - and will run effectively with power levels of the order of 50mW drawn from the supply. This makes the circuit attractive for hand held CB, manpacks etc., where power consumption is extremely important.

Despite these minor disadvantages, the advent of low cost ceramic and mechanical filters at 455kHz designed for CB use, offer, with the SL6700, a low cost 'no adjustment' system drawing low power while performing adequately for the majority of SSB applications.

MODEL CONTROL

The majority of RC models are operated on the 27MHz band. At this frequency, the SL6700 performs quite adequately - see Fig.9. However, for many applications, operation from a lower voltage is necessary, and some redesign of Fig.9 would be required. Nevertheless, the advantage of the SL6700 in this application is that operation at 4.5V presents no difficulty to the IC, and so only circuits such as the oscillator need to be altered. For minimum component count R1 may be omitted, and L1 and the 56pF and 1nF input capacitors replaced by a ceramic filter such as the Murata SFE 27MA4. Should greater sensitivity be required, a transmistor RF amplifier and another ceramic filter would give the required increase. The low current consumption (typically 5mA at 4.5V) of the SL6700 is a decided advantage in this application.

The SL6700 supply voltage is best fixed at 4.5V-5.0V although operation up to 6V is generally practicable. The supply should not exceed 7V een momentarily as permanent damage may result.

The SL6700 is a versatile linear integrated circuit, providing an extremely wide range of RF applications in the HF range.

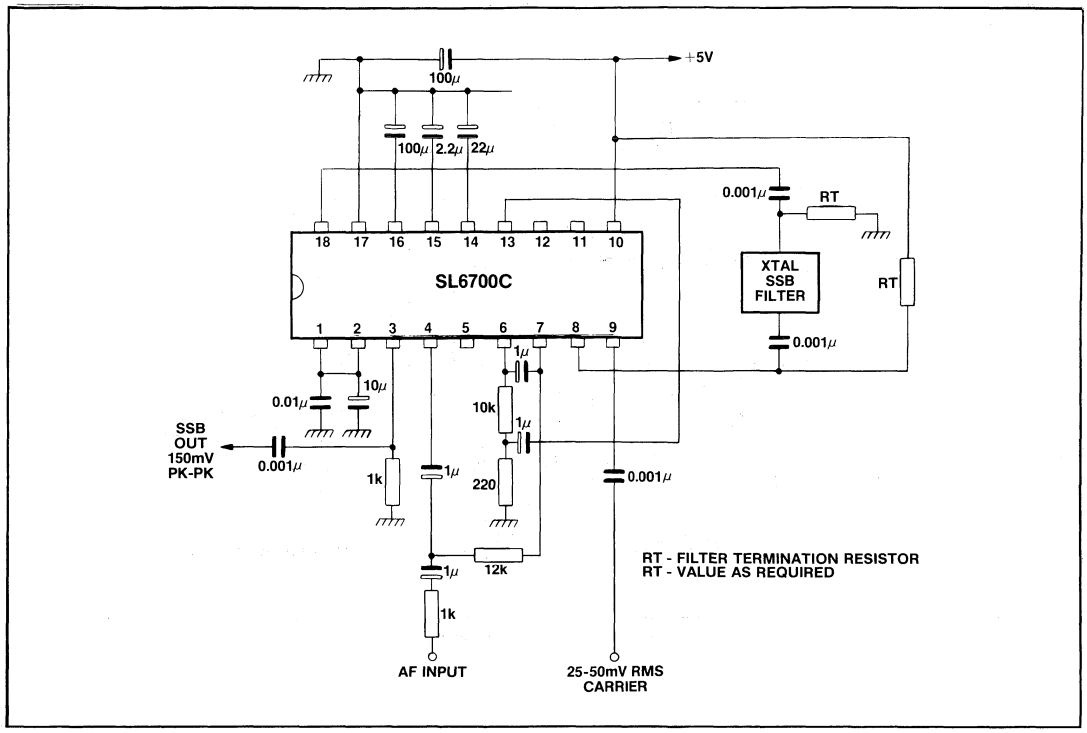


Fig.8

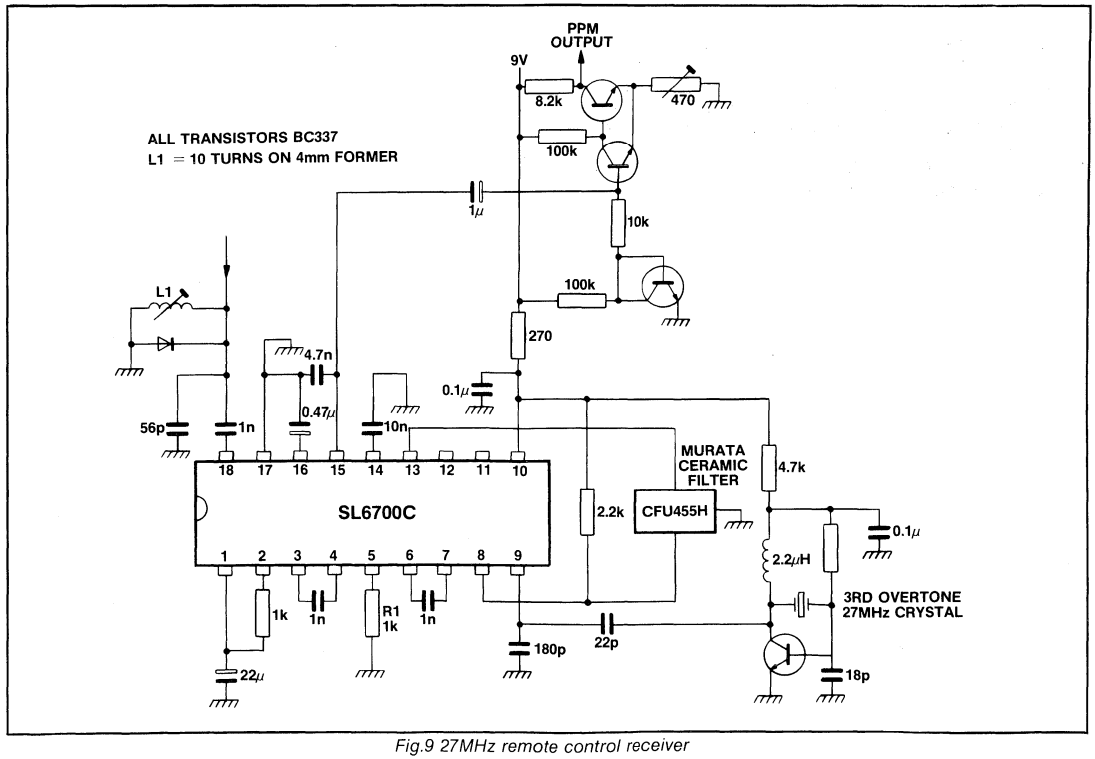


Fig.9 27MHz remote control receiver

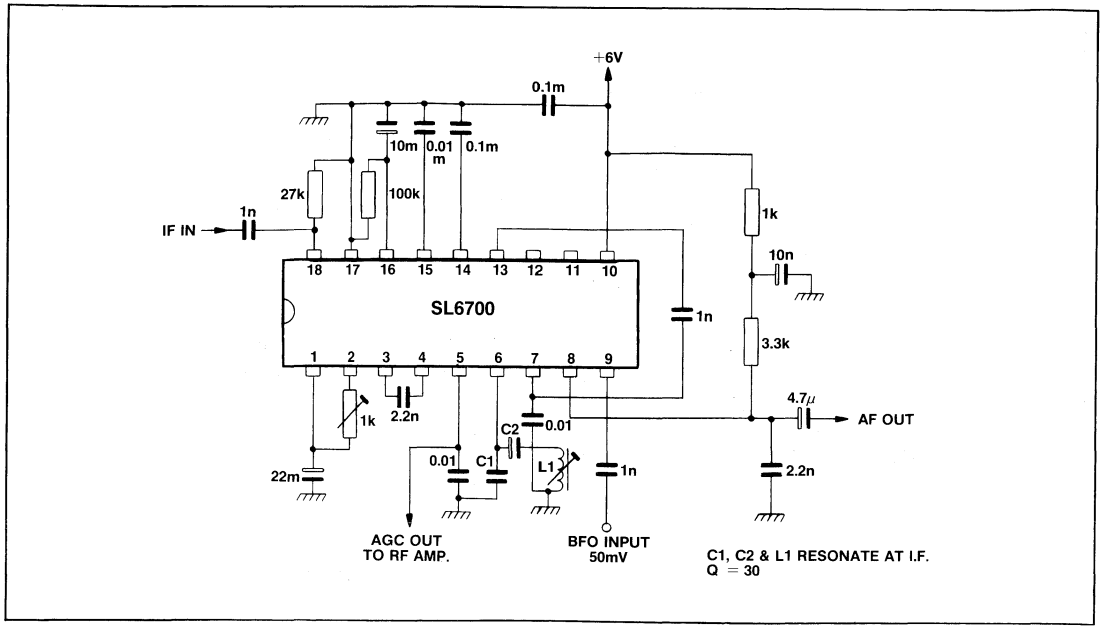


Fig.10 SL6700 CW receiver

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5. CHADWICK P.E.,DE MAW.D., Receiving with Plessey ICs. QST, April 1981, pp 13-15.

Thermal Design

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$

where θ_{ja} is thermal resistance junction-to-ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{ja})$
T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

A device is to be used at an ambient temperature of +50° C. θ_{ja} for the DG14 package with a chip of approximately 1mm sq is 107° C/W. Assuming the datasheet for the device gives P_D = 330mW and T_j max = 175° C.

$T_j = T_{amb} + P_D \theta_{ja}$
$= 50 + (0.33 \times 107)$
$= 85.31°C$ (typ.)

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Example 2

A device with T_{amb} max. = +175° C is to be used at an ambient temperature of +150° C. Again, θ_{ja} = 107° C/W, P_D = 330mW and T_j max. = +175° C.

$T_j = 150 + (0.33 \times 107)$
$= +185.3°\,C$ (typ.)

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the device operated as in Example 2 would result in a junction temperature given by:

$T_j = 150 + (0.33 \times 55)$
$= 168°\,C$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

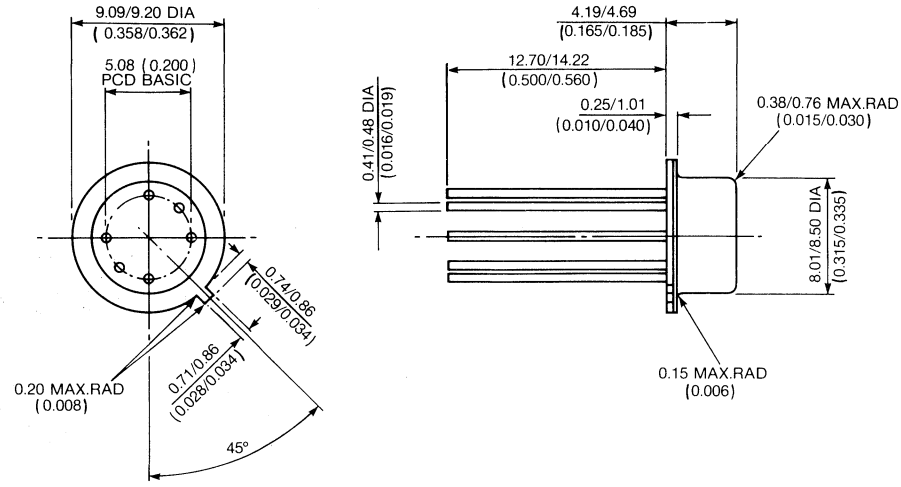
In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

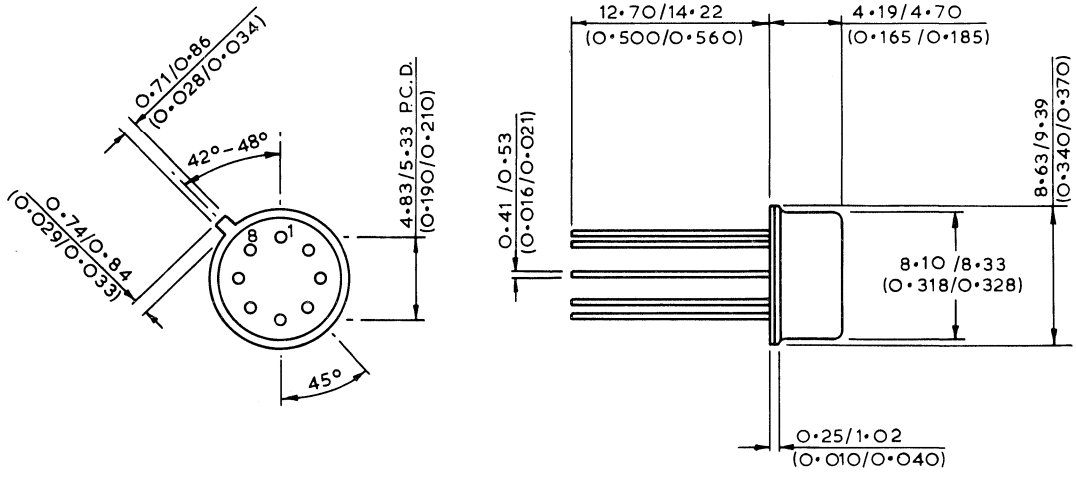
Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Package Outlines

Ordering Information



6-LEAD METAL CAN - CM6



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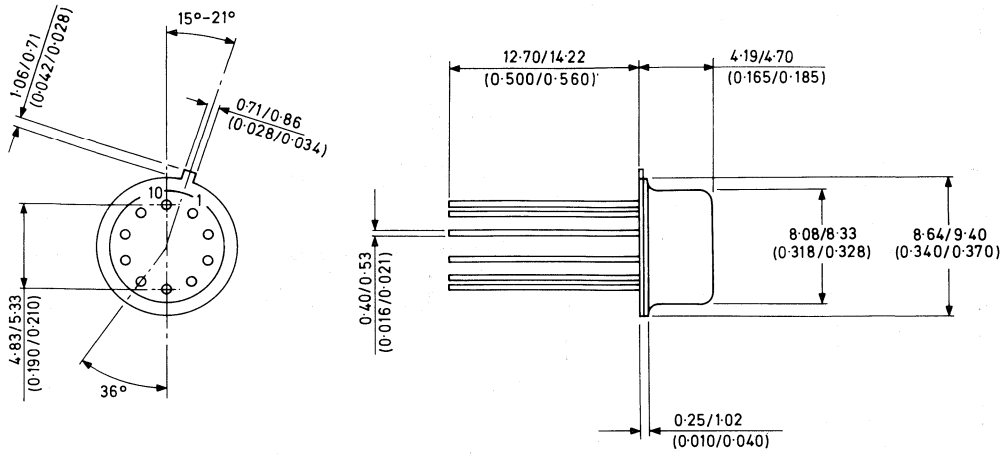

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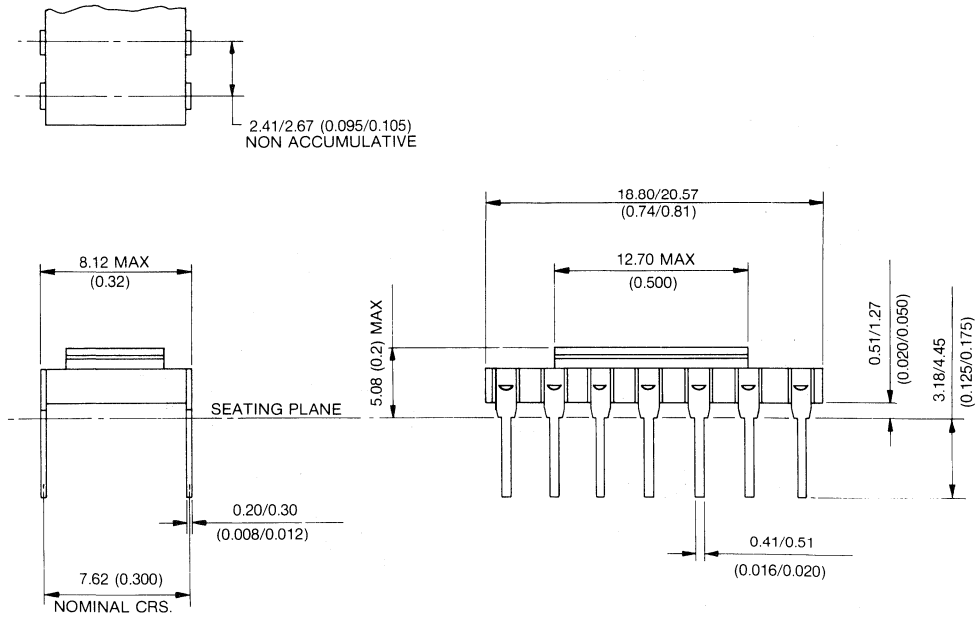
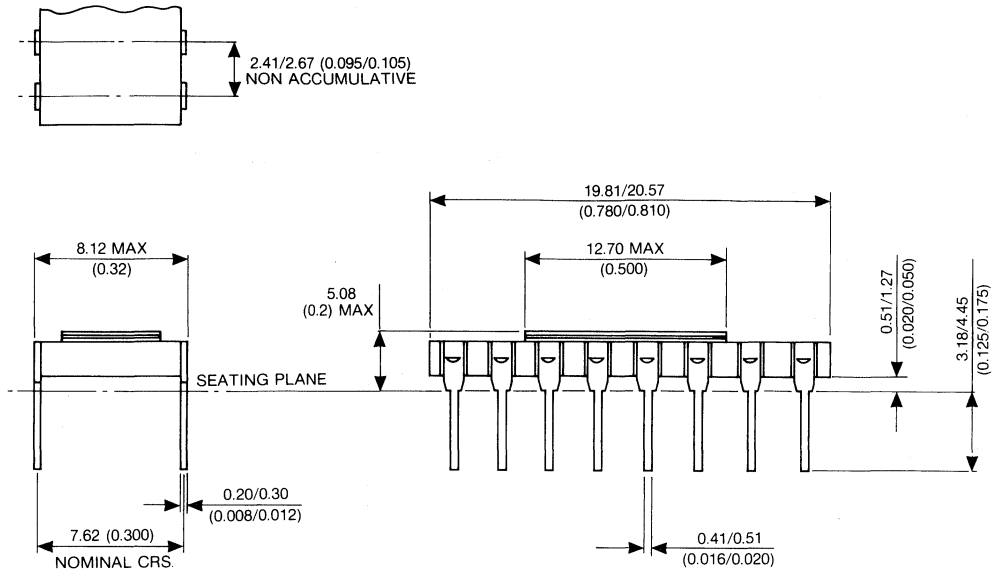
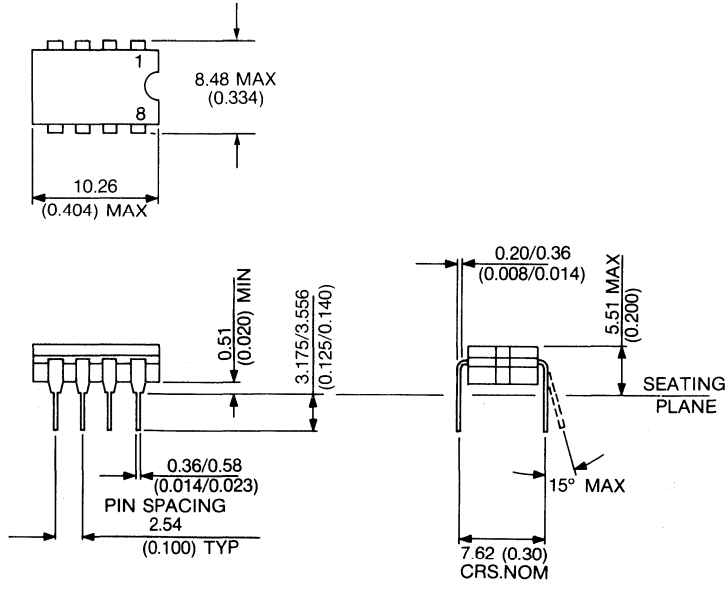


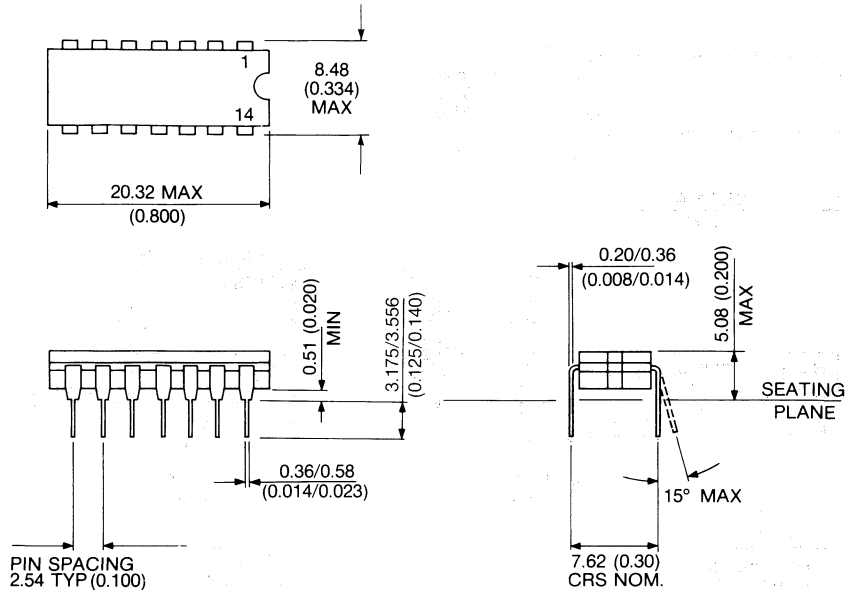
14-LEAD SIDEBRAZED CERAMIC DIL - DC14



16-LEAD SIDEBRAZED CERAMIC DIL - DC16



8-LEAD CERAMIC DIL - DG8



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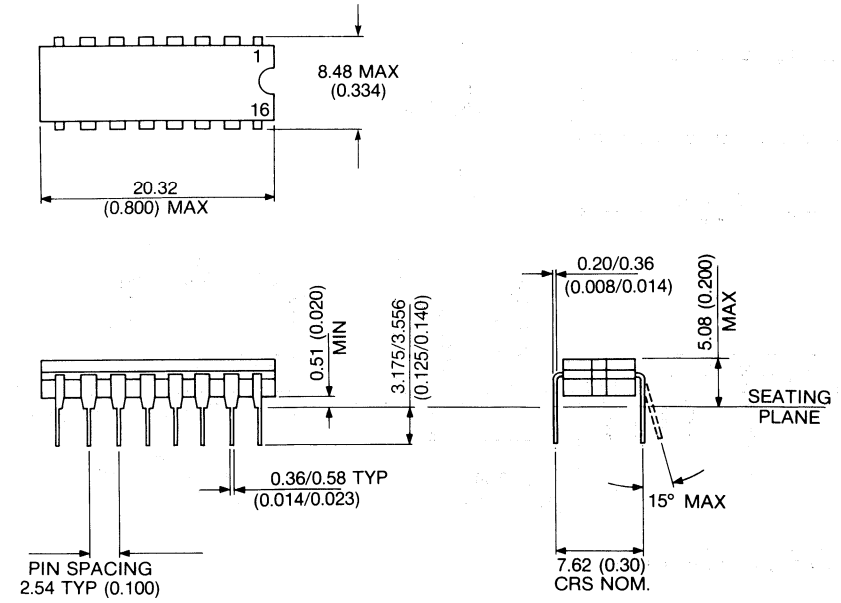

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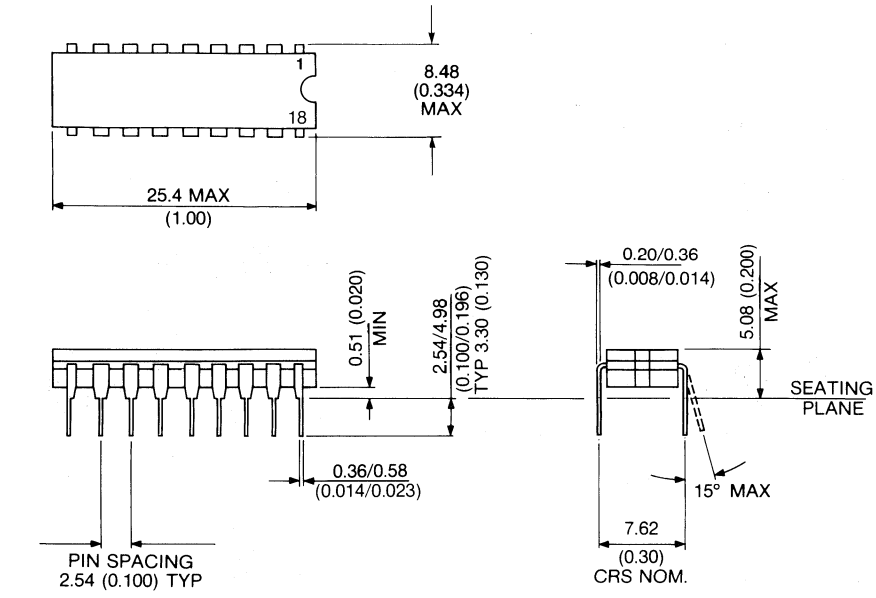
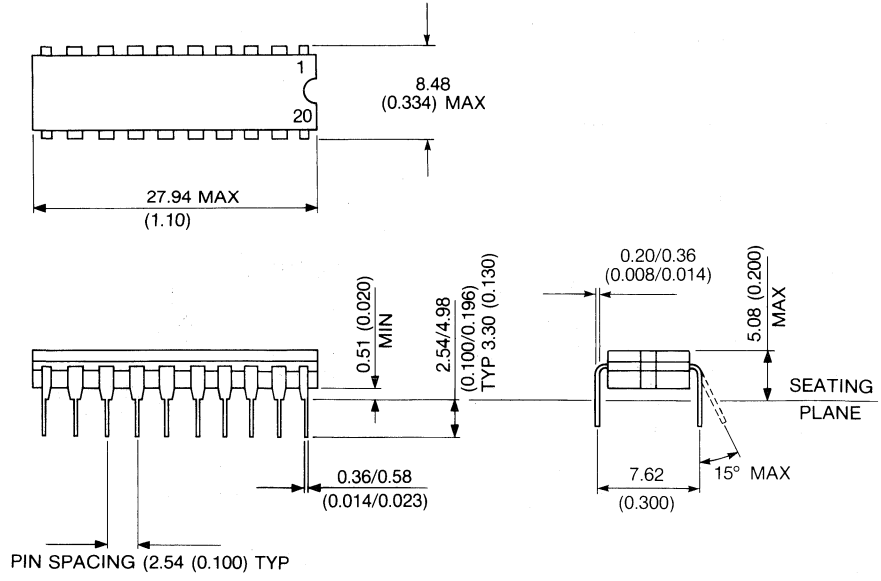


18-LEAD CERAMIC DIL - DG18



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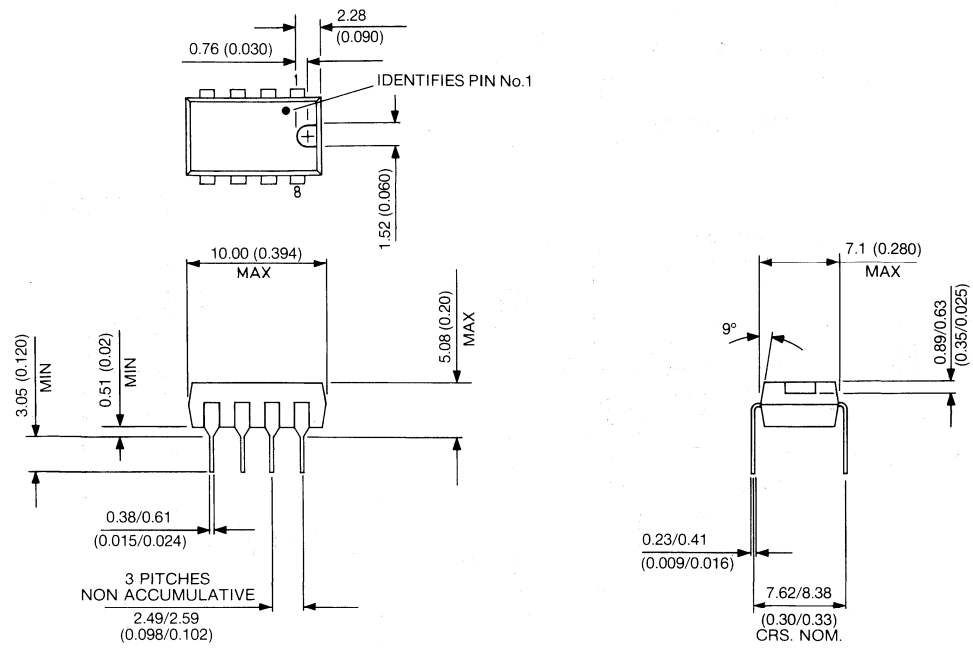
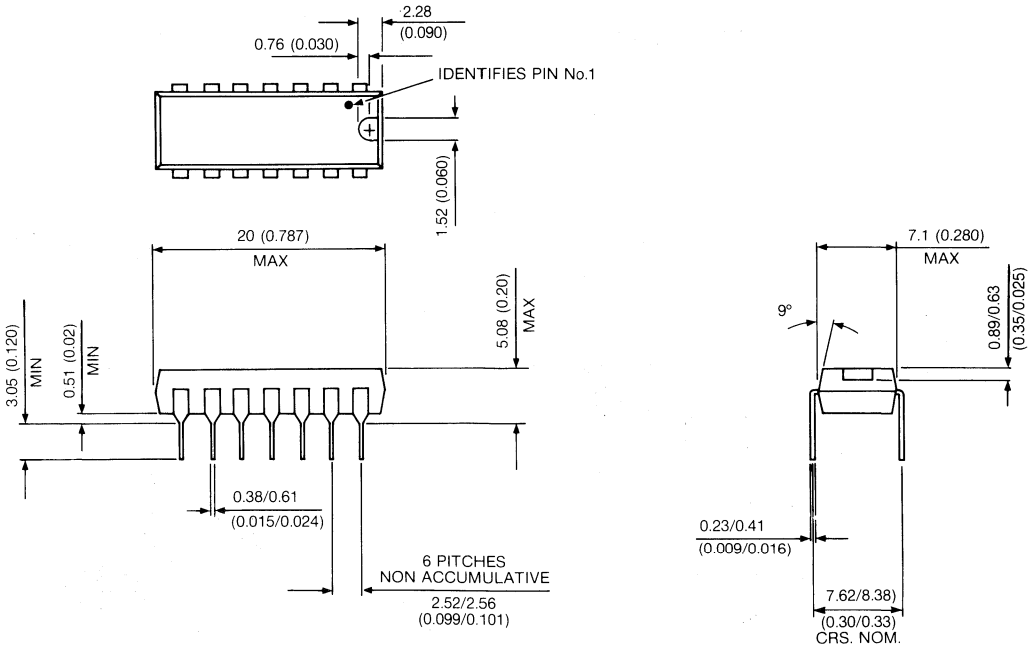


8-LEAD PLASTIC DIL - DP8



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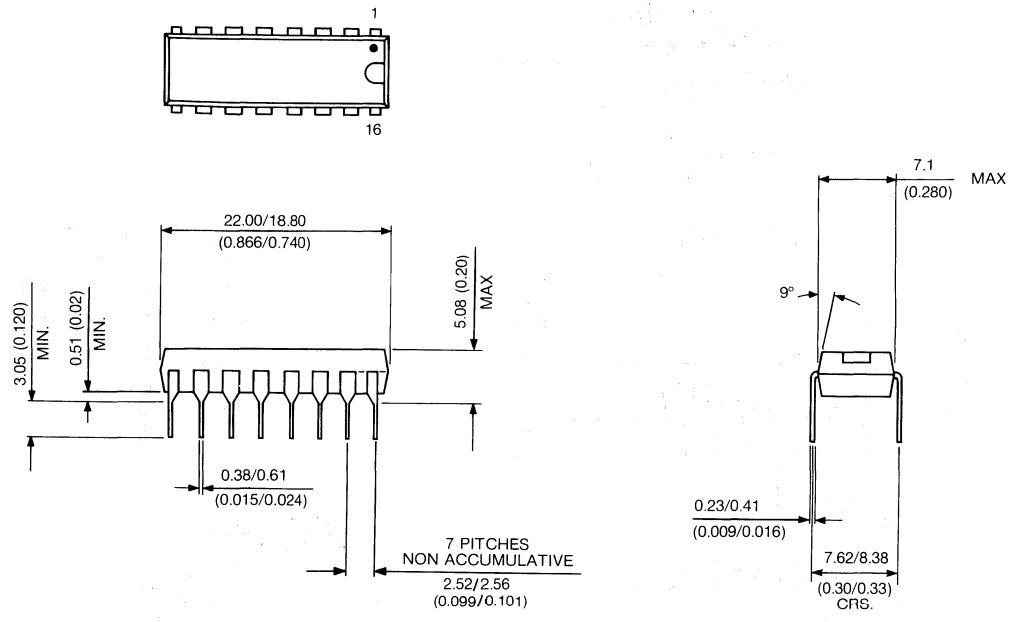

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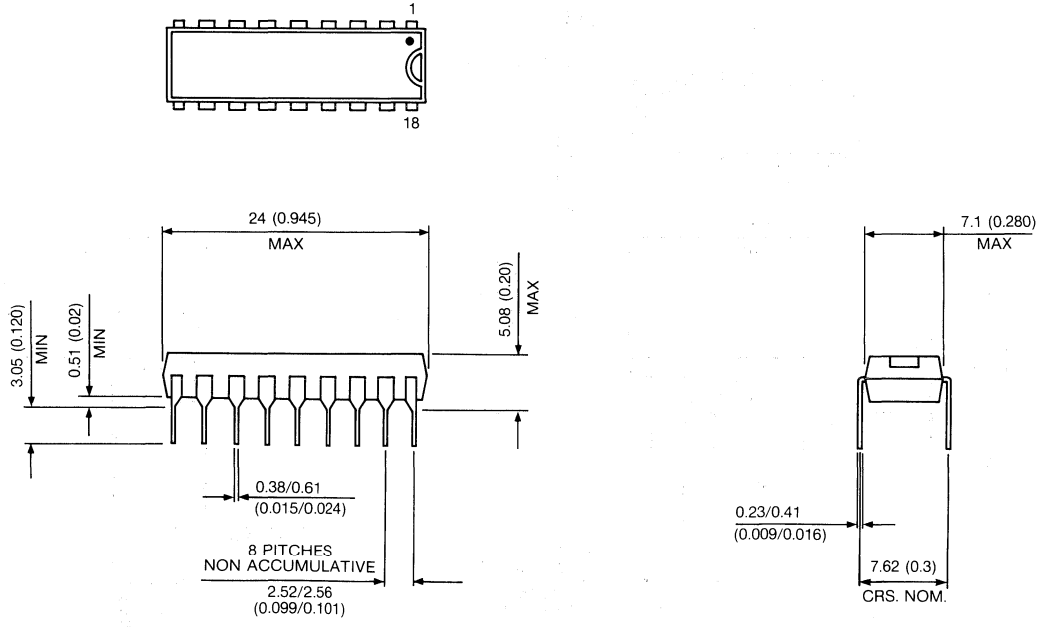

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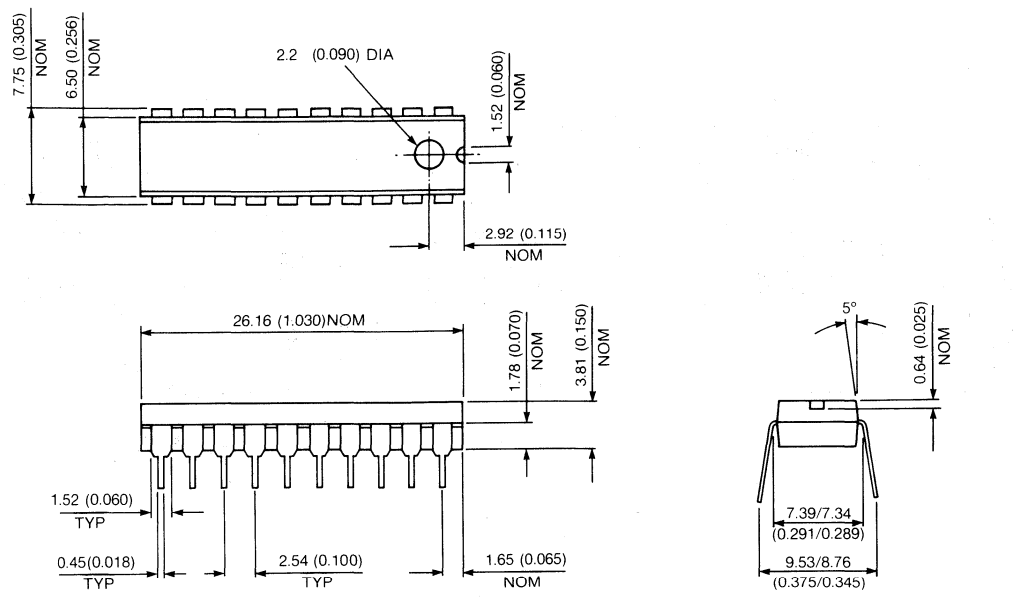

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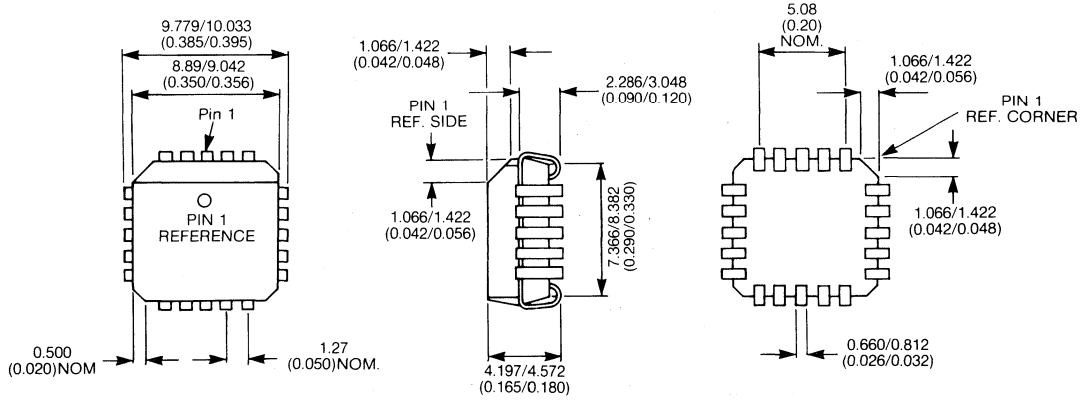
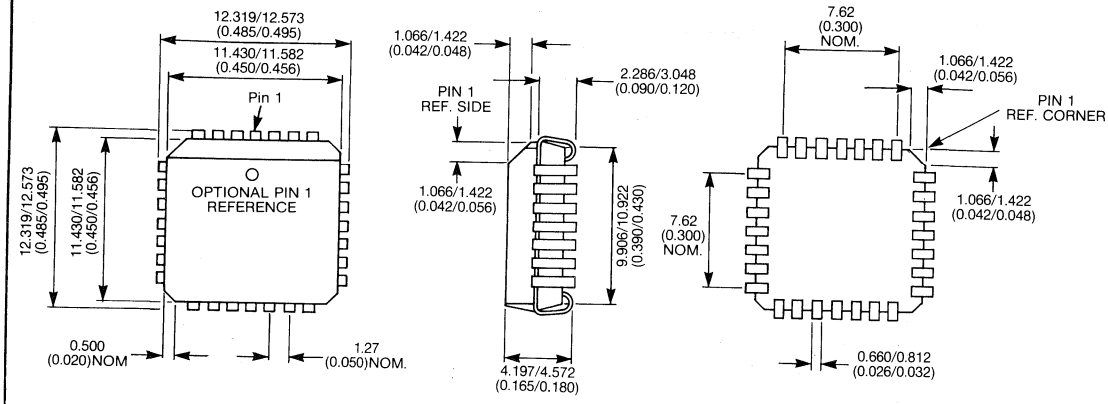


20-LEAD QUAD PLASTIC J LEAD - HP20



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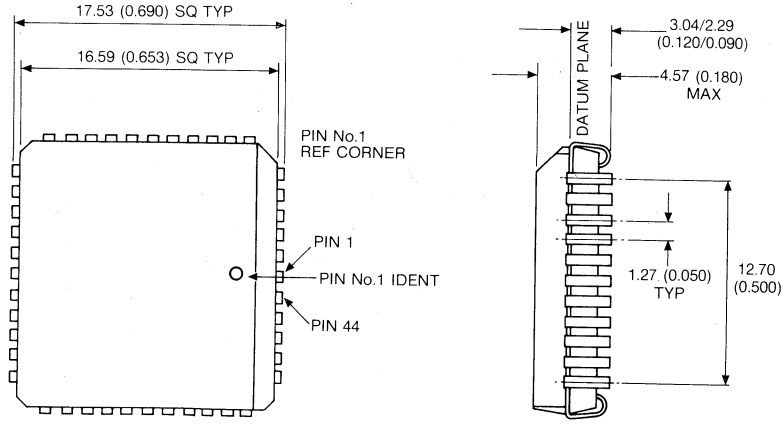
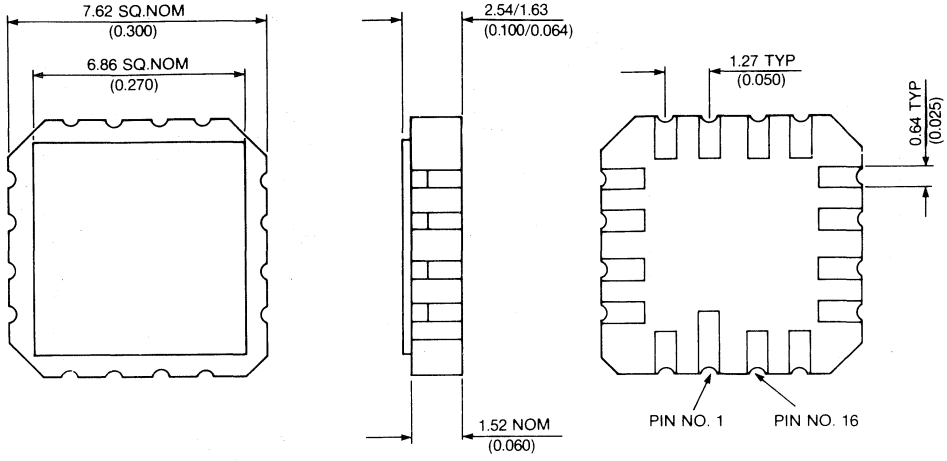
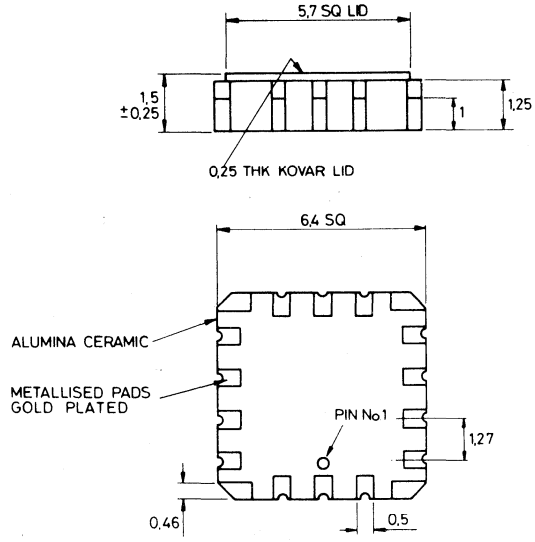


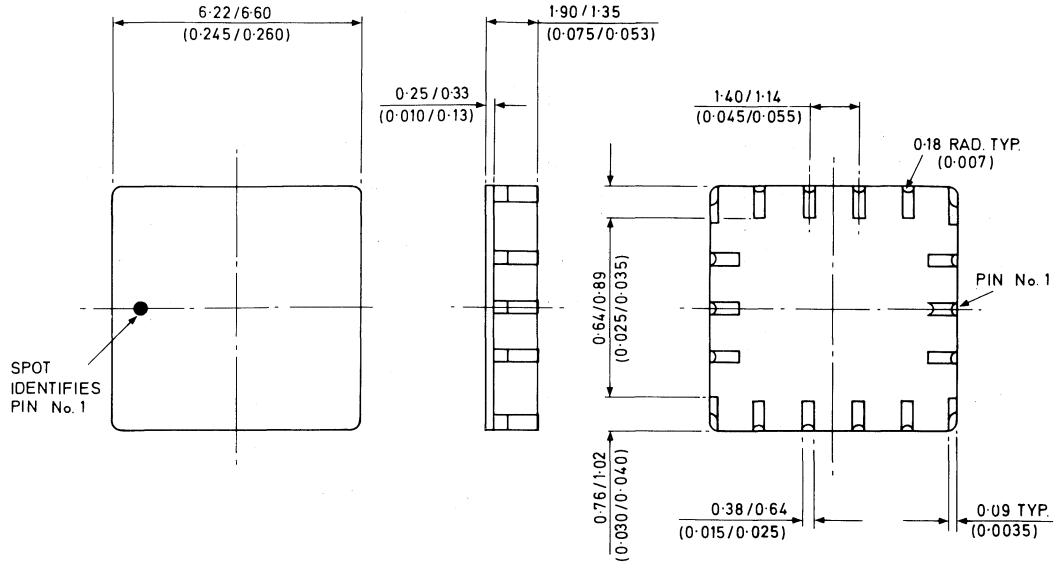
44-LEAD QUAD PLASTIC J LEAD - HP44



16-PIN LEADLESS CHIP CARRIER - LC16
(HERMETIC)



18-PIN LEADLESS CHIP CARRIER - AM18
(ZN460AM ONLY)



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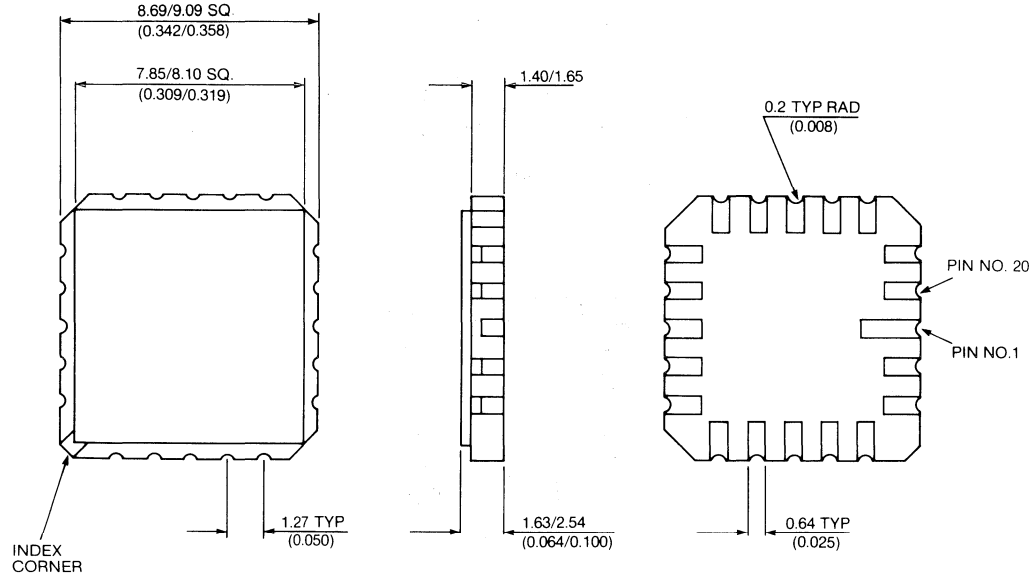
(HERMETIC) (SL6601 ONLY)



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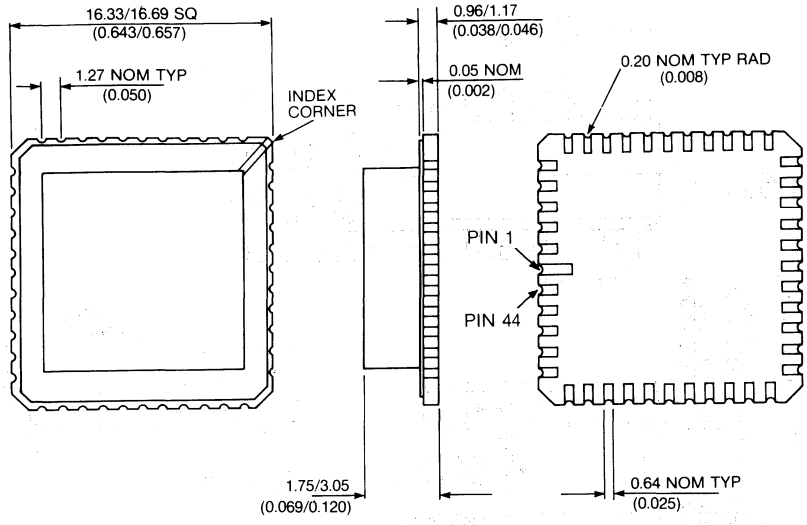
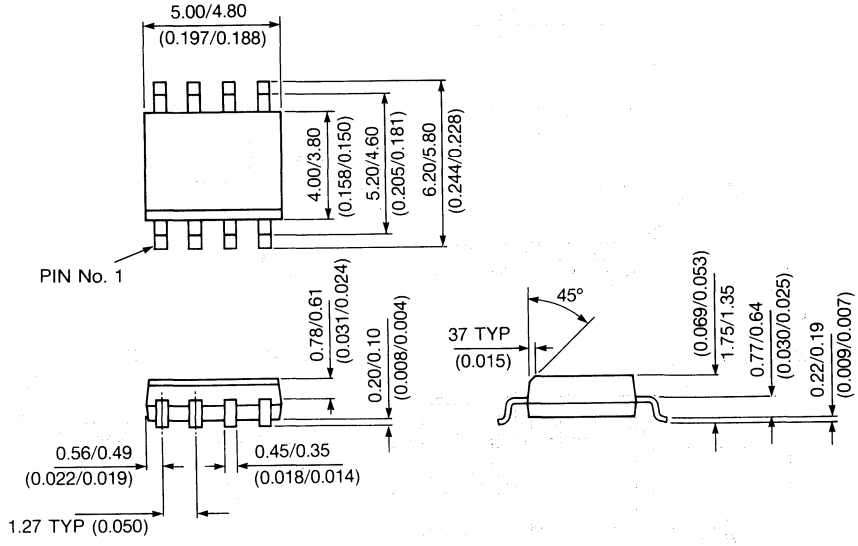
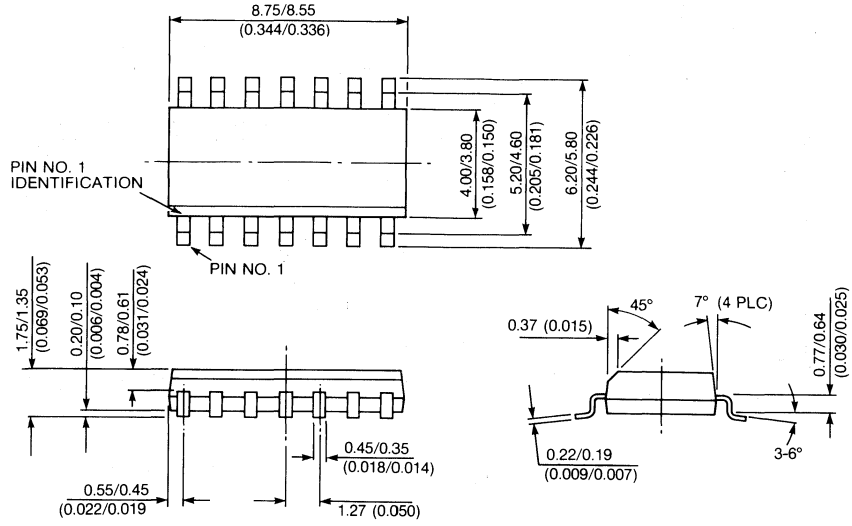
(HERMETIC)



44-PIN LEADLESS CHIP CARRIER - LE44
(NON-HERMETIC)



8-LEAD MINIATURE PLASTIC DIL - MP8



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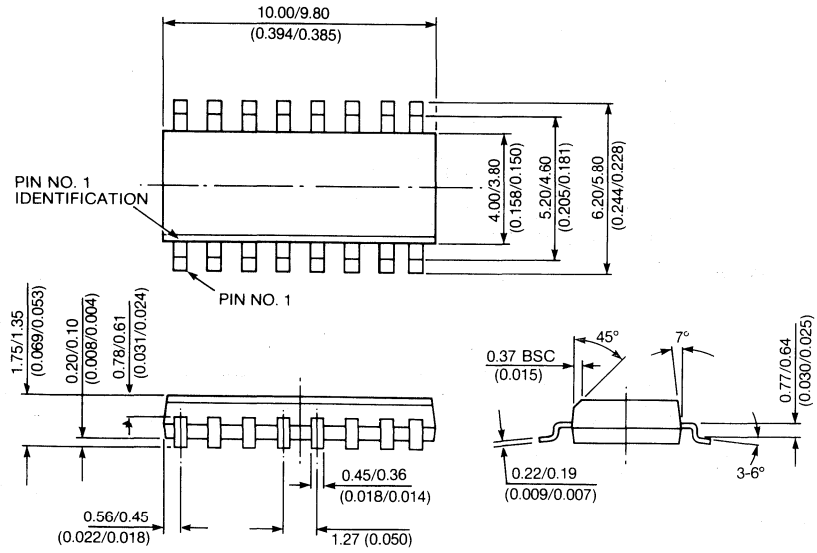

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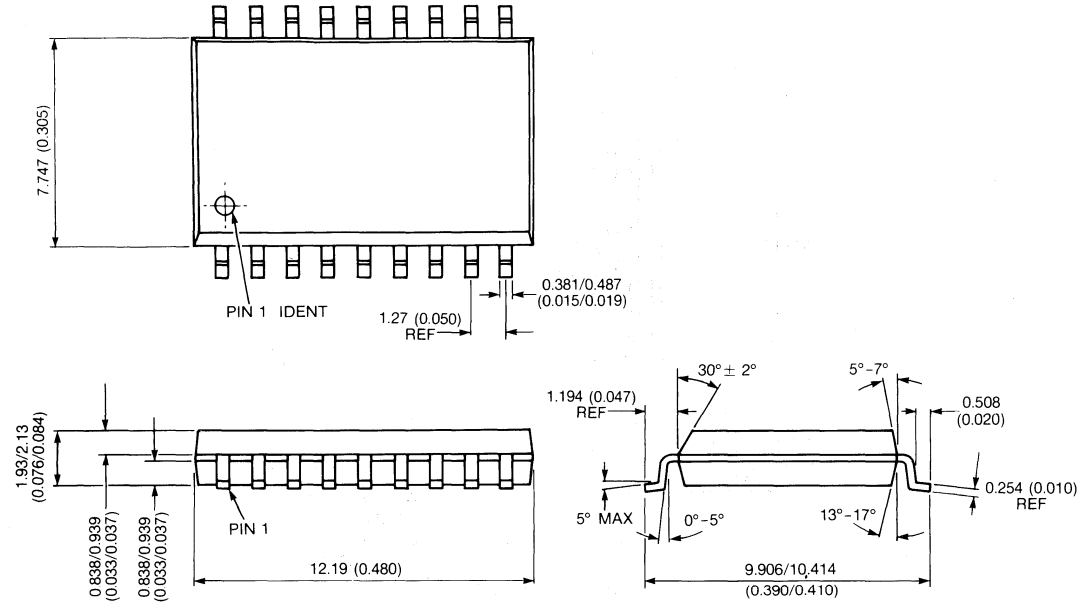

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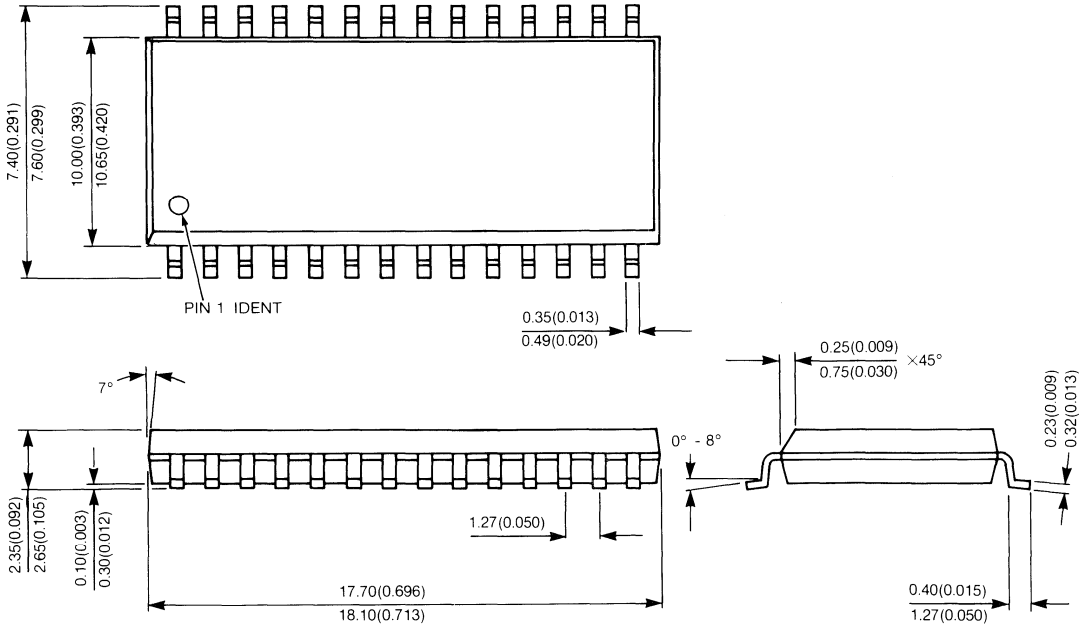

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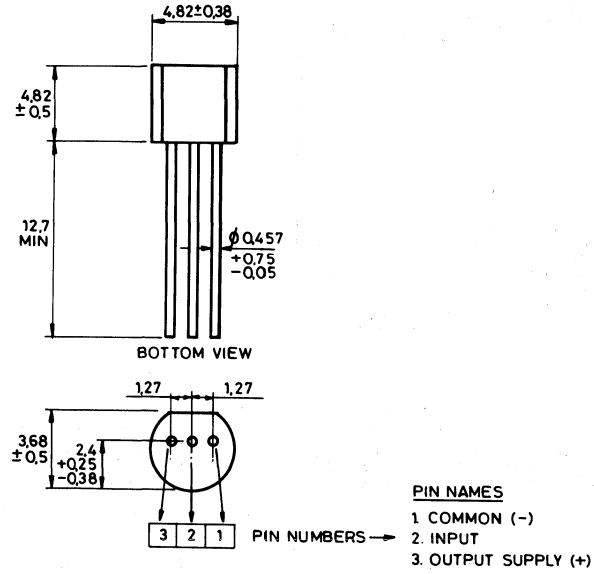

Dimensions in millimetres

TO-92 PLASTIC

Ordering information

Plessey Semiconductors integrated circuits are allocated type numbers which take the following general form

SL2521 B LC

where **SL** is a two-letter code identifying the product group and/or technology, **2521** is a three, four or five numeral code uniquely specifying the particular device, **B** is a one or two letter code denoting the precise electrical or thermal specification for certain devices and **LC** is a two-letter code defining the package style. For example, the **SL1613C** is offered in **DP** (Plastic DIL) and **MP** (Miniature plastic DIL) packages so the full ordering number for this device in ceramic DIL would be **SL1613C/DP** and **SL1613C/MP** for the miniature plastic DIL version.

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

A Pin-Grid Array
C Cylindrical
D Dual-in-Line (DIL)
F Flat Pack (leads on two sides)
G Flat Pack (leads on four sides)
Q Quad-in-Line

M Miniature
L Leadless Chip Carrier
H Leaded Chip Carrier (J-lead)

} Not yet designated by Pro-Electron

SECOND LETTER (indicates material)

C Metal-Ceramic (Metal Sealed)
G Glass-Ceramic (Glass Sealed)
M Metal
P Plastic
E Epoxy

Please Note:

Leadless Chip Carriers

LC Metal-Ceramic 3 Layer (Metal Sealed)
LG Glass-Sealed Ceramic
LE Epoxy-Sealed 1 Layer
LP Plastic

Leaded Chip Carriers

HG Glass-Sealed Ceramic
HP Plastic

Plessey Semiconductors Locations

Main offices

HEADQUARTERS **Plessey Semiconductors Ltd.,** Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom. Tel: 0793 36251 Tx: 449637 Fax: 0793 36251 Ext. 2198.

NORTH AMERICA **Plessey Semiconductors,** Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

International marketing centres

BENELUX **Plessey Semiconductors,** Avenue de Tervuren 149, Box 2, Brussels 1150, Belgium. Tel: 02 733 9730 Tx: 22100 Fax: 02 736 3547.

FRANCE **Plessey Semiconductors,** Avenue des Andes, B.P. No. 142, 91944 - Les Ulis Cedex. Tel: (6) 446-23-45 Telex: 602858F Fax: (6) 446-06-07.

ITALY **Plessey SpA,** Viale Certosa, 49, 20149 Milan. Tel: (2) 390044/5 Tx: 331347 Fax: 2316904.

UNITED KINGDOM (SOUTH) **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666 Ext.250.

UNITED KINGDOM (NORTH) **Plessey Semiconductors Ltd.,** Fields New Road, Chadderton, Oldham OL9 8NP, United Kingdom. Tel: 061-624 0515 Tx: 668038. Fax: 061 626 4946.

WEST GERMANY, AUSTRIA and SWITZERLAND **Plessey GmbH,** Ungererstrasse 129,D-8000 Munchen 40, West Germany. Tel: (089) 3609 06 0 Telex: 523980 Fax: (089) 3609 06 55.

SOUTH EAST ASIA **Plessey Company plc.,** Room 2204-7 Harbour Centre, 25 Harbour Road, Wanchai, Hong Kong. Tel: 58332111 Tx: 74754 Fax: 58339090.

World-wide agents

AUSTRALIA and NEW ZEALAND **Plessey Semiconductors Australia Pty Ltd.,** P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney 72 0133 Tx: AA20384 Direct Fax: (02) 7260669.

EASTERN EUROPE **Plessey Semiconductors Ltd.,** Unit 1, Crompton Road, Groundwell Industrial Estate, Swindon, Wilts. U.K. SN2 5AY. Tel: (0793) 726666 Tx: 444410 Fax: (0793) 726666.

GREECE **Mammeas,** Representations & Exportations, P.O.Box 181, Piraeus. Tel: 4172597 Tx: 213835 LHGR.

INDIA **Semiconductors Ltd.,** 71 Mittal Chambers, Nariman Point, Bombay 400 021. Tel: 2874518 Tx: 11 2781 ADOR IN.

Semiconductors Ltd., Unity Buildings, J.C. Road, Bangalore 560-001. Tel: 52072 & 578739.

Semiconductors Ltd., 513, Ashoka Estate, 24, Barakhamba Road, New Delhi — 110001. Tel: 44879 Tx: 31 3369.

Khandelwal Herrmann Electronics Limited, B-207, Neelam Centre, Worli, Bombay-400 025. Tel: 4947476.

JAPAN **Cornes & Company Ltd.,** Maruzen Building, 2 Chome Nihonbachi, Chuo-Ku, C.P.O.Box 158, Tokyo 100-91. Tel: 010 81 3 272 5771 Tx: 24874 Fax: 271-1479.

Cornes & Company Ltd., 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550. Tel: 532 1012 Tx: 525-4496 Fax: 541-8850.

Microtek Inc., Itoh Bldg., 7-9-17 Nishishinjuku, Shinjuku-ku, Tokyo 160. Tel: 03-371-1811 Tx: J27466 Fax: 03-369-5623.

HONG KONG **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kok Street, Tsuen Wan, N.T., Hong Kong. Tel: 0-444241-6 Tx: 36590 Fax: 499-3065.

KOREA **Young O Ind Co. Ltd.,** Yeoevido, P.O.Box 149, Seoul. Tel: 782 1707 Tx: K25701. Fax: 784 6786.

KML Corporation, 3rd Floor, Banpo Hall Building, 604-1 Banpo Dong, Kangnam-Ku, P.O.Box 19, Seoul. Tel: (02) 533-9281/2 Tx: KMLCORP K25981 Fax: (02) 533 1986.

MALAYSIA **Plessey Malaysia,** 1602 Pernas International Bldg, Jalan Sultan Ismail, Kuala Lumpur 50250. Tel: (03) 2611477 Tlx: 30918 PLESCOMA Direct Fax: (03) 2613385.

SCANDINAVIA

Denmark **Scansupply,** Nannasgade 18, DK-2200 Copenhagen N. Tel: 45 1 83 50 90 Tx: 19037 Fax: 45 1 83 25 40.

Finland **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 90 55 00 02 Tx: 122214 Fax: 055 1117.

Norway **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, Oslo 5. Tel: 02 64 11 50 Tx: 71963 Fax: 02 643443.

Sweden **Swedesupply AB,** PO Box 1028, 171 21 Solna. Tel: 08/735 81 30 Tx: 13435 Fax: 08/839033.

SINGAPORE **Plessey S.E. Asia Pte Ltd.,** 400 Orchard Road, No. 21-07 Orchard Towers, Singapore 0923. Tel: 7325000 Tx: RS22013 Direct Fax: 7329036.

SOUTH AFRICA **Plessey South Africa Ltd.,** 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793, Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SPAIN **JR Trading,** Apartado de Correos 8432, Madrid 8 Tel: 248 12 18/248 38 82 Tx: 42701. Fax: 241 4460.

TAIWAN **Artistex International Inc.,** B2, 11th Floor, 126, Nanking East Road, Section 4, Taipei, Taiwan, Republic of China. Tel: 2 7526330 Tx: 27113 Fax: 2 721 5446.

TURKEY **The Plessey Company plc.,** Koroglu Caddesi 5/4, Gaziosmanpasa, Ankara. Tel: 010 90 41 367352 Fax: 46526.

World-wide distributors

AUSTRALIA
Plessey Semiconductors Australia Pty Ltd., P.O.Box 2, Villawood, New South Wales 2163. Tel: Sydney (02) 720133 Tx: AA20384 Direct Fax: (02) 7260669.

AUSTRIA
DAHMS Elektronik Ges. mbH, Wiener Str. 287, A-8051 Graz. Tel: 0316/64030 Tx: 31099. Fax: 0316/6403029.
Othmar Lackner, Landstrasser Hauptstr. 37, A-1030 Wien. Tel: 0222 75 26 18-0 Tx: 111198. Fax: 0222/7526185.

BELGIUM
Master Chips, 4 St. Lazarus Laan, 1030 Brussels. Tel: 02 219 58 62 Tx: 62500. Fax: 02 217 92 01.

FRANCE
Mateleco:
Ile de France, 66, Avenue Augustin Dumont, 92240 Malakoff. Tel: (1) 46 57 70 55 Tx: 203436F.
Rhone-Alpes, 2 Rue Emile Zola, 38130 Echirolles. Tel: 76 40 38 33 Tx: 980837F.
ICC:
Bordeaux, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539F. Fax: 61 48 11 25.
Clermont-Ferrand, 2 bis, Avenue Fonmaure, 63400 Chamalieres. Tel: 73 36 71 41 Tx: 990928F.
Marseille, Z.A. Artizanord II, 13015 Marseille. Tel: 91 03 12 12 Tx: 441313F.
Toulouse, 78 Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10 Tx: 520897F.
CGE Composants S.A.:
Ile de France, 32 Rue Grange Dame Rose, 92360 Meudon la Foret. Tel: (1) 46 30 24 45 Tx: 632253F Fax: 46 30 0081
Aquitaine, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40 Tx: 571224F.
Bretagne, 9 Rue du General Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311F.
Centre/Pays-de-Loire, Allee de la Detente, 86360 Chaseneuil du Poitou. Tel: 49 52 88 88 Tx: 791525F.
Est, 27 Rue Kleber, 68000 Colmar. Tel: 89 41 15 43 Tx: 870569F.
Midi-Pyrenees, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38 Tx: 530957F.
Nord, 2 Rue de la Creativite, 59650 Villeneuve d'Ascq. Tel: 20 67 04 04 Tx: 136887F.
Provence/Cote d'Azur, Avenue Donadei, bat.B, 06700 St. Laurent du Var. Tel: 93 07 77 67 Tx: 461481F.
Rhone-Alpes, 101 Rue Dedieu, 69100 Villeurbanne. Tel: 78 68 32 29 Tx: 305301F.
ATAC-Diffusion SA, 2 Rue-Lecointre, 7 Ave de l'Europe, 92310 Sevres. Tel: 14 507 11 11 Tx: 203047 Fax: (1) 45341042.

ITALY
Eurelettronica SpA, Via E Fermi 8, 20090 Assago (Milan). Tel: 02-4880022 Tx: 350037. Fax: 488 0275.
Eurelettronica, Via Bertoloni 27, Rome. Tel: 875394 Tx: 610358.
Alta S.R.L., Via Matteo Di Giovanni 6, 50143 Florence. Tel: 055717402 Tx: 571246. Fax: 055/705658.
Adelsi Spa, Via Novara 570, 20153 Milan. Tel: 02 3580641 Tx: 332423 Adelsy I Fax: 02/3011988.
ESCO Italiana Spa., Via Modena 1, 20099 Sest S Giovanni. Tel: 02 24 09 241-251 Tx: 322383. Fax: 02/2409255.
Fanton S.R.L., Bologna, Milano, Firenze, Roma, Padora, Torino. Tel: (02) 3287312 Fax: 051/732216.

NETHERLANDS
Heynen B.V., Postbus 10, 6590 AA Gennep. Tel: 8851-96111 Tx: 37282 Fax: 08851 96220.
Tekelek Airtronic BV., Postbus 63-2700 AB, Zoetermeer. Tel: 079 31010 Tx: 33332. Fax: 079 417504.

SOUTH AFRICA
Plessey South Africa Ltd., 1 Jansen Road, Jet Park, Boksburg. Tel: (011) 8266793 Tx: 4-31421 SA Fax: (011) 8266704 after hours.

SWITZERLAND
Aumann & Co. AG, Forrlibuckstrasse 150, CH-8037 Zurich. Tel: 01/443300 Tx: 822966. Fax: 01/44 5023.
Elbatex AG., Hardstr. 72, 5430 Wettingen. Tel: 056 27 51 11 Tx: 58068 Fax: 056/271924.

TAIWAN
Artistex International Inc., B2, 11th Floor, 126, Nanking East Road, Section 4, Taipai, Taiwan, Republic of China. Tel: (02) 7526330 Tx: 27113 ARTISTEX Fax: (8862) 721 5446.

UNITED KINGDOM
Celdis Ltd.,37-39 Loverock Road, Reading, Berks RG3 1ED. Tel: 0734 585171 Tx: 848370 Fax: 0734 509933.
Farnell Electronic Components Ltd., Canal Road, Leeds LS12 2TU. Tel: 0532 636311 Tx: 55147 Fax: 0532 633404.
Gothic Crellon Ltd., 3 The Business Centre, Molly Millars Lane, Wokingham, Berkshire RG11 2EY. Tel: 0734 788878/787848 Tx: 847571 Fax: 0734 776095.
Gothic Crellon Ltd., P.O.Box 301, Trafalgar House, 28 Paradise Circus, Queensway, Birmingham B1 2BL. Tel: 021 6436365 Tx: 338731.
RR Electronics Ltd., St. Martins Way, Cambridge Road, Bedford MK42 0LF. Tel: 0234 47188/270777 Tx: 826251 Fax: 0234 210674.
Semiconductor Specialists (UK) Ltd., Carroll House, 159 High Street, Yiewsley, West Drayton, Middlesex UB7 7XB. Tel: 0895 445522 Tx: 21958 Fax: 0895 422044.

STC Electronic Services, Edinburgh Way, Harlow, Essex CM20 2DF.Tel: 0279 626777 Tx: 818801. Fax: 0279 441687.
Unitel Ltd., Unitel House, Fishers Green Road, Stevenage, Herts. Tel: 0438 312393 Tx: 825637. Fax: 0438 318711.

UK EXPORT (to countries other than those listed)
Extram (U.K.) Ltd., 1A Albert St., Slough, Berks. SL1 2BH. Tel: 0753 824311 Tx: 848441 EXTRAM G Fax: 0753 820250.

WEST GERMANY
Altron GmbH & Co. KG, Gaussstr. 10, 3160 Lehrte. Tel: 051 32 5 30 24 Tx: 922383 Fax: 05132/57776.
API Elektronik Vertriebs GmbH, Augustinerring 27, D-8062 Markt Indersdorf. Tel: 08136/7092 Tx: 5270505 Fax: 08136/7398.
AS Electronic Vertriebs-GmbH, Elisabethenstrasse 35, 6380 Bad Homburg. Tel: 06172/2 90 28-29 Tx: 410868.
Astronic GmbH, Winzererstrasse 47D, 8000 Munchen 40. Tel: 089/309031 Tx: 5216187 Fax: 089 300 6001.
Micronetics GmbH, Weil der Stadter Str. 45, 7253 Renningen 1. Tel: 07159/6019 Tx: 724708. Fax: 07159/5119.
Weisbauer Elektronik GmbH, Heiliger Weg 1, 4600 Dortmund 1. Tel: 0231 57 95 47 Tx: 822538 Fax: 0231/577514.

North American representatives

NATIONAL SALES — Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. United States of America. Tel: (408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576.

EASTERN REGION — 1767-42 Veterans Memorial Hwy., Central Islip, NY 11722. Tel: (516) 582-8070 Tlx: 705922 Fax: 516-582-8344.

NEW ENGLAND REGION — 132 Central St., 216 Foxboro, MA 02035. Tel: (617) 543-3855 Tlx: 316805 Fax: 617-543-2994.

WESTERN REGION — 4633 Old Ironsides Dr. 250, Santa Clara, CA 95054. Tel: (408) 986-8911 Tlx: 62217370 Fax: 408-970-0263.

SOUTHEAST REGION — 9330 LBJ Freeway, Ste. 665, Dallas, TX 75243. Tel: (214) 690-4930 Tlx: 510-600-3635 Fax: 214-680-9753.

NORTH CENTRAL REGION — 1919 South Highland 120C, Lombard, IL 60148. Tel: (312) 953-1484 Tlx: 705186 Fax: 312-953-0633.

FLORIDA & DIXIE REGION — 541 S.Orlando Ave., Suite 310, Maitland, FL 32751. Tel: (305) 539-0080 Fax: 304-539-0055.

SOUTHWEST REGION — 9 Parker, Irvine, CA 92718. Tel: (714) 472-2530 Tlx: 989096 Fax: 714-458-7084.

DISTRIBUTION SALES — 9 Parker, Irvine, CA 92718. Tel: (714) 472-0303 Tlx: (910) 595-1930 Fax: (714) 770-0627.

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North American sales offices

ALABAMA — **DHR Marketing, Inc.,** 904 Bob Wallace Avenue, Suite 222, Huntsville, AL 35801. Tel: (205) 533-5165 Fax: (205) 533-1312.

ARIZONA — **Reptronix/Chaparral,** 4625 South Lakeshore Dr., Tempe, AZ 85282-7127. Tel: (602) 345-4580 Fax: (602) 839-3841.

CALIFORNIA — **Cerco,** 5230 Carrol Canyon Rd. 214, San Diego, CA 92121. Tel: (619) 450-1754 Fax: 619-450-3681.
Pinnacle Sales Corp., 275 Saratoga Ave., Suite 200, Santa Clara, CA 95050. Tel: (408) 249-7400 Fax: 408-249-5129.
Select Electronics, 2109 Brookfield Drive, Thousand Oaks, CA91362.
Straube Associates, 2551 Casey Avenue, Mountain View, CA 94043. Tel: (415) 969-6060 Fax: (415) 964-6526.
Select Electronics, 14730 Beach Blvd-Bldg F, Suite 106, La Mirada, CA 90638. Tel: (714) 739-8891 Twx: 910-596-2818 Fax: 714-739-1604.

COLORADO — **MRC,** 2579 W. Main St. Littleton, CO 80120. Tel: (303) 794-4684 Fax: (303) 794-4644.

CONNECTICUT — **NRG Ltd.,** 63 Duka Avenue, Fairfield, CT 06430. Tel: (203) 384-1112 Fax: (203) 335-2127.

FLORIDA — **Lawrence Associates,** 1131 South U.S.19 Palm Barbor, FL 34684. Tel: (813) 787-2773 Fax: (813) 787-2654.
Lawrence Associates, 380 Lowndes Square, Casselberry, FL 32707. Tel: (305) 339-3855 Fax: (305) 767-0973.
Lawrence Associates, 5021 N. Dixie Highway, Boca Raton, FL 33431. Tel: (305) 368-7373 Fax: 305-394-5442.

GEORGIA — **DHR Marketing, Inc.,** 3100 Breckenridge Blvd. Suite 145, Duluth, GA 30136. Tel: (404) 564-0529 Fax: (404) 564-1127.

IDAHO — **Crown Electronic Sales, Inc.,** 601 W. Hays, Suite 20, Boise, Idaho 83702. Tel: (208) 344-9588 Fax: (208) 344-9550.

INDIANA	**Corrao Marsh, Inc.,** 6211 Stoney Creek Drive, Fort Wayne, IN 46825. Tel: (219) 482-2725 Fax: 219-484-7491.
	Corrao Marsh, Inc., 3117 West U.S. 40, Greenfield, IN 46140. Tel: (317) 462-4446. Fax: (317) 462-6568.
ILLINOIS	**Micro Sales, Inc.,** 54 West Seegars Road, Arlington Heights, IL 60006. Tel: (312) 956-1000 Twx: 510-600-0756 Fax: 312-956-0189.
IOWA	**Lorenz Sales,** 5270 N. Park Place N.E., Cedar Rapids, IA 52402. Tel: (319) 377-4666 Fax: 319-377-2273.
KANSAS	**Lorenz Sales, Inc.,** 8115 West 63rd St., Suite 1, Merriam, KS66202. Tel: (913) 384-6556.
MARYLAND	**Walker-Houck,** 10706 Reisters Town Rd., Suite D, Owings Mills, MA 21117. Tel: (301) 356-9500 Fax: 301-356-9503.
MASSACHUSETTS	**Stone Components,** 2 Pierce Street, Framingham, MA 01701. Tel: (617) 875-3266 Twx: 310-374-6662 Fax: 617-875-0537.
MICHIGAN	**R.P. Urban & Associates,** 2335 Burton Street SE, P.O. Box 7386, Grand Rapids, MI49510. Tel: (616) 245-0511 Fax: (616) 245-4083.
	R.P. Urban & Associates, 24634 Five Mile Road, Detroit, MI48239. Tel: (313) 535-2355 Fax: (313) 7109.
MINNESOTA	**Electro Mark Inc.,** Valley Oaks Business Cntr. 7167 Shady Oak Rd., Eden Prairie, MN 55344. Tel: (612) 944-5850 Fax: (612) 944-5855.
MISSOURI	**Lorenz Sales, Inc.,** Del Crest Plaza Bldg. Suite 208, 8420 Delmar Blvd., University City, MO 63124. Tel: (314) 997-4558 Fax: 319-337-2273.
NEBRASKA	**Lorenz Sales,** 2801 Garfield Street, Lincoln, NE 68502. Tel: (402) 475-4660.
NEW JERSEY	**Metz Benham Associates, Inc., (MBA),** Terrace Level, Suite II, 1982 Greentree Road, Cherry Hill, NJ 08003. Tel: (609) 424-0404 Fax: (609) 751-2160.
	Metro Logic, 280 Midland Ave., Bldg N-1, Saddle Brook, NJ 07662. Tel: (201) 797-8844 Fax: 201-797-8418.
NEW MEXICO	**Reptronix/Chaparral,** 237 C Eubank Blvd., N.E., Albuquerque, NM 87123. Tel: (505) 292-1718 Fax: (505) 299-1611.
NEW YORK	**Micro-Tech,** 1350 Buffalo Road, Rochester, NY 14624. Tel: (716) 328-3000 Fax: (716) 328-3003.
	Micro-Tech, 401 South Main Street, North Syracuse, NY 13212. Tel: (315) 458-5254 Fax: (315) 458-5919.
	Micro-Tech, 10 Guyton Street, Kingston, NY 12401. Tel: (914) 338-7588.
NORTH CAROLINA	**DHR Marketing, Inc.,** 4016 Barrett Drive, Suite 201 (27609) P.O. Box 19703, Raleigh, NC 27609. Tel: (919) 781-1961
SOUTH CAROLINA	**DHR Marketing, Inc.,** 37 Villa Road, Suite 409, Greenville, SC 29615. Tel: (803) 271-8712 Fax: (803) 271-8712.
OHIO	**Scott Electronics, Inc.,** 3131 S. Dixie Dr., Suite 200, Dayton, OH 45439. Tel: (513) 294-0539 Fax: (513) 294-4769.
	Scott Electronics, Inc., 360 Alpha Park, Cleveland, OH 44143. Tel: (216) 473-5050 Fax: (216) 473 5055.
	Scott Electronics, Inc., 6515 East Livingston Avenue, Reynoldsburg, OH 43068 Tel: (614) 1281 Fax: (614) 863-1485.
	Scott Electronics, Inc., 10901 Reed Hartman Hwy., Suite 301, Cincinnati, OH 45242. Tel: (513) 791-2513 Fax: (513) 791-8059.
OREGON	**Core II, P.O. Box 5459, Beaverton, OR 96006-0459.** Shipping Address only: 21785 S.W. T.V. Hwy, Unit Q, Beaverton, OR 97006. Tel: (503) 641-0877 Fax: (503) 591-8383.
	Crown Electronic Sales, Inc., 17020 S.W. Upper Boones Ferry Rd., Suite 202, Portland, OR 97223. Tel: (503) 620-8320 Fax: 503-639-4023.
TENNESSEE	**DHR Marketing, Inc.,** 417 Welchwood, Suite 102, Nashville, TN 37211.Tel: (615) 331-2745.
TEXAS	**Oeler & Menelaides, Inc.,** 8340 Meadow Rd., Suite 24, Dallas, TX 75231. Tel: (214) 361-8876 Fax: (214) 692-0235.
	Oeler & Menelaides, Inc., 12777 Jones Rd., Suite 175-18, Houston, TX 77070. Tel: (713) 894-5021.
	Oeler & Menelaides, Inc., 8705 Shoal Creek Rd., Suite 218, Austin, TX 78758. Tel: (512) 453-0275 Fax: (512) 453-0088.
WASHINGTON	**Core II,** 2535 152nd N.E. Suite A, Redmond, WA 98052. Tel: (206) 746-1799 (Home)
	Crown Electronic Sales, Inc., 14400 Bel-Red Rd., 108, Bellevue, WA 98007. Tel: (206) 643-8100 Fax: 206-747-6861.
WISCONSIN	**Micro Sales, Inc.,** N8 W12920 Leon Road, Suite 115, Menomonee Falls, WI 53051. Tel: (414) 251-0151.
CANADA EASTERN	**Gidden-Morton Assoc.Inc.,**7050 Bramalea Road, Suite 27A, Mississauga, Ontario L5S 1T1. Tel: (416) 671-8111 Fax: (416) 671-2422.
	Gidden-Morton Assoc.Inc.,3860 Cote-Vertu, Suite 221, St. Larent, Quebec H4R 1N4. Tel: (514) 335-9572 Fax: 514-335-9573.
	Gidden-Morton Assoc.Inc.,301 Moodie Drive, Suite 101, Nepean, Ontario K2H 9C4. Tel: (613) 726-0844 Fax: 613-726-0953.
CANADA WESTERN	**Dynasty Components, Inc.,** 12618 55A Avenue, Surrey, British Columbia V3W 1C3. Tel: (604) 597-0068 Fax: (604) 597-0043.

American design centres

ARIZONA **CaDel,** 715 N. Constitution Drive, Dueson, AZ 85748. Tel: (602) 296-8591.

CALIFORNIA **Analog Solutions,** 532 Fourth Street, Encinitas, CA 92024. Tel: (619) 944-1657.

Silicon Development Corp., 16162 Beach Boulevard, Suite 304, Huntington Beach, CA 92647. Tel: (714) 847-1992.

CANADA **Ontario Centre for Microelectronics,** 1150 Morrison Drive, Suite 400, Ottawa, K2H 9B8. Tel: (613) 596-6690.

Alberta Microelectronics Center, Suite 200, 1620-29 St., N.W., Calgary, Alberta T2N 4L7. Tel: (403) 289-2043.

COLORADO **Analog Solutions,** 5484 White Place, Boulder, CO 80303. Tel: (303) 442-5083.

FLORIDA **Silicon Beach Enterprises, Inc.,** 700 U.S. Highway One, Suite C, North Palm Beach, FL 33408. Tel: (305) 844-7805.

ILLINOIS **Frederikssen & Shu Laboratories, Inc.,** 531 West Golf Road, Arlington Heights, IL 60005. Tel: (312) 956-0710.

MARYLAND **MicroCom Design, Inc.,** 9696 Deere Co. Road, Timonium, MD 21093.Tel: (301) 561-4811.

MASSACHUSETTS **Custom Silicon, Inc.,** 600 Suffolk Road, Lowell, MA 01854. Tel: (617) 454-4600.

North American distributors

ALABAMA **Pioneer/Technologies,** 4825 University Square, Huntsville, AL 35805. Tel: (205) 837-9300 Twx: 810-726-2197.

Hammond, 4411 B Evangel Circle, Huntsville, AL 35816. Tel: (205) 830-4764. Fax: (205) 830-4287.

ARIZONA **Insight Electronics,** 1525 W. University Dr., Suite 105, Tempe, AZ 85282. Tel: (602) 829-1800 Twx: 510-601-1618 Fax: (602) 967-2658.

Wyle-Phoenix, 17855 No. Black Canyon Hwy., Phoenix, AZ 85023. Tel: (602) 866-2888 Fax: 602-866-6937.

CALIFORNIA **Cypress Electronics (Corp.),** 2175 Martin Ave., Santa Clara, CA 95050. Tel: (408) 980 2500 Fax: (408) 986-9584.

Cypress Electronics, 6230 Descanso Ave., Buena Park, CA 90620. Tel: (714) 521-5230 Tlx: 5215716 Fax: (714) 521-5716.

Insight Electronics (Corp.), 6885 Flanders Dr., Unit G, San Diego, CA 92121. Tel: (619) 587-0471 Twx: 183035 Fax: (619) 587-1380.

Insight Electronics, 28035 Dorothy Dr., Suite 220, Agoura CA 91301. Tel: (818) 707-2100 Fax: (818) 707-0321.

Insight Electronics, 3505 Cadillac Ave., Unit E-1, Costa Mesa CA 92626. Tel: (714) 556-6890 Twx: 62354990 Fax: (714) 556-6897.

Pacesetter Electronics, 5417 E. La Palma Avenue, Anaheim, CA 92807. Tel: (714) 779-5855.

Wyle-Santa Clara, 3000 Bowers Av., Santa Clara, CA 95051. Tel: (408) 727-2500 Twx: 910-338-0296 Fax: 408-727-5896.

Wyle-Sacramento, 11151 Sun Center Drive, Rancho Cordova, CA 95670. Tel: (916) 638-5282 Fax: 916-638-1491.

Wyle-Irvine, 17872 Cowan Ave., Irvine, CA. Tel: (714) 863-9953 Twx: 3719599 Fax: (714) 863-0473.

Wyle-L.A./San Fernando, 26677 West Agoura Rd., Calabasas, CA 91302. Tel: (818) 880-9000 Twx: 3103720232 Fax: 818-880-5510.

Wyle-San Diego, 9525 Chesapeake Dr., San Diego, CA 92123. Tel: (619) 565-9171 Fax: 619-565-0512.

NORTH CAROLINA **Hammond,** 2923 Pacific Ave., Greensboro, NC 27406. Tel: (919) 275-6391 Tlx: 62894645 Fax: (919) 275-6391.

Pioneer/Technologies, 9801A South Pine Blvd., Charlotte, NC 28210. Tel: (704) 527-8188 Twx: 810-621-0366.

COLORADO **Cypress Electronics,** 12441 West 49th Ave., Wheatridge, CO 80033. Tel: (303) 431-2622 Fax: (303) 431-7191.

Wyle-Denver, 451 East 124th St., Thornton, CO 80241. Tel: (303) 457-9953 Twx: 9109360770 Fax: 303-457-4831.

CONNECTICUT **Jaco Electronics,** 384 Pratt Street, Meriden, CT 06450. Tel: (203) 235-1422.

Pioneer/Standard, 112 Main Street, Norwalk, CT 06851. Tel: (203) 853-1515 Twx: 710 468 3373.

FLORIDA **All American,** 16251 NW 54th Avenue, Miami, FL33014. Tel: (305) 621-3282.

Hammond (Corp.), 6600 N.W. 21st Ave., Ft. Lauderdale, FL 33309. Tel: (305) 973-7103 Twx: (510) 956-9401.

Hammond, 1230 West Central Blvd., Orlando, FL 32802. Tel: (305) 849-6060 Twx: 810-850-4121 Fax: (305) 648-8584.

Pioneer/Technologies, 674 South Military Trail, Deerfield Beach, FL 33442. Tel: (305) 428-8877 Twx: 510-955-9653.

Pioneer/Technologies, 337 South Northlake Blvd., Suite 1000, Altamonte Springs, FL 32701. Tel: (305) 834-9090 Twx: 810-853-0284.

GEORGIA **Hammond,** 5860 Oakbrook Pkwy, Suite 160, Norcross, GA 30093. Tel: (404) 449-1996 Fax: (404) 242-9834.
Pioneer/Technologies, 3100 F Northwoods Pl., Norcross, GA 30071. Tel: (404) 448-1711 Twx: 810-766-4515.

INDIANA **Pioneer/Standard,** 6408 Castleplace Dr., Indianapolis, IN 46250. Tel: (317) 849-7300 Twx: 810-260-1794.

ILLINOIS **Advent Electronics,** Rosamont, IL 60018. Tel: (312) 297-6200 Twx: 910 233 2477.
Pioneer/Standard, 2171 Executive Drive, Addison, ILL 60101. Tel: (312) 495-9680.

KANSAS **Pioneer,** 10551 Lackman Rd., Lenexa, KS 66215. Tel: (913) 492-0500 Twx: 510-601-6411.

MASSACHUSETTS **Emtel Electronics,** 375 Vanderbilt Ave., Norwood, MA 02062. Tel: (617) 769-9500 Fax: (617) 769-8329.
Jaco Electronics, 222 Andover Street, Wilmington, MA 01877. Tel: (617) 273-1860.
Pioneer/Standard, 44 Hartwell Avenue, Lexington, MA 02173. Tel: (617) 861-9200 Twx: 710-326-6617.
Textrel Semi (Die only), 56 Middlesex Turnpike, Burlington, MA 01303. Tel: (617) 270-9246.

MARYLAND **Jaco Electronics,** Rivers Center, 10270 Old Columbia Road, Columbia, MD 21046 Tel: (301) 995-6620.
Pioneer/Tech. Group. Inc., 9100 Gaither Rd., Gaithersburg, MD 20877. Tel: (301) 921-0660 Twx: 710-828-0545 Fax: (301) 921-4255.

MICHIGAN **Pioneer/Standard,** 13485 Stamford, Livonia, MI 48150. Tel: (313) 525-1800 Twx: 810-242-3271.
Pioneer, 4505 Broadmoore Ave., S.E., Grand Rapids, MI 49508. Tel: (616) 698-1800 Twx: 510-600-8456.

MINNEAPOLIS **Cypress Electronics,** 7650 Executive Drive, Eden Prairie, MN 55334. Tel: (612) 934-2104 Fax: (612) 934 2057.
Industrial Components, Inc., Minneapolis, MN 55435. Tel: (612) 831-2666 Twx: 910 576 3153.
Pioneer/Standard, 10203 Bren Road East, Minnetonka, MN 55343. Tel: (612) 944-3355 Twx: 910-576-2738.

NEW JERSEY **Jaco Electronics,** 555 Preakness Road, Tontoa, NJ 07512. Tel: (201) 942-4000.
Pioneer/Standard, 45 Rte. 46 Pinebrook, NJ 07058. Tel: (201) 575-3510 Twx: 710-734-4382.
General Components, Inc., 245 D Clifton Ave., W. Berlin, NJ 08091. Tel: (609) 768-6767 Twx: 920-333-3057.

NEW YORK **Add Electronics,** 7 Adler Drive, E. Syracuse, NY 13057. Tel: (315) 437-1835.
Jaco Electronics, Hauppauge, NY 11787. Tel: (516) 273-5500 Twx: 510-227-6232 Fax: (516) 273-5799.
Mast, 95 Oser Ave., Hauppauge, NJ 11788. Tel: (516) 273-4422 Twx: 4974384.
Pioneer/Standard, 68 Corporate Drive, Binghamton, NY 13904. Tel: (607) 722-9300 Twx: 510-252-0893.
Pioneer/Standard, 60 Crossways Park West, Woodbury, NY 11797. Tel: (516) 921-8700 Twx: 510-221-2184 Fax: (516) 921-2143.
Pioneer/Standard, 840 Fairport Park, Fairport Park, NY 14450. Tel: (716) 381-7070 Twx: 510-253-7001.

OHIO **Pioneer/Standard,** 4800 East 131st St., Cleveland, OH 44105. Tel: (216) 587-3600 Twx: 810-421-0011 Fax: (216) 587-3906.
Pioneer, 4433 Interpoint Bl., Dayton, OH 45424. Tel: (513) 236-9900 Twx: 810 459 1622.

OREGON **Cypress Electronics,** 15075 S.W. Coll Parkway, Suite D, Beaverton, OR 97006. Tel: (503) 641-2233 Fax: (503) 643-1237.
Wyle-Portland, 5250 N.E. Elam Young Pkwy., Suite 600, Portland, OR 97123. Tel: (503) 640-6000 Fax: 503-640-5846.

PENNSYLVANIA **Advacom Electronics,** 5620 West Road, McKean, PA 16426. Tel: (814) 476-7774.
Pioneer/Technologies, 261 Gibraltar Rd., Horsham, PA 19044. Tel: (215) 674-4000 Twx: 510-665-6778.
Pioneer/Standard, 259 Kappa Drive, Pittsburg, PA 15238. Tel: (412) 782-2300 Twx: 710-795-3122.

TEXAS **Pioneer/Standard,** 9901 Burnet Road, Austin, TX 78758. Tel: (512) 835-4000 Twx: 910-874-1323.
Pioneer/Standard, 13710 Omega Road, Dallas, TX 75244. Tel: (214) 386-7300 Twx: 910-860-5563 Fax: (214) 490-6419.
Pioneer/Standard, 5853 Point West Drive, Houston, TX 77056. Tel: (713) 988-5555 Twx: 910-881-1606 Fax: (713) 988-1732.
Wyle-Dallas, 1810 North Greenville Ave., Richardson, TX 75083. Tel: (214) 235-9953 Fax: 214-644-5064.
Wyle-Houston, 11001 So. Hilcrest, Suite 100, Houston, TX 77099. Tel: (713) 879-9953 Fax: 713-879-6540.
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